JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

Course structure and syllabus for M.Tech. DIGITAL SYSTEMS & COMPUTER ELECTRONICS (DSCE) for affiliated Engineering Colleges 2009-10

I YEAR I SEMESTER

Subject	Hours/ Week
Digital System Design	4
Embedded System Concepts	4
Advanced Data Communications	4
Neural Networks & Applications	4
Advanced Computer Architecture	4
ELECTIVE I	4
Network Security & Cryptography	
DSP Processors & Architectures	
Low Power VLSI Design	
LABORATORY: Digital Systems Design Lab	4

I YEAR II SEMESTER

Subject	Hours/ Week
Design of Fault Tolerant Systems	4
Systems Programming	4
Microcomputer System Design	4
Hi-speed Networks	4
Image & Video Processing	4
ELECTIVE II	4
System Modeling & Simulation	
Algorithms for VLSI Design Automation	
FPGA Architecture & Applications	
LABORATORY:	
Signal Processing & Micro Processors Lab	4

II YEAR (III & IV Semesters)

SUBJECTS
Seminar
Project work

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. (DSCE)

I SEMESTER

DIGITAL SYSTEM DESIGN

UNIT I

DESIGN OF DIGITAL SYSTEMS: ASM charts, Hardware description language and control sequence method, Reduction of state tables, state assignments.

UNIT II

SEQUENTIAL CIRCUIT DESIGN: design of Iterative circuits, design of sequential circuits using ROMs and PLAs, sequential circuit design using CPLD, FPGAs.

UNIT III

FAULT MODELING: Fault classes and models, Stuck at faults, bridging faults, transition and intermittent faults.

TEST GENERATION: Fault diagnosis of Combinational circuits by conventional methods – Path Sensitization technique, Boolean difference method, Kohavi algorithm.

UNIT IV

TEST PATTERN GENERATION: D–algorithm, PODEM, Random testing, transition count testing, Signature analysis and testing for bridging faults.

UNIT V

FAULT DIAGNOSIS IN SEQUENTIAL CIRCUITS: State identification and fault detection experiment. Machine identification, Design of fault detection experiment.

UNIT VI

PROGRAMMING LOGIC ARRAYS: Design using PLA's, PLA minimization and PLA folding.

UNIT VII

PLA TESTING: Fault models, Test generation and Testable PLA design.

UNIT VIII

ASYNCHRONOUS SEQUENTIAL MACHINE: Fundamental mode model, flow table, state reduction, minimal closed covers, races, cycles and hazards.

TEXTBOOKS:

1. Z. Kohavi – "Switching & finite Automata Theory" (TMH)
2. N. N. Biswas – "Logic Design Theory" (PHI)
3. Nolman Balabanian, Bradley Calson – "Digital Logic Design Principles" – Wily Student Edition 2004.

REFRENCES:

1. M. Abramovici, M. A. Breues, A. D. Friedman – "Digital System Testing and Testable Design", Jaico Publications
2. Charles H. Roth Jr. – "Fundamentals of Logic Design".
3. Frederick. J. Hill & Peterson – "Computer Aided Logic Design" – Wiley 4th Edition

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. (DSCE)

I SEMESTER

EMBEDDED SYSTEM CONCEPTS

UNIT I

INTRODUCTION: Embedded system overview, embedded hardware units, embedded software in a system, embedded system on chip (SOC), design process, classification of embedded systems

UNIT II

EMBEDDED COMPUTING PLATFORM: CPU Bus, memory devices, component interfacing, networks for embedded systems, communication interfacings: RS232/UART, RS422/RS485, IEEE 488 bus.

UNIT III

SURVEY OF SOFTWARE ARCHITECTURE: Round robin, round robin with interrupts, function queue scheduling architecture, selecting an architecture saving memory space

UNIT IV

EMBEDDED SOFTWARE DEVELOPMENT TOOLS: Host and target machines, linkers, locations for embedded software, getting embedded software into target system, debugging technique

UNIT V

RTOS CONCEPTS: Architecture of the kernel, interrupt service routines, semaphores, message queues, pipes

UNIT VI

INSTRUCTION SETS; Introduction, preliminaries, ARM processor, SHARC processor.

UNIT VII

SYSTEM DESIGN TECHNIQUES:

Design methodologies, requirement analysis, specifications, system analysis and architecture design

UNIT VIII

DESIGN EXAMPLES: Telephone PBX, ink jet printer, water tank monitoring system, GPRS, Personal Digital Assistants, Set Top boxes..

TEXT BOOKS:

1. Computers as a component: principles of embedded computing system design- wayne wolf
2. An embedded software premier: David E. Simon
3. Embedded / real time systems-KVKK Prasad, Dreamtech press, 2005

REFERENCES:

1. Embedded real time systems programming-sri ram V Iyer, pankaj gupta, TMH, 2004
2. Embedded system design- A unified hardware/software introduction- frank vahid, tony D. Givargis, John Willey, 2002

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. (DSCE)

I SEMESTER

ADVANCED DATA COMMUNICATIONS

UNIT I

DIGITAL MODULATION: Introduction, Information Capacity Bits, Bit Rate, Baud, and M-ARY Coding, ASK, FSK, PSK, QAM, BPSK, QPSK, 8PSK, 16PSK, 8QAM, 16QAM, DPSK, Methods, Band Width Efficiency, Carrier Recovery, Clock Recovery.

UNIT II&III

BASIC CONCEPTS OF DATA COMMUNICATIONS, INTERFACES AND MODEMS: Data Communication, Components, Networks, Distributed Processing, Network Criteria- Applications, Protocols and Standards, Standards Organizations, Regulatory Agencies, Line Configuration- Point-to-point- Multipoint, Topology, Mesh, Star, Tree, Bus, Ring, Hybrid Topologies, Transmission Modes, Simplex, Half duplex- Full Duplex, Categories of Networks- LAN, MAN, WAN and Internetworking, Digital Data Transmission- Parallel and Serial, DTE-DCE Interface- Data Terminal Equipment, Data Circuit- Terminating Equipment, Standards EIA 232 Interface, Other Interface Standards, Modems- Transmission Rates.

UNIT IV

ERROR DETECTION AND CORRECTION: Types of Errors- Single- Bit Error, CRC (Cyclic Redundancy Check), Performance, Checksum, Error Correction- Single-Bit Error Correction, Hamming Code.

UNIT V

DATA LINK CONTROL: Stop and Wait, Sliding Window Protocols.

DATA LINK PROTOCOLS: Asynchronous Protocols, Synchronous Protocols, Character Oriented Protocol- Binary Synchronous Communication (BSC) - BSC Frames- Data Transparency, Bit Oriented Protocols, HDLC, Link Access Protocols**.**

UNIT VI

SWITCHING*:* Circuit Switching- Space Division Switches- Time Division Switches, TDM Bus, Space and Time Division Switching Combinations, Public Switched Telephone Network, Packet Switching- Datagram Approach- Virtual Circuit Approach, Circuit Switched Connection Versus Virtual Circuit Connection, Message Switching.

MULTIPLEXING: Time Division Multiplexing (TDM), Synchronous Time Division Multiplexing, Digital Hierarchy, Statistical Time Division Multiplexing.

UNIT VII&VIII

MULTIPLE ACCESS: Random Access, Aloha- Carrier Sense Multiple Access (CSMA)- Carrier Sense Multiple Access with Collision Detection (CSMA)- Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA), Controlled Access- Reservation- Polling- Token Passing, Channelization- Frequency- Division Multiple Access (FDMA), Time - Division Multiple Access (TDMA), - Code - Division Multiple Access (CDMA).

TEXT BOOKS:

1. B. A.Forouzan, "Data Communication and Computer Networking", 3rd ed., TMH, 2008.
2. W. Tomasi, "Advanced Electronic Communication Systems", 5 ed., PEI2008.

REFERENCES:

1. Prakash C. Gupta, "Data Communications and Computer Networks", PHI, 2006.
2. William Stallings, "Data and Computer Communications", 8th ed., PHI 2007.
3. T. Housely, "Data Communication and Tele Processing Systems", 2nd Edition, BSP, 2008.

4. Brijendra Singh, "Data Communications and Computer Networks", 2nd ed., PHI 2005.

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M.Tech. (DSCE)

I SEMESTER

NEURAL NETWORKS & APPLICATIONS

UNIT I

INTRODUCTION: History of Neural Networks, Structure and functions of biological and artificial neuron, Neural network architectures, learning methods, evaluation of neural networks.

UNIT II

SUPERVISED LEARNING - I: McCulloch- Pitts neuron model, perception learning, Delta learning, Windrow- Hoff learning rules, linear seperability, Adeline modification.

UNIT III

SUPERVISED LEARNING –II MULTI LAYER NETWORKS: Architectures, Madalines, Back propagation algorithm, importance of learning parameter and momentum term, radial basis functions, polynomial networks.

UNIT IV&V

UNSUPERVISED LEARNING : Winner-Take- all learning, out star learning, learning vector quantizers, Counter propagation networks, Kohonen self – organizing networks, Grossberg layer, adaptive resonance theory, Hamming net.

UNIT VI

ASSOCIATIVE MEMORIES: Hebbian learning rule, continues and discrete Hopfild networks, recurrent and associative memory, Boltzman machines, Bi-directional associative memory.

UNIT VII&VIII

APPLICATIONS OF NEURAL NETWORKS: Optimization, Travelling Salesman problem, solving simultaneous linear equations, application in pattern recognition and image processing. Pattern recognition, Optimization, Associative memories, speech and decision-making. VLSI implementation of neural networks.

TEXT BOOKS:

1. J.M. Zurada, "Introduction to Artificial Neural Systems" - Jaico Publishing House, Bombay,2001.
2. Kishan Mehrotra , Chelkuri. K.Mohan, Sanjay Ranka, "Elements of Artificial Neural Networks", Penram International
3. B.Yagnanarayana, "Artificial Neural Networks", PHI, New Delhi.

REFERENCES:

1. S.N Sivanandham, S. sumathi, S.N.Deepa,"Introduction to Neural networks using matlab 6.0", Tata McGraw Hill, New Delhi, 2005.
2. P.D. wasserman, "Neural computing theory & practice", ANZA PUB.

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M.Tech. (DSCE)

I SEMESTER

ADVANCED COMPUTER ARCHITECTURE

UNIT I

FUNDAMENTALS OF COMPUTER DESIGN: Technology trends, cost- measuring and reporting performance quantitative principles of computer design.

UNIT II

INSTRUCTION SET PRINCIPLES AND EXAMPLES: classifying instruction set, memory addressing, type and size of operands, addressing modes for signal processing, operations in the instruction set- instructions for control flow- encoding an instruction set.- the role of compiler

UNIT III

INSTRUCTION LEVEL PARALLELISM (ILP): over coming data hazards- reducing branch costs, high performance instruction delivery, hardware based speculation, limitation of ILP

UNIT IV

ILP SOFTWARE APPROACH: Compiler Techniques, Static Branch Protection, VLIW Approach, H.W support for more ILP at compile time- H.W verses S.W solutions

UNIT V

MEMORY HIERARCHY DESIGN: cache performance, reducing cache misses penalty and miss rate, virtual memory, protection and examples of VM.

UNIT VI

MULTIPROCESSORS AND THREAD LEVEL PARALLELISM: symmetric shared memory architectures, distributed shared memory, Synchronization, multi threading.

UNIT VII

STORAGE SYSTEMS: Types, Buses, RAID, errors and failures, bench marking a storage device, designing a I/O system.

UNIT VIII

INTER CONNECTION NETWORKS AND CLUSTERS: Interconnection network media, practical issues in interconnecting networks, examples, clusters, designing a cluster

TEXT BOOKS:

1. John. Hennessy & David A. Patterson Morgan Kufmann, ”Computer Architecture A quantitative approach”, 3rd edition (An Imprint of Elsevier)

REFERENCES:

1. Kai Hwang and A.Briggs, “Computer Architecture and parallel Processing”, International Edition McGraw-Hill.
2. Dezso Sima, Terence Fountain, Peter Kacsuk, “Advanced Computer Architectures”, Pearson.

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M.Tech.(DSCE)

I SEMESTER

NETWORK SECURITY & CRYPTOGRAPHY
(ELECTIVE I)

UNIT I

INTRODUCTION: Attacks, Services and Mechanisms, Security attacks, Security services, A Model for Internet work security. CLASSICAL TECHNIQUES: Conventional Encryption model, Steganography, Classical Encryption Techniques.

UNIT II

MODERN TECHNIQUES: Simplified DES, Block Cipher Principles, Data Encryption standard, Strength of DES, Differential and Linear Cryptanalysis, Block Cipher Design Principles and Modes of operations.

ALGORITHMS: Triple DES, International Data Encryption algorithm, Blowfish, RC5, CAST-128, RC2, Characteristics of Advanced Symmetric block cifers.

UNIT II

CONVENTIONAL ENCRYPTION: Placement of Encryption function, Traffic confidentiality, Key distribution, Random Number Generation.

PUBLIC KEY CRYPTOGRAPHY: Principles, RSA Algorithm, Key Management, Diffie-Hellman Key exchange, Elliptic Curve Cryptography.

UNIT IV

NUMBER THEORY: Prime and Relatively prime numbers, Modular arithmetic, Fermat's and Euler's theorems, Testing for primality, Euclid's Algorithm, the Chinese remainder theorem, Discrete logarithms.

MESSAGE AUTHENTICATION AND HASH FUNCTIONS: Authentication requirements and functions, Message Authentication, Hash functions, Security of Hash functions and MACs.

UNIT V

HASH AND MAC ALGORITHMS: MD File, Message digest Algorithm, Secure Hash Algorithm, RIPEMD-160, HMAC.

DIGITAL SIGNATURES AND AUTHENTICATION PROTOCOLS: Digital signatures, Authentication Protocols, Digital signature standards.

UNIT VI

AUTHENTICATION APPLICATIONS: Kerberos, X.509 directory Authentication service.

ELECTRONIC MAIL SECURITY: Pretty Good Privacy, S/MIME.

UNIT VII

IP SECURITY: Overview, Architecture, Authentication, Encapsulating Security Payload, Combining security Associations, Key Management.

WEB SECURITY: Web Security requirements, secure sockets layer and Transport layer security, Secure Electronic Transaction.

UNIT VIII

INTRUDERS, VIRUSES AND WORMS: Intruders, Viruses and Related threats. FIRE WALLS: Fire wall Design Principles, Trusted systems.

TEXT BOOKS

1. Cryptography and Network Security: Principles and Practice - William Stallings, Pearson Education., 2000.

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I SEMESTER

DSP PROCESSORS & ARCHTECTURE
(ELECTIVE I)

UNIT I

INTRODUCTION TO DIGITAL SIGNAL PROCESING: Introduction, A Digital signal-processing system, The sampling process, Discrete time sequences. Discrete Fourier Transform (DFT) and Fast Fourier Transform (FFT), Linear time-invariant systems, Digital filters, Decimation and interpolation, Analysis and Design tool for DSP Systems MATLAB, DSP using MATLAB.

UNIT II

COMPUTATIONAL ACCURACY IN DSP IMPLEMENTATIONS: Number formats for signals and coefficients in DSP systems, Dynamic Range and Precision, Sources of error in DSP implementations, A/D Conversion errors, DSP Computational errors, D/A Conversion Errors, Compensating filter.

UNIT III

ARCHITECTURES FOR PROGRAMMABLE DSP DEVICES: Basic Architectural features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Speed Issues, Features for External interfacing.

UNIT IV

EXECUTION CONTROL AND PIPELINING: Hardware looping, Interrupts, Stacks, Relative Branch support, Pipelining and Performance, Pipeline Depth, Interlocking, Branching effects, Interrupt effects, Pipeline Programming models.

UNIT V

PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Commercial Digital signal-processing Devices, Data Addressing modes of TMS320C54XX DSPs, Data Addressing modes of TMS320C54XX Processors, Memory space of TMS320C54XX Processors, Program Control, TMS320C54XX instructions and Programming, On-Chip Peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54XX Processors.

UNIT VI

IMPLEMENTATIONS OF BASIC DSP ALGORITHMS: The Q-notation, FIR Filters, IIR Filters, Interpolation Filters, Decimation Filters, PID Controller, Adaptive Filters, 2-D Signal Processing.

UNIT VII

IMPLEMENTATION OF FFT ALGORITHMS: An FFT Algorithm for DFT Computation, A Butterfly Computation, Overflow and scaling, Bit-Reversed index generation, An 8-Point FFT implementation on the TMS320C54XX, Computation of the signal spectrum.

UNIT VIII

INTERFACING MEMORY AND I/O PERIPHERALS TO PROGRAMMABLE DSP DEVICES: Memory space organization, External bus interfacing signals, Memory interface, Parallel I/O interface, Programmed I/O, Interrupts and I/O, Direct memory access (DMA). A Multichannel buffered serial port (McBSP), McBSP Programming, a CODEC interface circuit, CODEC programming, A CODEC-DSP interface example.

TEXT BOOKS:

1. Digital Signal Processing – Avtar Singh and S. Srinivasan, Thomson Publications, 2004.
2. DSP Processor Fundamentals, Architectures & Features-Lapsley et al.S. Chand & Co, 2000.

REFERENCES:

1. Digital Signal Processors, Architecture, Programming and Applications–B. Venkata Ramani and M. Bhaskar, TMH, 2004.
2. Digital Signal Processing – Jonatham Stein, John Wiley, 2005.

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I SEMESTER

LOW POWER VLSI DESIGN
(ELECTIVE I)

UNIT I

LOW POWER DESIGN, AN OVER VIEW: Introduction to low- voltage low power design, limitations, Silicon-on-Insulator.

UNIT II

MOS/BiCMOS PROCESSES: Bi-CMOS processes, Integration and Isolation considerations, Integrated Analog/Digital CMOS Process.

UNIT III

LOW-VOLTAGE/LOW POWER CMOS/ BICMOS PROCESSES: Deep submicron processes, SOI CMOS, lateral BJT on SOI, future trends and directions of CMOS/Bi-CMOS processes.

UNIT IV

DEVICE BEHAVIOR AND MODELING: Advanced MOSFET models, limitations of MOSFET models, Bipolar models. Analytical and Experimental characterization of sub-half micron MOS devices, MOSFET in a Hybrid mode environment.

UNIT V

CMOS AND Bi-CMOS LOGIC GATES: Conventional CMOS and Bi-CMOS logic gates, Performance Evaluation.

UNIT VI

LOW- VOLTAGE LOW POWER LOGIC CIRCUITS: Comparison of advanced Bi-CMOS Digital circuits. ESD-free Bi-CMOS, Digital circuit operation and comparative Evaluation.

UNIT VII

LOW POWER LATCHES AND FLIP FLOPS: Evolution of Latches and Flip flops-quality measures for latches and Flip flops, Design perspective.

UNIT VIII

SPECIAL TECHNIQUES: Power Reduction in Clock Networks, CMOS Floating Node, Low Power Bus, Delay Balancing, Low Power Techniques for SRAM.

TEXT BOOKS:

1. CMOS/BiCMOS ULSI low voltage, low power by Yeo Rofail/ Gohl(3 Authors)-Pearson Education Asia 1st Indian reprint,2002.
2. Gary K. Yeap,"Practical Low Power Digital VLSI Design", KAP, 2002.

REFERENCES:

1. Basic VLSI Design,Douglas A.Pucknell & Kamran Eshraghian,3rd edition PHI.
2. Digital Integrated circuits, J.Rabaey PH. N.J 1996
3. CMOS Digital ICs Sung-mo Kang and yusuf leblebici 3rd edition TMH 2003 .
4. IEEE Trans Electron Devices, IEEE J.Solid State Circuits, and other National and International Conferences and Symposia.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech.(DSCE) I SEMESTER

DIGITAL SYSTEMS DESIGN LAB

CYCLE 1:

1. Simulation and Verification of Logic Gates.
2. Design and Simulation of Half adder, Serial Binary Adder, Multi Precession Adder, Carry Look Ahead Adder and Full Adder.
3. Simulation and Verification of Decoder, MUXs, Encoder using all Modeling Styles.
4. Modeling of Flip-Flops with Synchronous and Asynchronous reset.
5. Design and Simulation of Counters- Ring Counter, Johnson Counter, and Up- Down Counter, Ripple Counter.
6. Design of a N- bit Register of Serial-in Serial-out, Serial in Parallel out, Parallel in Serial out and Parallel in Parallel Out.
7. Design of Sequence Detector (Finite State Machine- Mealy and Moore Machines).
8. 4- Bit Multiplier, Divider. (for 4-Bit Operand)
9. Design ALU to Perform – ADD, SUB, AND-OR, 1's and 2's COMPLIMENT, Multiplication, Division.

CYCLE 2: After completing cycle 1, Digital Circuit Description Using Verilog/ VHDL.

1. Verification of the Functionality of the circuit using function Simulators.
2. Timing Simulator for Critical Path time Calculation.
3. Synthesis of Digital Circuit.
4. Place and Router Techniques for FPGA's like Xilinx, Altera, Cypress, etc.,
5. Implementation of Design using FPGA and CPLD Devices.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech.(DSCE)

II SEMESTER

DESIGN OF FAULT TOLERANT SYSTEMS

UNIT I

BASIC CONCEPTS: Reliability concepts, Failure & Faults, Reliability and failure rate, Relation between reliability and Mean time between failure, Maintainability and Availability, Reliability of series, Parallel and Parallel-Series combinational circuits.

UNIT II

FAULT TOLERANT DESIGN: Basic concepts – Static, dynamic, hybrid, Triple Modular Redundant System, Self purging redundancy, Siftout redundancy (SMR), SMR Configuration, Use of error correcting code, Time redundancy and software redundancy.

UNIT III

SELF CHECKING CIRCUITS: Basic concepts of Self checking circuits, Design of Totally Self Checking checker, Checkers using m out of n codes, Berger code, Low cost residue code.

UNIT IV

FAIL SAFE DESIGN: Strongly fault secure circuits, fail safe design of sequential circuits using partition theory and Berger code, Totally self checking PLA design.

UNIT V

DESIGN FOR TESTABILITY FOR COMBINATIONAL CIRCUITS: Basic concepts of testability, controllability and observability, the Reed Muller's expansion technique, OR-AND-OR design, use of control and syndrome testable design.

UNIT VI

Theory and operation of LFSR, LFSR as Signature analyzer, Multiple-input Signature Register.

UNIT VII

DESIGN FOR TESTABILITY FOR SEQUENTIAL CIRCUITS: Controllability and observability by means of scan register, Storage cells for scan design, classic scan design, Level Sensitive Scan Design (LSSD).

UNIT VIII

BUILT IN SELF TEST: BIST concepts, Test pattern generation for BIST exhaustive testing, Pseudorandom testing, pseudo exhaustive testing, constant weight patterns, Generic offline BIST architecture.

TEXT BOOKS:

1. Parag K. Lala – "Fault Tolerant & Fault Testable Hardware Design" (PHI)
2. M. Abramovili, M.A. Breues, A. D. Friedman – "Digital Systems Testing and Testable Design" Jaico publications.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech. (DSCE)

II SEMESTER

SYSTEMS PROGRAMMING

UNIT I

LANGUAGE PROCESSORS: Introduction, Language Processing Activities, Fundamentals of Language Processing, Fundamental of Language Specifications, Language Processors Development Tools.

UNIT II

DATA STRUCTURES FOR LANGUAGE PROCESSING: Search Data Structures, Allocation Data Structures.

UNIT III

SCANNING ANG PARSING:

Scanning: Introduction, Finite State Automata, regular Expressions, Building DFA's, Performing Semantic Actions, Writing a Scanner.

Parsing: Introduction, Parse Trees and Abstract Syntax Trees, Top Down Parsing and its Algorithm, Predictions and Backtracking, Implementing Top Down Parsing, Comments on Top Down Parsing, Top Down Parsing Without Back Tracking, Practical Top Down Parsing, Bottom Up Parsing and its Algorithm, Simple Precedence, Simple Precedence grammar, Operator Precedence Grammars, Operator Precedence Parsing, Algorithms, LALR Parsing.

UNIT IV

ASSEMBLERS: Elements of Assembly Language Programming, A Simple Assembly Scheme, Pass Structure of Assemblers, A single Pass Assembler for IBM PC.

UNIT V

MACROS AND MACRO PROCESSORS: Macro Definition and Call, Macro Expansion, Nested Macro Calls, Advanced Macro Facilities, Design of Macro Processors.

UNIT VI

COMPILERS AND INTERPRETERS: Aspects of Compilation, Memory Allocation, Compilation of Expressions, Compilation of Control Structures, Code Optimization, Interpreters.

UNIT VII

LINKERS: Relocation and Linking Concepts, Design of Linkers, Self Relocation Programs, A Linker for MS DOS, Linking for Overlays, Loaders.

UNIT VIII

SOFTWARE TOOLS: Software Tools for Program Development, Editors, Debug Monitors, Programming Environments, User Interfaces.

TEXT BOOKS:

1. Systems Programming and Operating Systems by D.M.Dhamdhere, 2nd edition, TMH.

REFERENCES:

1. Systems Programming by John J. Donovan, Mc. Graw Hill International Editions.

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II SEMESTER

MICRO COMPUTER SYSTEM DESIGN

UNIT I

REVIEW OF 8086 PROCESSOR: Architecture, Register organization, Addressing Modes and Instruction Set (Brief treatment only), Difference between 8086 and 8088 with rest to pin structures.

UNIT II

THE 80286 MICRO PROCESSORS: Architecture, Register Organization, Addressing Modes and instruction sets of 80286 (brief treatment only)

UNIT III

THE 80386, AND 80486 MICRO PROCESSORS: Architectural features, Register Organization, Memory management, Virtual 8086 mode, The Memory Paging Mechanism, Pin Definitions of 80386 and 80486 (brief treatment).

UNIT IV

THE PENTIUM AND PENTIUM PRO PROCESSORS: The Memory System, Input/output system, Branch Prediction Logic, Cache Structure, Pentium Registers, Serial Pentium pro features.

UNIT V

THE PENTIUM IV AND DUAL CORE MICRO PROCESSORS: Architecture, Special Registers and Pin Structures (brief treatment only)

UNIT VI

I/O PROGRAMMING: Fundamentals of I/O, Considerations Programmed I/O, Interrupt I/O, Block Transfers and DMA, I/O Design Example.

UNIT VII

INTRODUCTION TO MULTIPROGRAMMING: Process Management, Semaphores Operations, Common Procedure Sharing, Memory Management, Virtual Memory Concept of 80286 and other advanced Processors.

UNIT VIII

ARITHMETIC COPROCESSOR, MMX AND SIMD TECHNOLOGIES: Data formals for Arithmetic Coprocessor, Internal Structure of 8087 and Advanced Coprocessors. Instruction Set (brief treatment).

TEXTBOOKS:

1. Barry, B. Brey, "The Intel Microprocessors,"8th Edition Pearson Education, 2009.
2. A.K. Ray and K.M. Bhurchandi,"Advanced Microprocessor and Peripherals," TMH.

.

REFERENCES:

1. YU-Chang, Glenn A. Gibson, "Micro Computer Systems: The 8086/8088 Family Architecture, Programming and Design" 2nd Edition, Pearson Education, 2007
2. Douglas V. Hall, "Microprocessors and Interfacing," Special Indian Edition, 2006.

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II SEMESTER

HI-SPEED NETWORKS

UNITI

NETWORK SERVICES & LAYERED ARCHITECTURE: Traffic characterization and quality of service, Network services, High performance networks, Network elements, Basic network mechanisms, layered architecture.

UNIT II

ISDN & B-ISDN: Over view of ISDN, ISDN channels, User access, ISDN protocols, Brief history of B-ISDN and ATM, ATM based services and applications, principles and building block of B-ISDN, general architecture of B-ISDN, frame relay.

UNIT III

ATM NETWORKS: Network layering, switching of virtual channels and virtual paths, applications of virtual channels and connections.

UNIT IV

QOS parameters, traffic descriptors, ATM service categories, ATM cell header, ATM layer, ATM adaptation layer.

UNIT V

INTERCONNECTION NETWORKS: Introduction, Banyan Networks, Routing algorithm & blocking phenomenon, Batcher-Banyan networks, crossbar switch, three stage class networks.

UNIT VI

REARRANGEABLE NETWORKS: Rearrangeable class networks, folding algorithm, bens network, looping algorithm.

UNIT VII

ATM SIGNALING, ROUTING AND TRAFFIC CONTROL: ATM addressing, UNI signaling, PNNI signaling, PNNI routing, ABR Traffic management.

UNIT VIII

TCP/IP NETWORKS: History of TCP/IP, TCP application and Services, Motivation, TCP, UDP, IP services and Header formats, Internetworking, TCP congestion control, Queue management: Passive & active, QOS in IP networks: differentiated and integrated services.

TEXT BOOKS:

1. ISDN & B-ISDN with Frame Relay – William Stallings, PHI.
2. Communication Networks - Leon Garcia widjaja, TMH, 2000.
3. ATM Fundamentals – N. N. Biswas, Adventure books publishers, 1998.

REFERENCES:

1. High Performance TCP/IP Networking – Mahbub Hassan , Raj Jain, PHI, 2005.
2. ATM Networks – Rainer Handel, Manfred N. Hubber, Stefan Schroder, Pearson edu., 2002.
3. High Speed Networks and Internets – William Stallings, Pearson edu., 2002.
4. High Performance Communication Networks – T. Walrand & P. Varaiya, 2nd ed., Harcourt Asia Publ

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II SEMESTER

IMAGE & VIDEO PROCESSING

UNIT I

IMAGE REPRESENTATION: Gray scale and colour Images, image sampling and quantization. Two dimensional orthogonal transforms: DFT, WHT, Haar transform, KLT, DCT.

UNIT II

IMAGE ENHANCEMENT: Filters in spatial and frequency domains, histogram-based processing, homomorphic filtering. Edge detection, non parametric and model based approaches, LOG filters, localization problem.

UNIT III

IMAGE RESTORATION: Degradation Models, PSF, circulant and block - circulant matrices, deconvolution, restoration using inverse filtering, Wiener filtering and maximum entropy-based methods.

UNIT IV

IMAGE SEGMENTATION: Pixel classification, Bi-level Thresholding, Multi-level Thresholding, P-tile method, Adaptive Thresholding, Spectral & spatial classification, Edge detection, Hough transform, Region growing.

UNIT V

FUNDAMENTAL CONCEPTS OF IMAGE COMPRESSION: Compression models, Information theoretic perspective, Fundamental coding theorem.

UNIT VI

LOSSLESS COMPRESSION: Huffman Coding, Arithmetic coding, Bit plane coding, Run length coding, Lossy compression: Transform coding, Image compression standards.

UNIT VII

VIDEO PROCESSING: Representation of Digital Video, Spatio-temporal sampling, Motion Estimation.

UNIT VIII

Video Filtering, Video Compression, Video coding standards.

TEXT BOOKS/REFERENCES:

1. R. C. Gonzalez, R. E. Woods,"Digital Image Processing", Pearson Education. 2nd edition,2002
2. W. K. Pratt, "Digital image processing", Prentice Hall, 1989
3. A. Rosenfold and A. C. Kak, "Digital image processing", Vols. 1 and 2, Prentice Hall, 1986.
4. H. C. Andrew and B. R. Hunt, "Digital image restoration", Prentice Hall, 1977
5. R. Jain, R. Kasturi and B.G. Schunck, "Machine Vision", McGraw-Hill International Edition, 1995
6. A. M. Tekalp, "Digital Video Processing", Prentice-Hall, 1995
7. A. Bovik, "Handbook of Image & Video Processing", Academic Press, 2000

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech (DSCE)

II SEMESTER **SYSTEM MODELING & SIMULATION**

(ELECTIVE II)

UNIT I

BASIC SIMULATION MODELING: Systems, Models and Simulation, Discrete Event Simulation, Simulation of single server queuing system, Simulation of Inventory System, Alternative approach to modeling and simulation.

UNIT II

SIMULATION SOFTWARE: Comparison of simulation packages with Programming languages, Classification of Software, Desirable Software Features, General purpose simulation packages, Arena, Extend and others, Object Oriented Simulation, Examples of application oriented simulation packages.

UNIT III

BUILDING SIMULATION MODELS: Guidelines for determining levels of model detail, Techniques for increasing model validity and credibility.

UNIT IV

MODELING TIME DRIVEN SYSTEMS: Modeling input signals, delays, System integration, Linear Systems, Motion control models, Numerical Experimentation.

UNIT V

EXOGENOUS SIGNALS AND EVENTS: Disturbance signals, State Machines, Petri Nets & Analysis, System encapsulation.

UNIT VI

MARKOV PROCESS: Probabilistic systems, Discrete Time Markov processes, Random walks, Poisson processes, the exponential distribution, simulating a poison process, Continuous-Time Markov processes.

UNIT VII

EVENT DRIVEN MODELS: Simulation diagrams, Queuing theory, simulating queuing systems, Types of Queues, Multiple servers.

UNIT VIII

SYSTEM OPTIMIZATION: System Identification, Searches, Alpha/beta trackers, Multidimensional Optimization, Modeling and Simulation methodology.

TEXT BOOKS:

1. Frank L. Severance, "System Modeling & Simulation, An Introduction", John Wiley & Sons, 2001.
2. Averill M. Law, W. David Kelton, "Simulation Modeling and Analysis", TMH, 3rd Edition, 2003.

REFRENCES:

1. Geoffery Gordon, "Systems Simulation", PHI, 1978.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech.(DSCE)

II SEMESTER

ALGORITHMS FOR VLSI DESIGN AUTOMATION
(ELECTIVE II)

UNIT I

PRELIMINARIES: Introduction to Design Methodologies, Design Automation tools, Algorithmic Graph Theory, Computational complexity, Tractable and Intractable problems.

UNIT II

GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: Backtracking, Branch and Bound, Dynamic Programming, Integer Linear Programming, Local Search, Simulated Annealing, Tabu search, Genetic Algorithms.

UNIT III

Layout Compaction, Placement, Floor planning And Routing Problems, Concepts and Algorithms.

UNIT IV

MODELLING AND SIMULATION: Gate Level Modeling and Simulation, Switch level Modeling and Simulation.

UNIT V

LOGIC SYNTHESIS AND VERIFICATION: Basic issues and Terminology, Binary-Decision diagrams, Two-Level logic Synthesis

UNIT VI

HIGH-LEVEL SYNTHESIS: Hardware Models, Internal representation of the input Algorithm, Allocation, Assignment and Scheduling, Some Scheduling Algorithms, Some aspects of Assignment problem, High-level Transformations.

UNIT VII

PHYSICAL DESIGN AUTOMATION OF FPGA'S: FPGA technologies, Physical Design cycle for FPGA's, partitioning and Routing for segmented and staggered Models.

UNIT VIII

PHYSICAL DESIGN AUTOMATION OF MCM'S

MCM technologies, MCM physical design cycle, Partitioning, Placement- Chip Array based and Full Custom Approaches, Routing, Maze routing, Multiple stage routing, Topologic routing, Integrated Pin, Distribution and routing, Routing and Programmable MCM's.

TEXTBOOKS:

1. S.H.Gerez, "Algorithms for VLSI Design Automation", WILEY Student Edition, John wiley & Sons (Asia) Pvt. Ltd., 1999.
2. Naveed Sherwani, "Algorithms for VLSI Physical Design Automation" ,3rd edition, Springer International Edition, 2005.

REFERENCES:

1. Computer Aided Logical Design with Emphasis on VLSI – Hill & Peterson, Wiley, 1993.
2. Modern VLSI Design Systems on silicon – Wayne Wolf, Pearson Education Asia, 2nd Edition, 1998.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech.(DSCE)

II SEMESTER

FPGA ARCHITECTURE & APPLICATIONS
(ELECTIVE II)

UNIT I

PROGRAMMABLE LOGIC: ROM, PLA, PAL, PLD, PGA – Features, Programming and Applications using Complex Programmable Logic Devices Altera Series – Max 5000/7000 Series and Altera FLEX Logic – 10000 Series CPLD, AMD's – CPLD (Mach 1 To 5); Cypres FLASH 370 Device Technology, Lattice Plsi's Architectures – 3000 Series – Speed Performance and in System Programmability.

UNIT II

FPGA: Field Programmable Gate Arrays – Logic Blocks, Routing Architecture, Design Flow, Technology Mapping J for Fpgas.

UNIT III

CASE STUDIES: Xilinx XC4000 & ALTERA's FLEX 8000/10000 FPGAs: AT & T – ORCA's (Optimized Reconfigurable Cell Array): ACTEL's – ACT-1,2,3 and Their Speed Performance.

UNIT IV

FINITE STATE MACHINES (FSM): Top Down Design – State Transition Table, State Assignments for FPGAs. Problem of Initial State Assignment for One Hot Encoding. Derivations of State Machine Charges.

UNIT V

Realization of State Machine Charts with a PAL. Alternative Realization for State Machine Chart using Microprogramming. Linked State Machines. One – Hot State Machine, Petrinetes for State Machines – Basic Concepts, Properties. Extended Petrinetes for Parallel Controllers. Finite State Machine – Case Study, Meta Stability, Synchronization.

UNIT VI& VII

FSM ARCHITECTURES AND SYSTEMS LEVEL DESIGN: Architectures Centered Around Non-Registered PLDs. State Machine Designs Centered Around Shift Registers. One – Hot Design Method. Use of ASMs in One – Hot Design. K Application of One – Hot Method. System Level Design – Controller, Data Path and Functional Partition.

UNIT VIII

DIGITAL FRONT END DIGITAL DESIGN TOOLS FOR FPGAS & ASICS: Using Mentor Graphics EDA Tool ("FPGA Advantage") – Design Flow Using FPGAs – Guidelines and Case Studies of Paraller Adder Cell, Paraller Adder Sequential Circuits, Counters, Multiplexers, Parallel Controllers.

TEXT BOOKS/REFERENCS:

1. P.K.Chan & S. Mourad, Digital Design Using Field Programmable Gate Array, jPrentice Hall (Pte), 1994.
2. S.Trimberger, Edr., Field Programmable Gate Array Technology, Kluwer Academic Publicatgions,1994.
3. J. Old Field, R.Dorf, Field Programmable Gate Arrays, John Wiley & Sons, Newyork, 1995.
4. S.Brown, R.Francis, J.Rose, Z.Vransic, Field Programmable Gate Array, Kluwer Pubin, 1992.

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY ANANTAPUR

M.Tech.(DSCE)

II SEMESTER

SIGNAL PROCESSING & MICROPROCESSORS LAB

1. Design and Simulation FIR Filter Using any Windowing Technique.
2. Design of IIR Filters from Analog Filters.
3. Cancellation of Channel Effects using Adaptive Filter (using LMS / RLS Algorithms).
4. Simulation of AR Parameters using Burg's Algorithm for Prediction of Filter Coefficients.
5. Interface a Seven Segment LED to a Decimal Data source refer DIGITAL SYSTEM DESIGN AND MICROPROCESSOR by Hayes Tata McGraw Hill.
6. Interface A/D and D/A, and reconstruct the sampled Signal.
7. Use Interrupt and Sample the Sinusoidal.
8. Interface keyboard and write a Routine to Read a Key from the Keyboard.