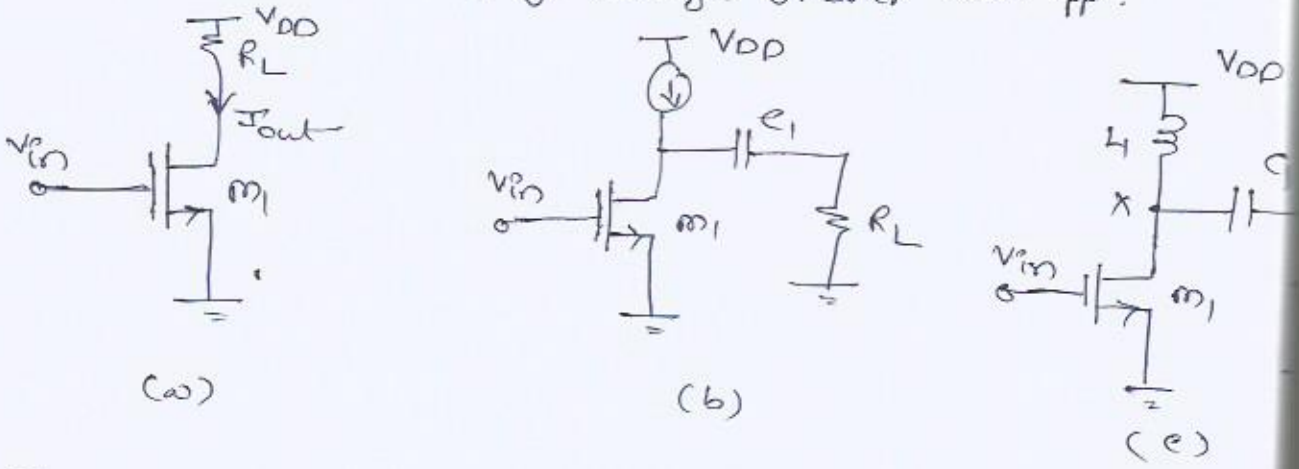
Power Amplifiers

The basic building block of RF transceivers a
Power Amplifiers.

General Considerations:- for a common source stage to
drive the load directly, the configurations are shown
below with a supply voltage greater than V_{pp}.



(a) (b) (c)

fig: CS stages with a) resistive b) current source c) inductive

- Suppose if the load is realized as an inductor the drain ac voltage exceeds V_{DD}, even reaching $2V_{DD}$ (or higher).
- while allowing a lower supply voltage, the inductive lo does not relax the "stress" on the transistor, the maxm drain-source voltage experienced by M_1 is still at least 2ov (1ov above V_{DD} = 1ov) if the stage must d 1W to a 50Ω load.
- The fundamental issue occurred while designing a PA is merely trade-off b/n the O/P power and the volt

b/n the PA and the load as shown below.

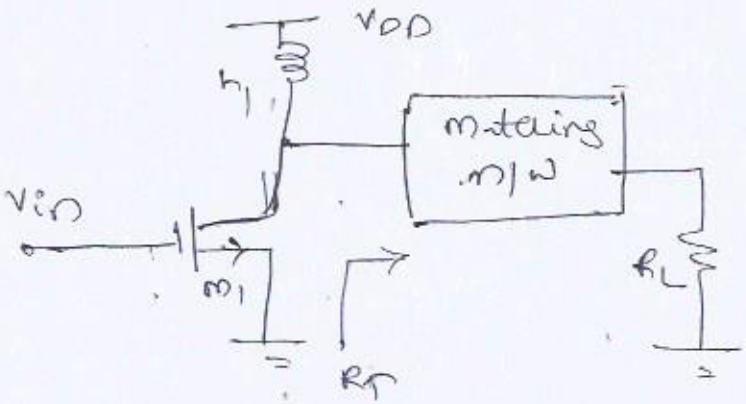


fig: Impedance transformation by a matching n/w.

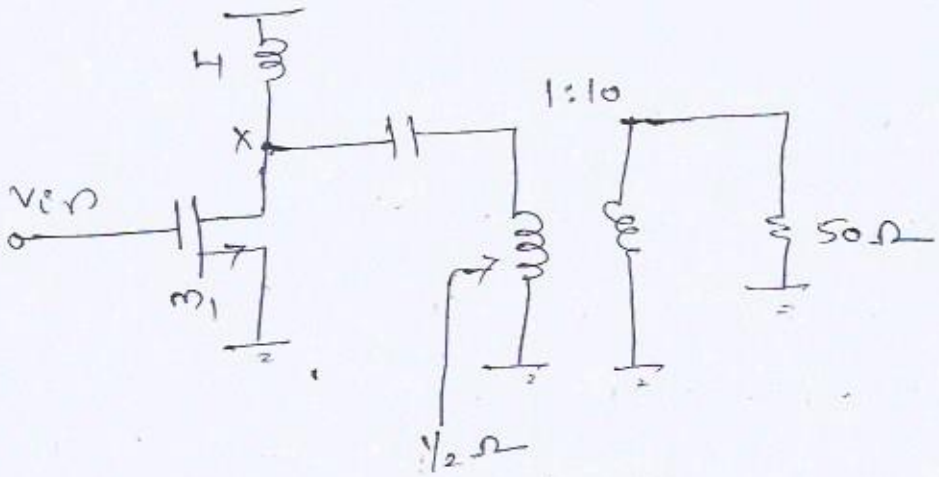


fig: Realization by a transformer.

This n/w transforms the load resistance to a lower value, R_T so that smaller voltage swings still deliver the required Power.

- Need for transforming the voltage swings means that the current generated by the o/p transistor must be proportionally higher.

Classification of Power Amplifiers:-

- Power Amplifiers are classified as class A, B, C, D, E, f etc
- In Power Amplifiers both the i/p and the o/p waveforms are considered sinusoidal.

→ Class A Power Amplifiers:-

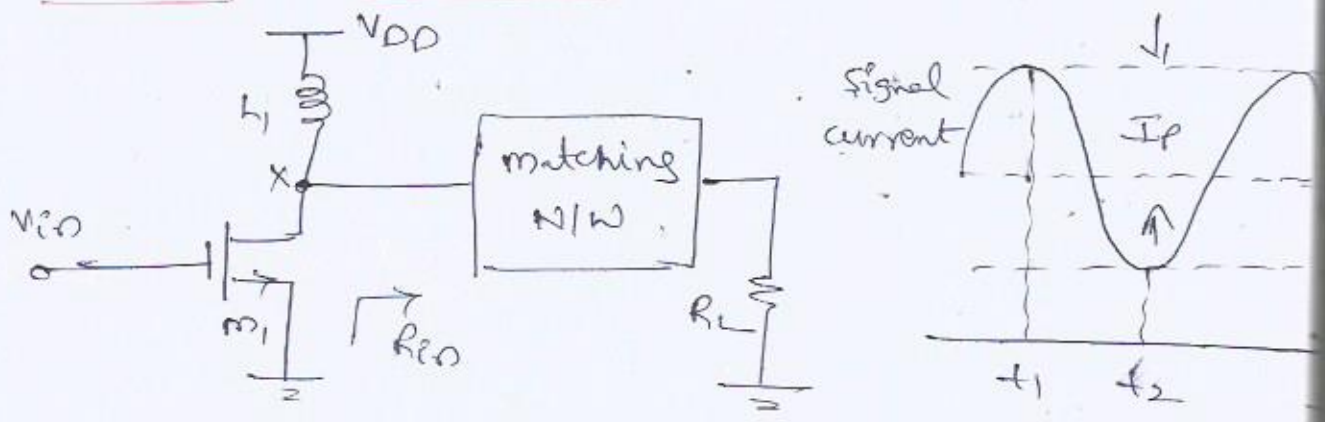


fig: class A stage

- Class A Amplifiers are defined as circuits in which the transistor(s) remain on and operate linearly across the full i/p and o/p range.
- Transistor bias current is chosen higher than the peak signal current I_p, to ensure that the device does not turn off at any point during the signal excursion.
- From the fig the transistor is always ON does not necessarily imply that the PA is sufficiently linear the transconductance varies considerably from t_1 to t_2 while the definition of class A seems to hold.
- If linearity is required, then class A operation necessary.
- In order to calculate the max drain efficiency of class A Amplifier we allow V_x to reach $2V_{DD}$ and nearly zero.
- Power delivered to the matching n/w is approximately equal to $\left(\frac{2V_{DD}}{2}\right)^2 / (2R_{in}) = \frac{V_{DD}^2}{2R_{in}}$, which is also

- for example if the inductive load carries a constant current of $\frac{V_{DD}}{R_{in}}$ from the supply voltage, Thus,

$$\eta = \frac{\frac{V_{DD}^2}{2R_{in}}}{\frac{V_{DD}^2}{R_{in}}} = 50\%.$$

The other 50% of the supply power is dissipated by M_1 itself.

- It is important to recognize the assumptions leading to an efficiency of 50% in class A stages.

1) the drain (collector) peak to peak voltage swing is equal to twice the supply voltage i.e the transistor can withstand a drain-source (or collector-emitter) voltage of $2V_{DD}$ with no reliability or breakdown issues.

2) The transistor barely turns off i.e the nonlinearity resulting from the very large change in the transconductance of the device is tolerable.

3) The matching n/w interposed b/n the o/p transistor and the antenna, is lossless.

→ Class B Power Amplifiers :-

- class B Power Amplifier employs two parallel stages, each of which conducts for only 180°, thereby achieving an higher efficiency than the class A.

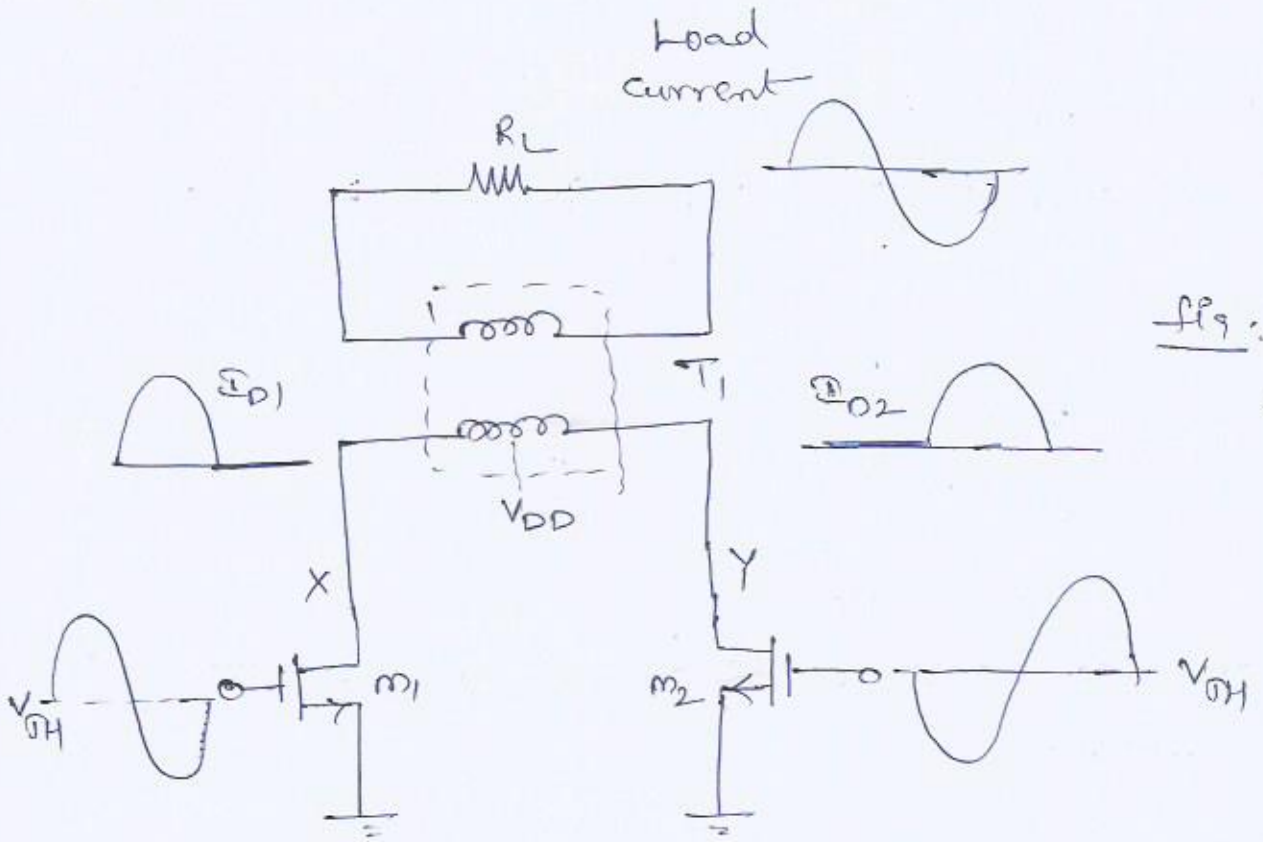
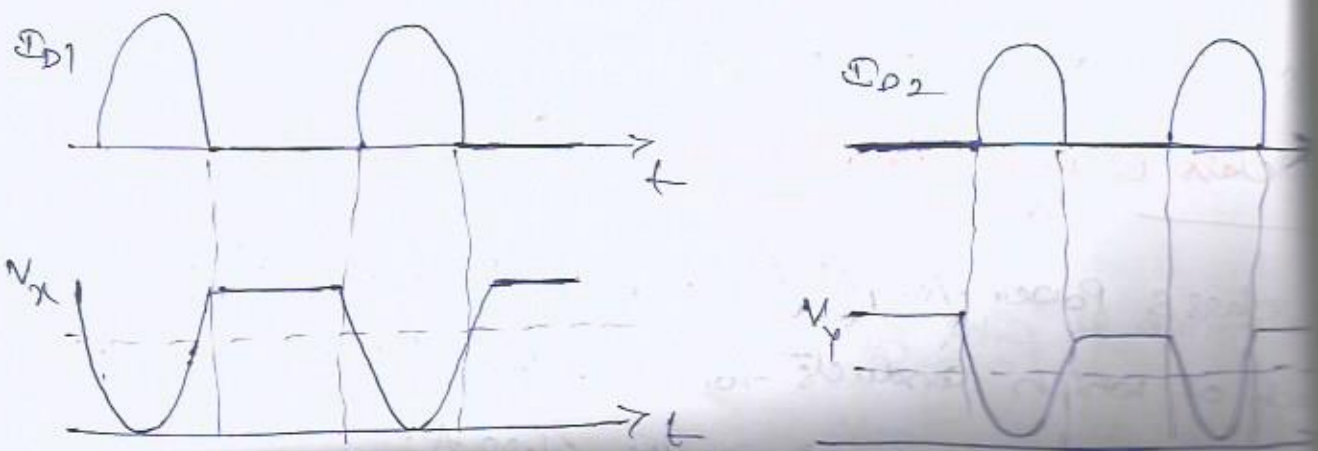


fig: cla
stag

- But class B operation requires that each transis
turn off for half of the period (i.e conduction angle
180°)
- The gate bias voltage of the devices is therefore chos
approximately equal to their threshold voltage.
- If the parasitic capacitances are small and the prim
and secondary inductances are large then V_x and V_y
also half-wave rectified sinusoids that swing ar
V_{DD} are shown below



- when V_{DD} is approximately half that below V_{DD}, an undesirable situation occurs because it results in a low efficiency. for this reason, the secondary of the transformer is tuned by a parallel capacitance so as to suppress the harmonics of the half-wave rectified at X and Y, allowing equal swings above and below V_{DD}.

Class B Power Amplifiers:

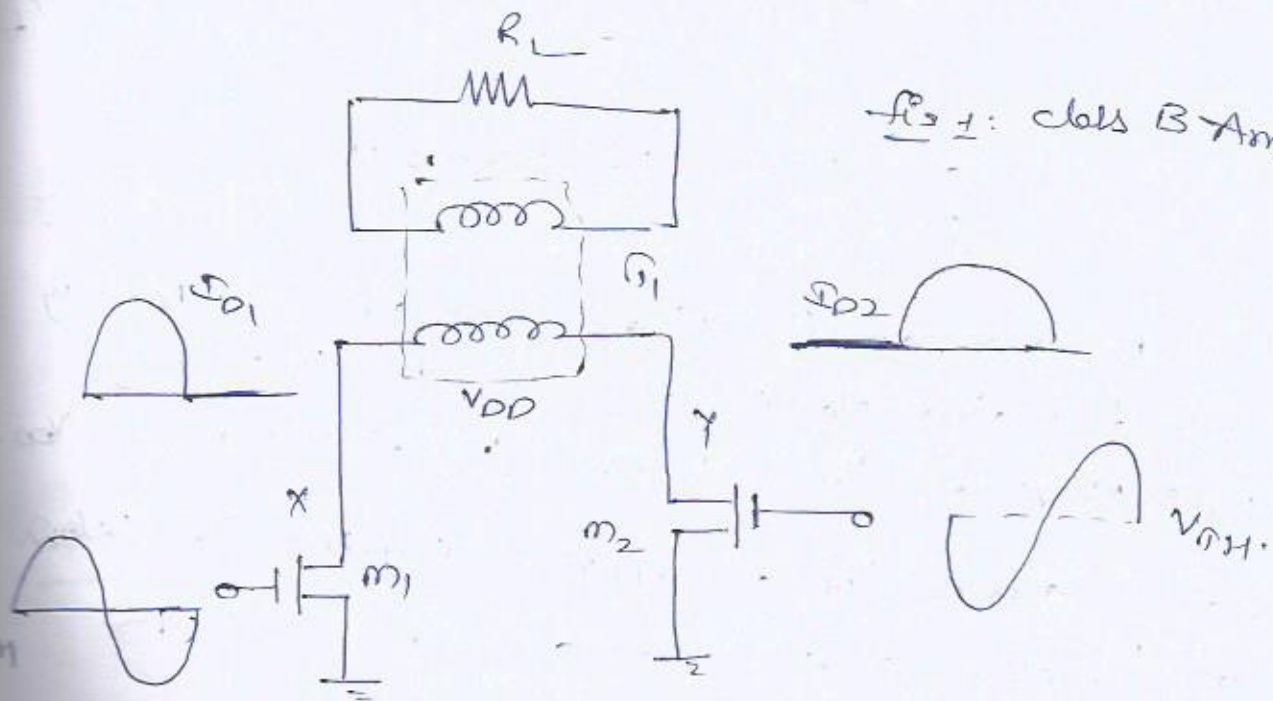


fig 1: class B Amplifier

class B Power Amplifier employs two parallel stages each of which conducts for only 180°, thereby achieving a higher efficiency than the class A.

- As shown in above fig drain currents of M_1 and M_2 are combined by transformer T_1.
- The above ckt works in a quasi differential stage and a balun driving the single ended load.
- class B operation requires that each transistor

to their threshold voltage.

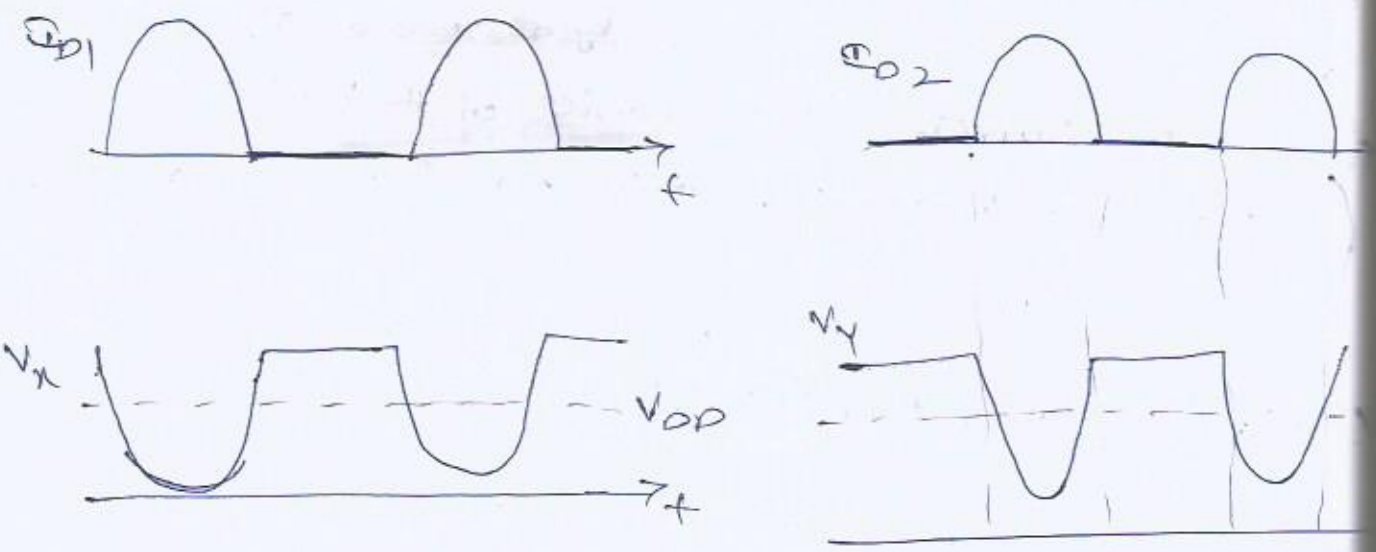


fig 2: Current and voltage waveforms in a class B stage.

- When parasitic capacitances are small and the primary and secondary inductances are large then v_x and v_y are half-wave rectified sinusoids that swing around V_{DD}.
- The swing above V_{DD} is approximately half that below V_{DD}, an undesirable situation occurs leads to low efficiency.
- For this reason, the secondary (or primary) of the transformer is tuned by a parallel capacitance so as to suppress the harmonics of the half wave rectified sinusoids at x and Y, allowing equal swings above and below V_{DD}.
- The efficiency of class B Power Amplifier is equal to $\eta = \frac{\pi}{4} \approx 78\%$

→ **Class AB Power Amplifiers:** The term "class AB is sometimes used to refer to a single ended Power Amplifier whose conduction angle falls between 180° and 360° i.e in which the o/p transistor turns off for less than half of a Period. From another perspective, a class AB Power Amplifier is less linear than class A stage and more linear than a class B stage. This is usally accomplished by reducing the i/p voltage swing and hence backing off from the 1 db compression point.

→ **Class C Power Amplifiers :-**

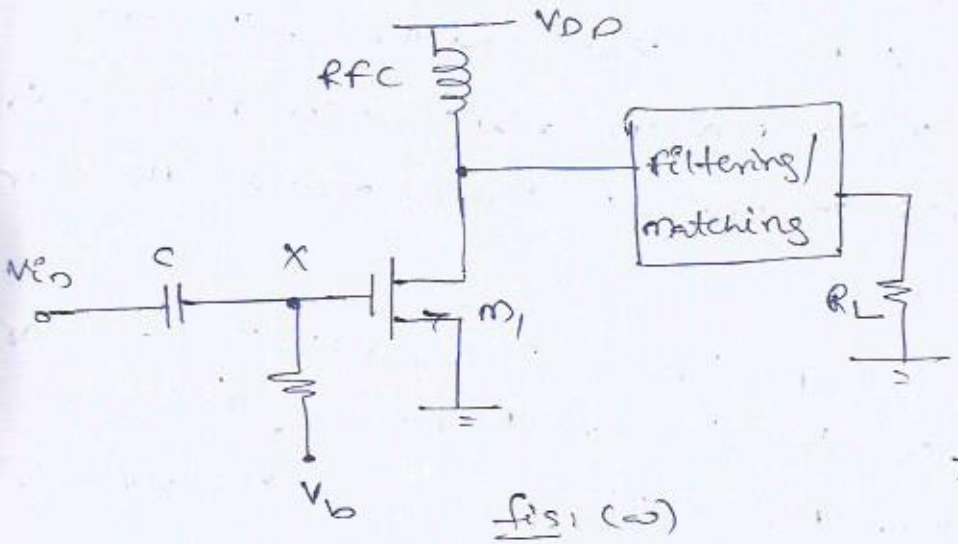
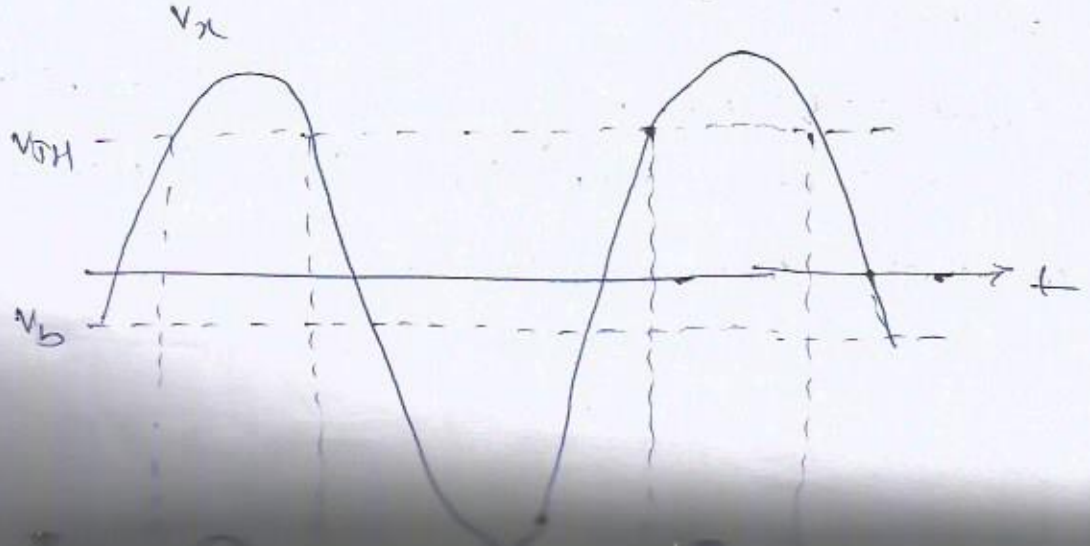


fig: (a)

fig: a) class C stage

b) I/O waveforms



- In class A and class B amplifiers, smaller conduction angle yields a higher efficiency.
- In class C stage this angle is reduced further (and the ckt becomes more nonlinear).
- Class C Power Amplifier ckt is biased such that it turns ON if the peak value of V_{in} raises V_X above V_{TH}.
- V_X exceeds V_{TH} for only a fraction of the Period if M_1 were stimulated by a narrow pulse. As a result the transistor delivers a narrow pulse of current to the o/p every cycle.
- In order to avoid large harmonic levels at the output the matching n/w must Provide some filtering. In fact the i/p impedance of the matching n/w is also designed to resonate at the freq of interest, there by making the output voltage a sinusoid.
- In class C Power Amplifier as θ decreases, the transistor is ON for a smaller fraction of the Period, thus dissipating less Power. For the same reason, however the transistor delivers less Power to the load.
- As θ approaches to zero a maximum efficiency of 100% occurs in class C Power amplifier this is the Prominent feature of class C Power amplifier.

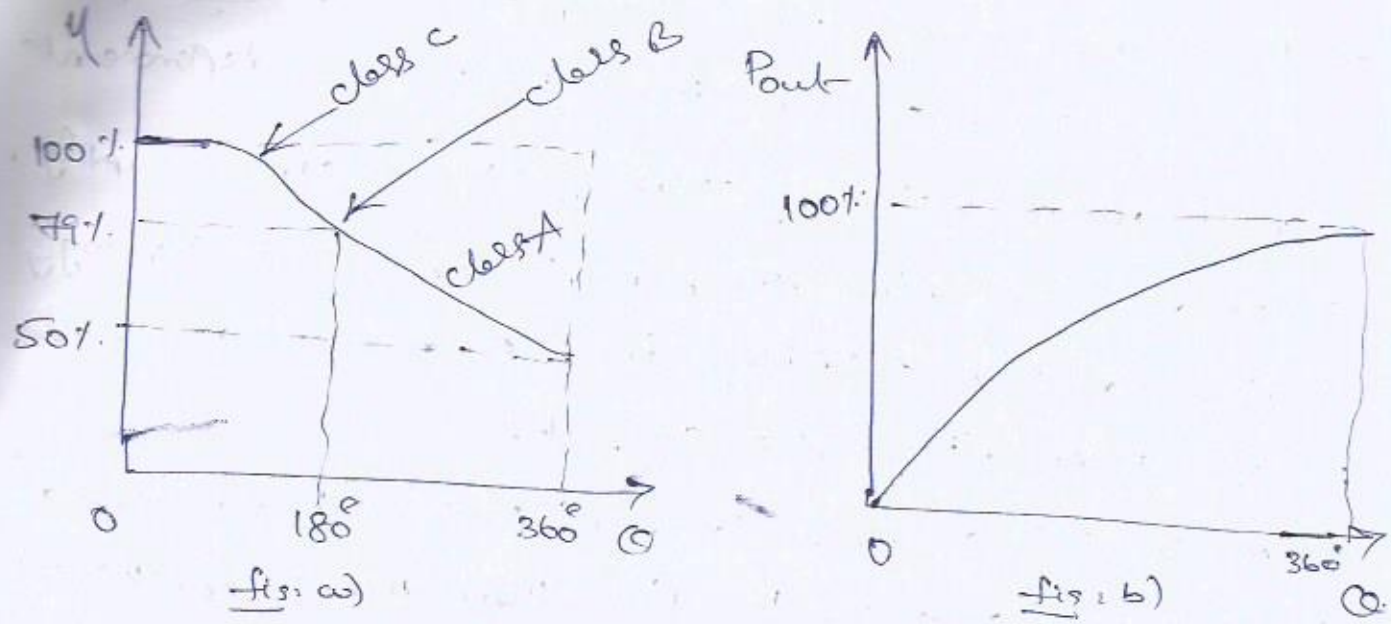


fig: a) b)

fig: a) Efficiency b) o/p Power as a function of conduction angle

- from above waveforms it is shown that Pout falls to zero as θ approaches zero.

- In other words we can say that class C stage provides a high efficiency only if it delivers a fraction of the peak o/p power (the power corresponding to full class A operation).

→ class E stage:

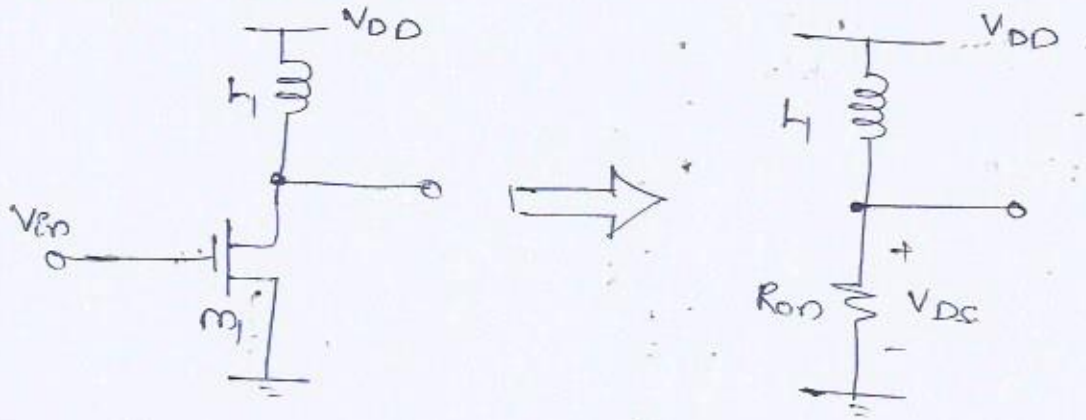


fig: o/p stage with switching transistor.

- class E stage are nonlinear amplifiers that achieve

- As shown above when the o/p transistor ckt operates as a switch, rather than a voltage dependent current source, ideally turning ON and off abruptly called as "switching Power amplifier" such a topology achieves a high efficiency if 1) M_1 sustains a small voltage when it carries current.

2) M_1 carries a small current when it sustains a finite voltage and 3) the transition times b/n the on and off states are minimized.

- from (1) and (3) we conclude that the ON-resistance of the switch must be very small and the voltage applied to the gate of M_1 must approximate a rectangular waveform.

- However, even with these two conditions (2) may still be violated if M_1 turns ON when V_X is high.

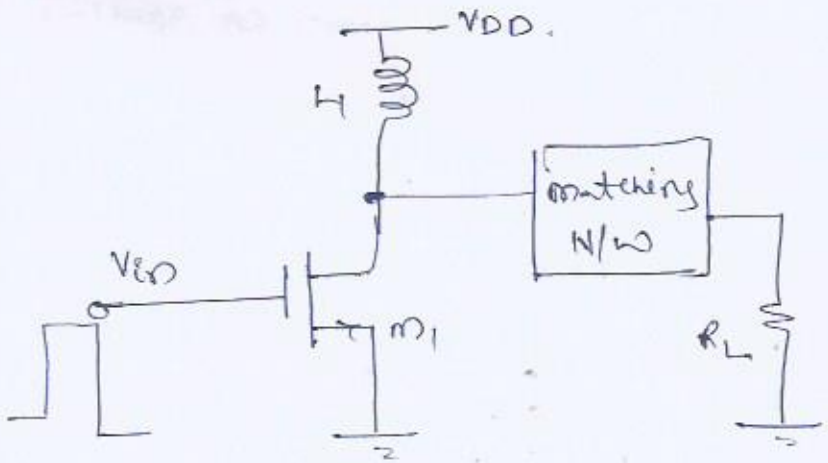
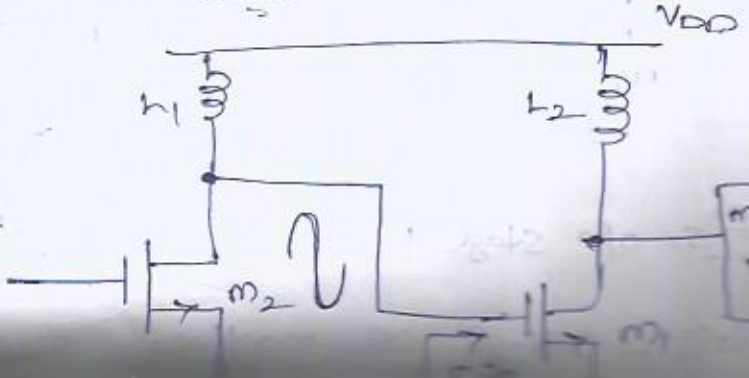


fig: (a)



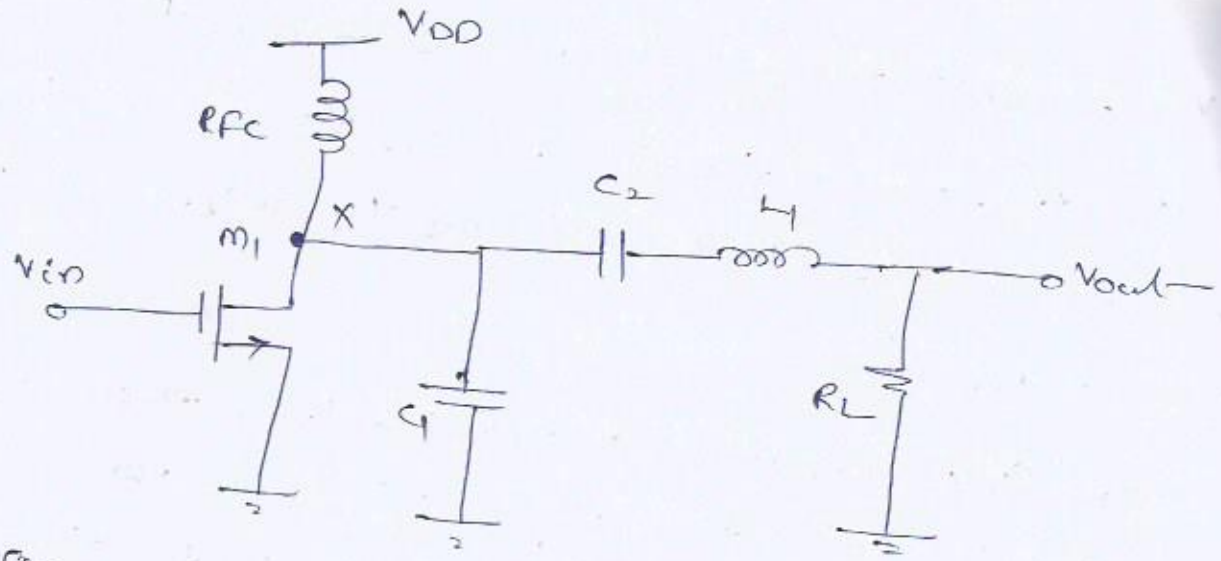


fig: class E stage.

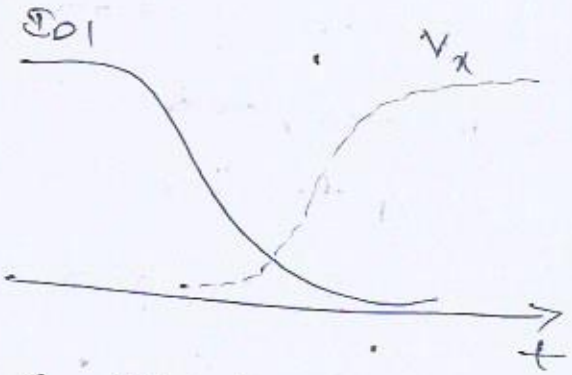
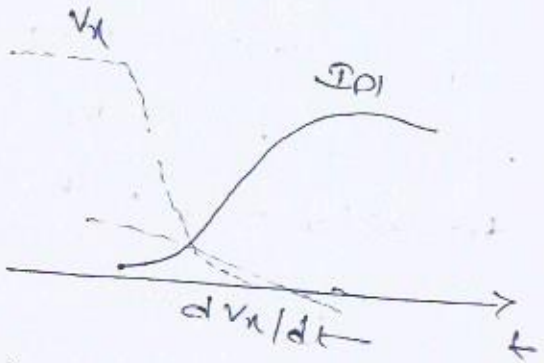


fig: Condition to ensure minimal overlap b/n drain current and voltage



c) condition to ensure low sensitivity to timing errors.

- class E amplifiers deal with the finite i/p and o/p transition times by proper load design
- class E stage consists of an o/p transistor, M_1, a grounded capacitor C_1 and a series n/w C_2 and L_1.
- C_1 includes the junction capacitance of M_1 and the parasitic capacitance of the RFC.
- The values of C_1, C_2, L_1 and R_L are chosen such that it satisfies three conditions

2) V_x reaches zero just before the switch turns ON

3) dV_x/dt is also near zero when the switch turns ON. We examine these conditions to understand the circuits properties

The first condition, guaranteed by C_1, resolves the issue of finite fall time at the gate of M_1. Without C_1, V_x would rise as V_{in} dropped, allowing M_1 to dissipate substantial power.

The second condition ensures that the V_{DS} and I_D of the switching device do not overlap in the vicinity of the turn-on point, thus minimizing the power dissipation in the transistor even with finite i/p and o/p transition times.

The third condition lowers the sensitivity of the efficiency to violations of the second condition. That is, if device or supply variations introduce some overlap in the voltage and current waveforms, the efficiency degrades only slightly because $dV_x/dt = 0$ means V_x does not change significantly near the turn-off point.

→ Class f Power Amplifiers :-

- When the load n/w provides a high termination impedance at the second or third harmonics, the voltage waveform across the switch exhibits sharper edges than a sinusoid, thereby reducing the power loss in the transistor. Such a ckt is called class f amp.

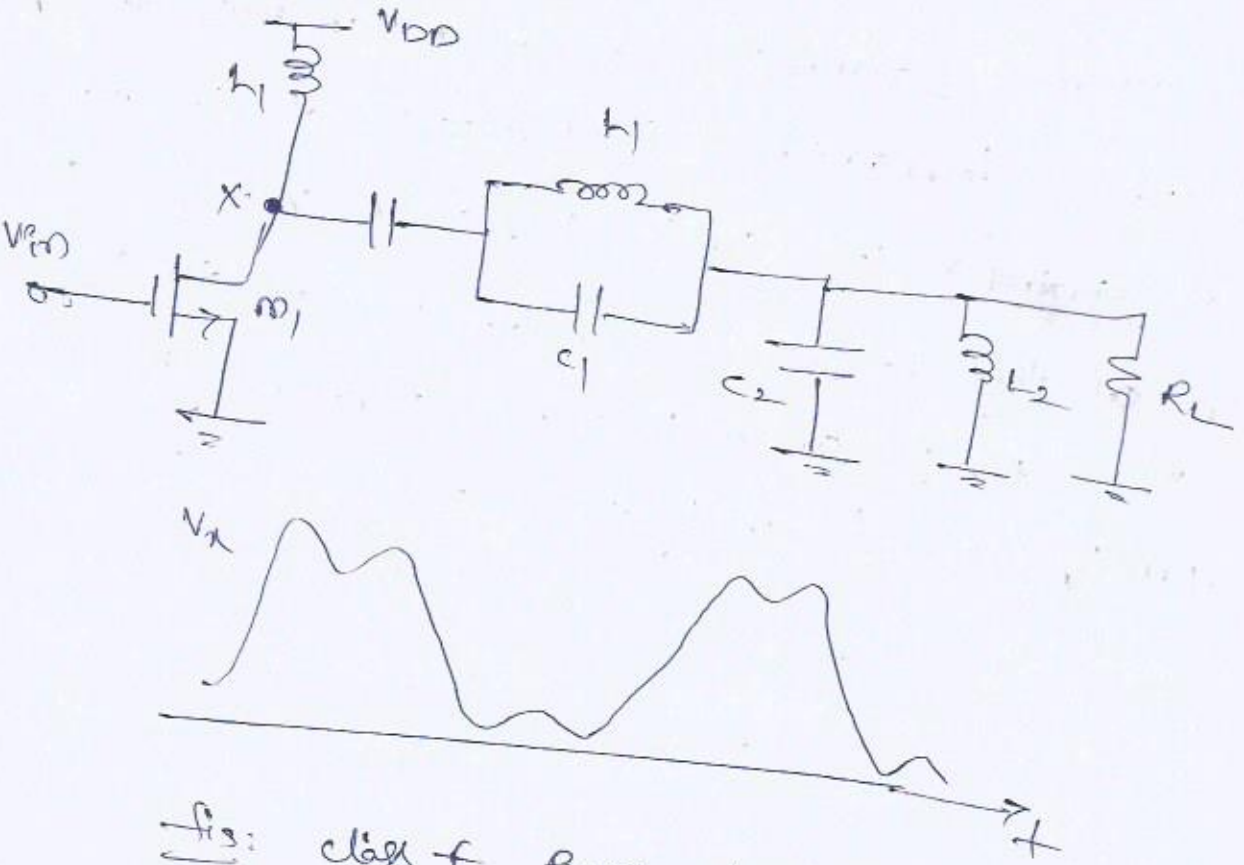


fig: class f Power Amplifier

As shown in above fig the third-harmonic peaking is visible only if the o/p transistor experiences "hard" switching i.e its o/p current resembles a rectangular wave. This in turn requires that the gate (or base) voltage be driven by relatively sharp edges.

If the drain current of the transistor is assumed to be a half-wave rectified sinusoid, it can be proved that the peak efficiency of class f amplifiers is equal to 88% for third harmonic peaking.

→ Voltage controlled oscillators:-

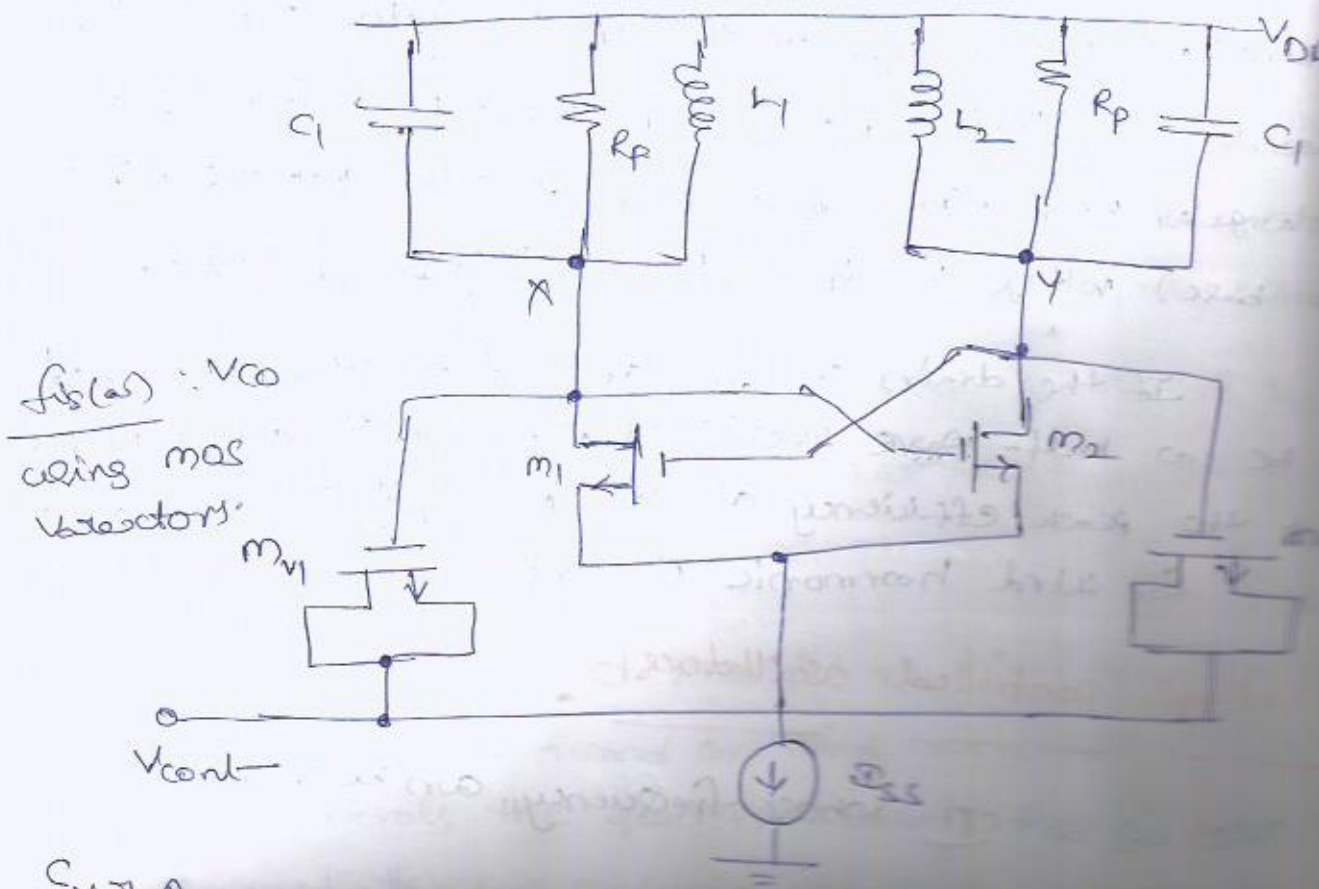
- VCO is an ckt whose frequency can be varied electronically.

Watt

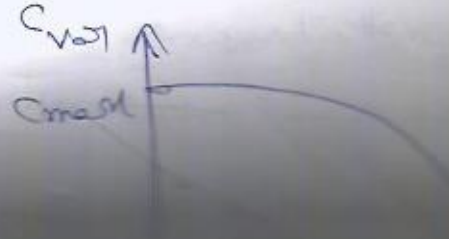
– The above fig shows the behavior of VCO where the o/p freq varies from ω_1 to ω_2 (the required tuning range) as the control voltage V_{cont} goes from V_1 to V_2. The slope of the characteristic, K_{VCO} is called the "gain" or "sensitivity" of the VCO and expressed in rad/Hz/V. We formulate this characteristic as

$$\omega_{out} = K_{VCO} V_{cont} + \omega_0.$$

where ω_0 denotes the intercept point on the vertical axis. It is desirable that this characteristic be relatively linear i.e K_{VCO} not change significantly across the tuning range.



fig(a): VCO using MOS Varactors.



- In order to vary the freq of an LC oscillator, the resonance freq of its tank must be varied.
- Since it is difficult to vary the inductance electronically, we only vary the capacitance by means of a varactor.
- MOS varactors are more commonly used than PN junctions, especially in low-voltage design.
- As shown in above fig varactors M_{V1} and M_{V2} appear in parallel with the tanks (if V_{cont} is provided by an ideal voltage source).
- Note that the gates of the varactors are tied to the oscillator nodes and the source/drain/n-well terminals to V_{cont}.
- This avoids loading X and Y with the capacitance b/n the n-well and the substrate.
- Since the gates of M_{V1} and M_{V2} reside at an average level equal to V_{DD}, their gate-source voltage remains +ve and their capacitance ↓'s as V_{cont} goes from zero to V_{DD}.
- This behavior persists even in the presence of large voltage swings at X and Y and hence across M_{V1} and M_{V2}.
- The key point here is that the average voltage across each varactor varies from V_{DD} to zero as V_{cont} goes from zero to V_{DD}, thus creating a monotonic decrease in their capacitance. The oscillation freq can thus be expressed as

→ Phase Locked Loops (PLL) :-

- To achieve high frequency accuracy most of the synthesizers employ "phase-locking".
- PLL is a negative feedback loop consisting of a VCO and a "phase detector".

Phase detector :-

- A phase detector is a circuit that senses two periodic i/p's and produces an o/p whose average value is proportional to the difference between the phases of the inputs.

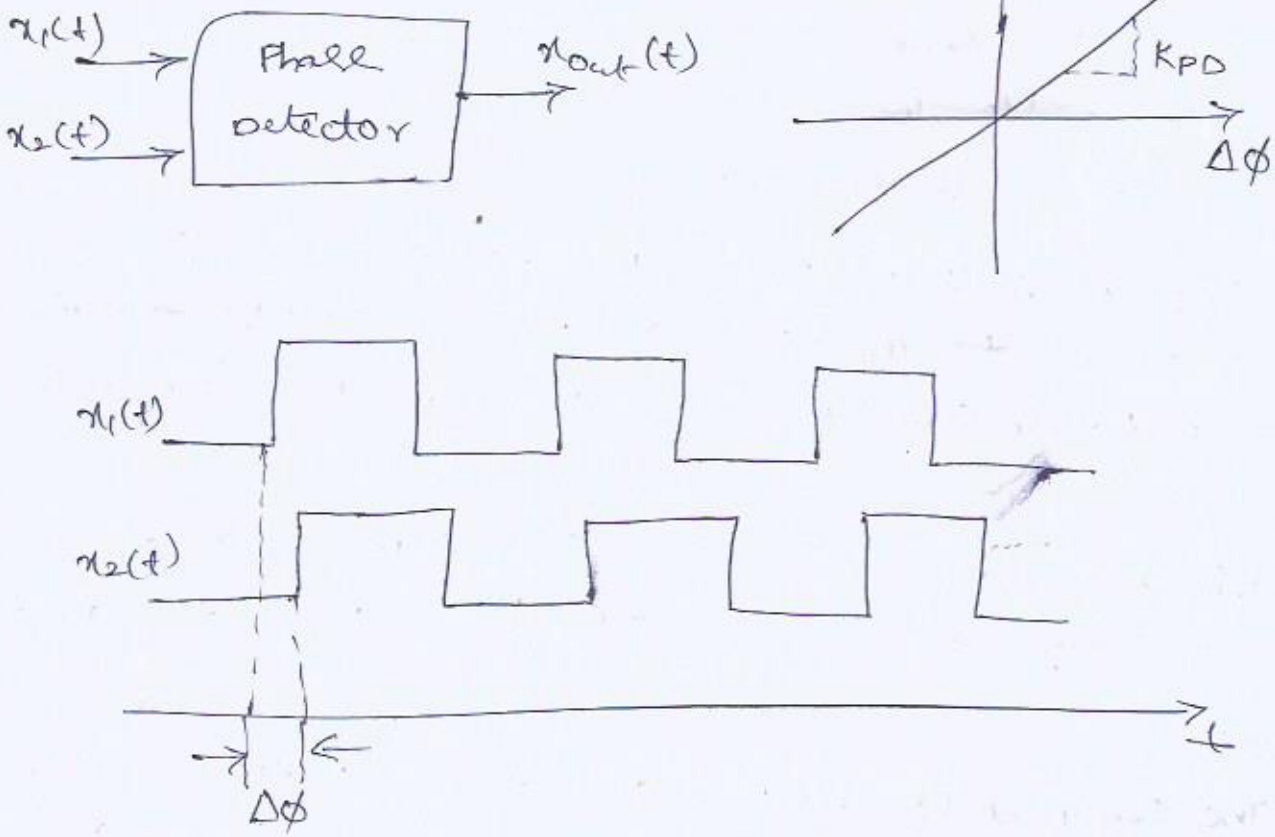
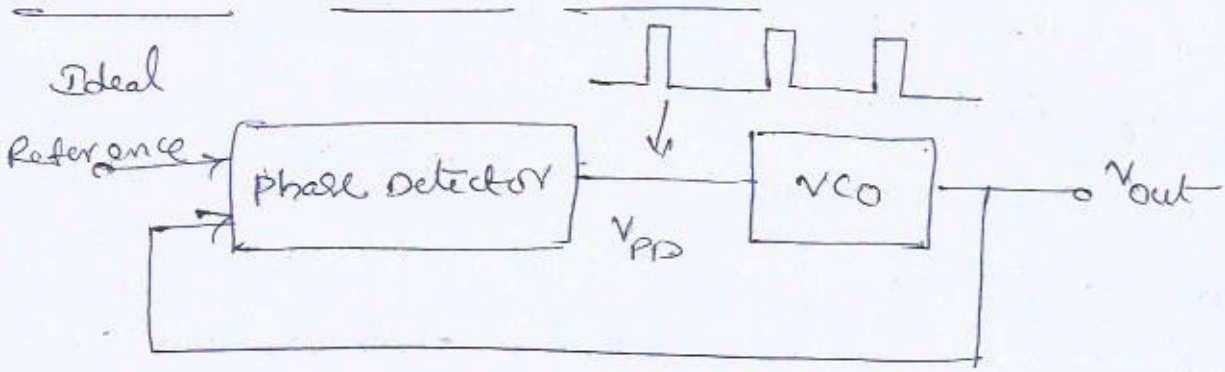


Fig: Phase detector and its input/output characteristic

- The input-/output characteristic of the phase detector is ideally a straight line, with a slope called the

Voltage Controlled oscillator (VCO) :-



fig(1:) Simple PLL.

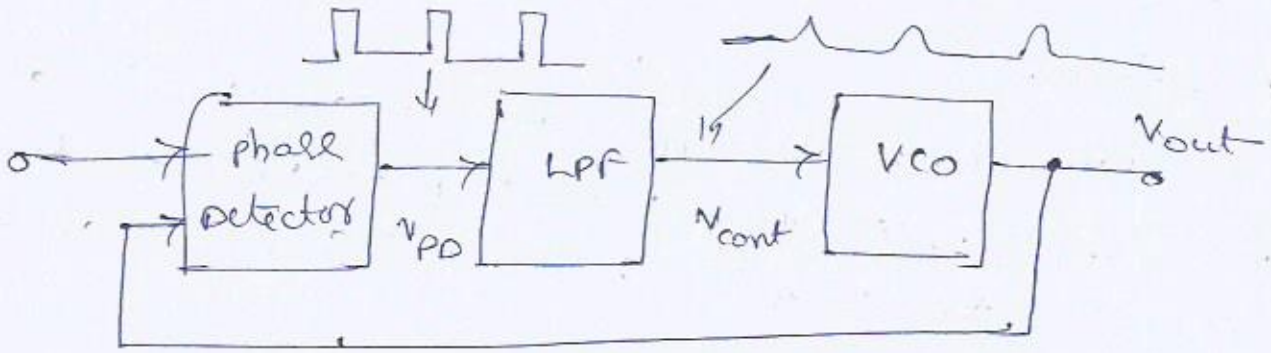


fig (2) Addition of low pass filter to remove high frequency components generated by Phase detector.

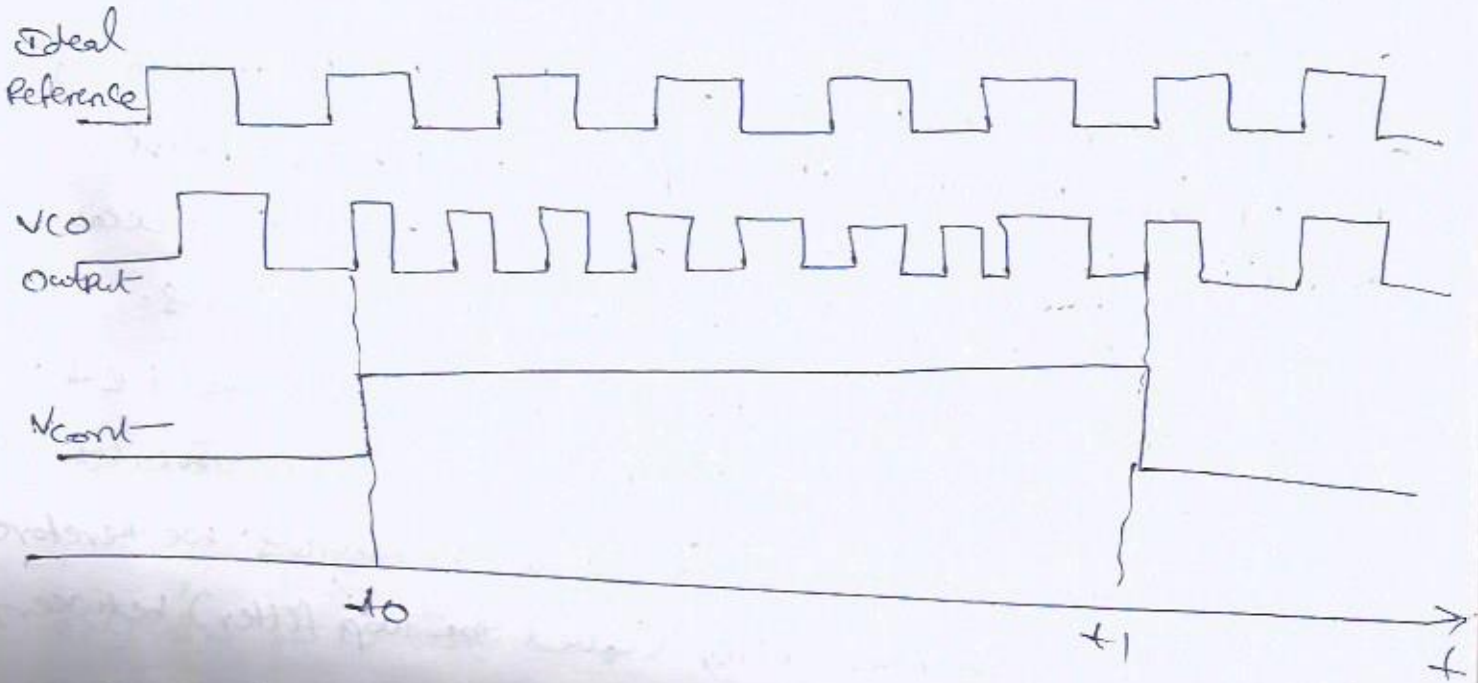


fig: Alignment of VCO output phase by changing its frequency.

by adjusting the phase of the VCO.

- Control voltage is the only i/p and that the phase does not change instantaneously

- we recognize that we must 1) change the freq of the VCO 2) Allow the VCO to accumulate phase faster (or more slowly than the reference so that the phase error vanishes and 3) change the freq back to its initial value as shown in waveforms.

when Vcont is stepped at $t = t_0$ and remains at the new value until $t = t_1$, when the phase error goes to zero. Thereafter, the two signals have equal frequencies and a zero phase difference.

- In order to determine the time at which the phase reaches zero can be done by comparing the VCO phase and the reference phase can serve this purpose; yielding the -ve feedback loop as shown in fig(1)

- If the loop gain is sufficiently high, the ckt minimizes the i/p error. Note that the loop only "understands" phase quantities. (rather than voltage or current quantities) because the input "subtractor" (the PD) operates with phases.

- The above shown PLL faces a critical issue that i.e the phase detector produces repetitive pulses at its o/p, modulating the VCO frequency and generating large sidebands. we therefore interpose a low pass filter (called the loop filter) between the phase detector and the VCO so as to suppress the HF pulses