UNIT-1

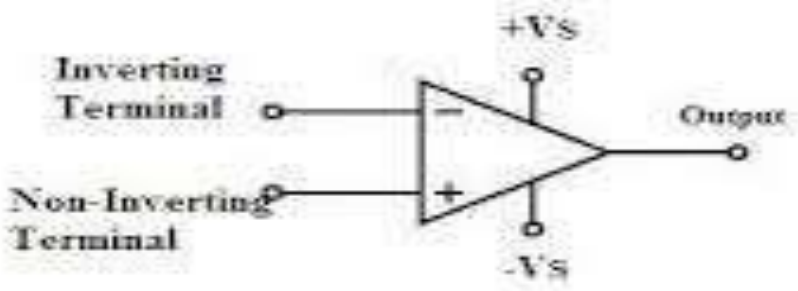
OPAMP CHARACTERISTICS

BASIC INFORMATION OF OP-AMP

- An “Operational amplifier” is a direct coupled high-gain amplifier usually consisting of one or more differential amplifiers and usually followed by a level translator and output stage.
- The operational amplifier is a versatile device that can be used to amplify dc as well as ac input signals and was originally designed for computing such mathematical functions as addition, subtraction, multiplication and integration.

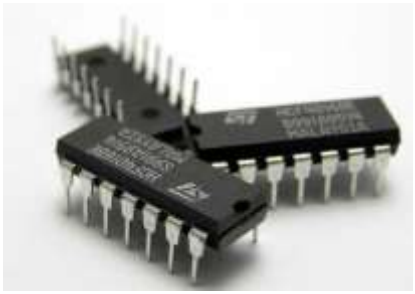
BASIC INFORMATION OF OP-AMP

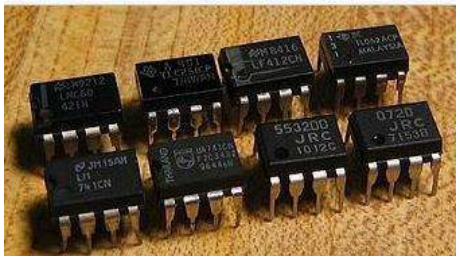
- Op-amps have five basic terminals, that is, two input terminals, one output terminal and two power supply terminals.



PACKAGES

The metal can (TO) Package





The Dual-in-Line (DIP) Package

The Flat Package

Op-amp pin diagram

There are 8 pins in a common Op-Amp, like the 741 which is used in many instructional courses.

Pin 1: Offset null

- Pin 2: Inverting input terminal
- Pin 3: Non-inverting input terminal

Pin 4: –VCC (negative voltage supply)

Pin 5: Offset null

- Pin 6: Output voltage

Pin 7: +VCC (positive voltage supply)

Pin 8: No Connection

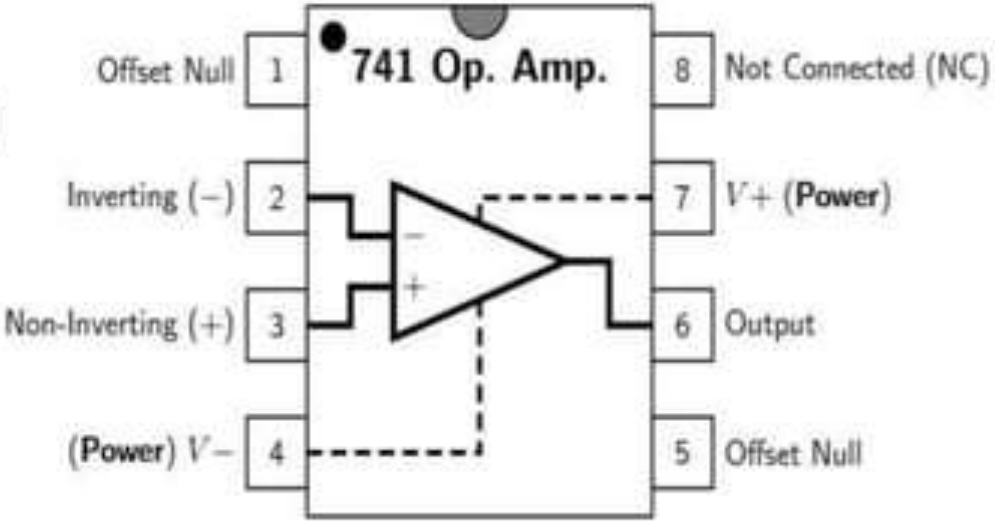
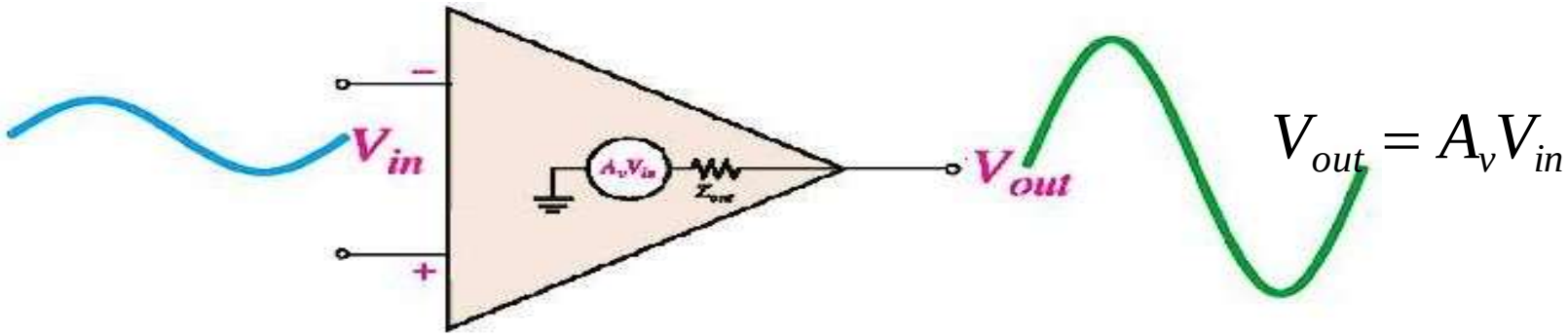


Figure : Pin connection, LM741.

IDEAL OP-AMP

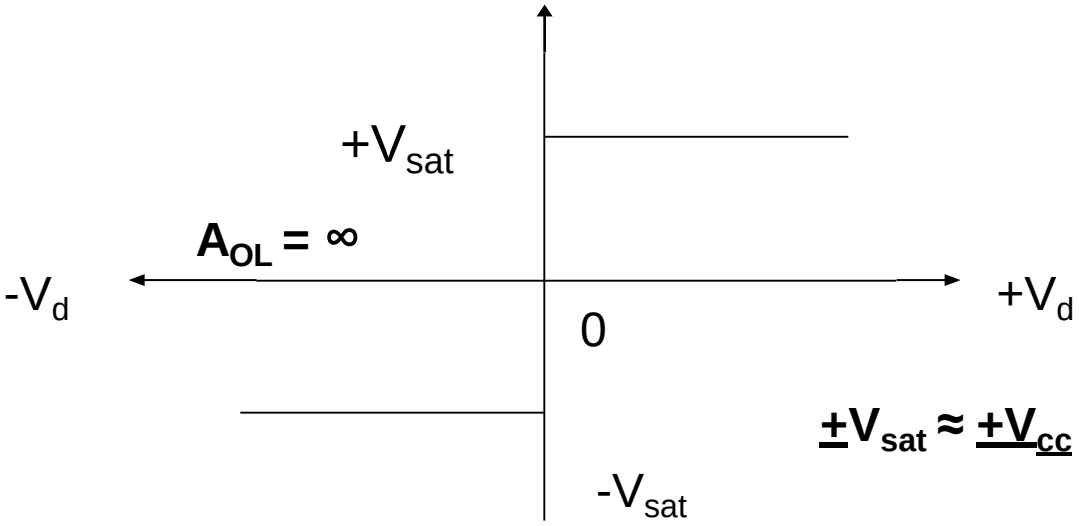


- Infinite Open-Loop Gain
- Open-Loop Gain, A is the gain of the op-amp
- without feedback.
- In the ideal op-amp, A is infinite
- In real op-amp, A is 20k to 200k

IDEAL OP-AMP

- An ideal op-amp draws no current at both the input terminals I.e. $I_1 = I_2 = 0$. Thus its input impedance is infinite. Any source can drive it and there is no loading on the driver stage
- The gain of an ideal op-amp is infinite, hence the differential input $V_d = V_1 - V_2$ is essentially zero for the finite output voltage V_o
- The output voltage V_o is independent of the current drawn from the output terminals. Thus its output impedance is zero and hence output can drive an infinite number of other circuits

IDEAL VOLTAGE TRANSFER CURVE

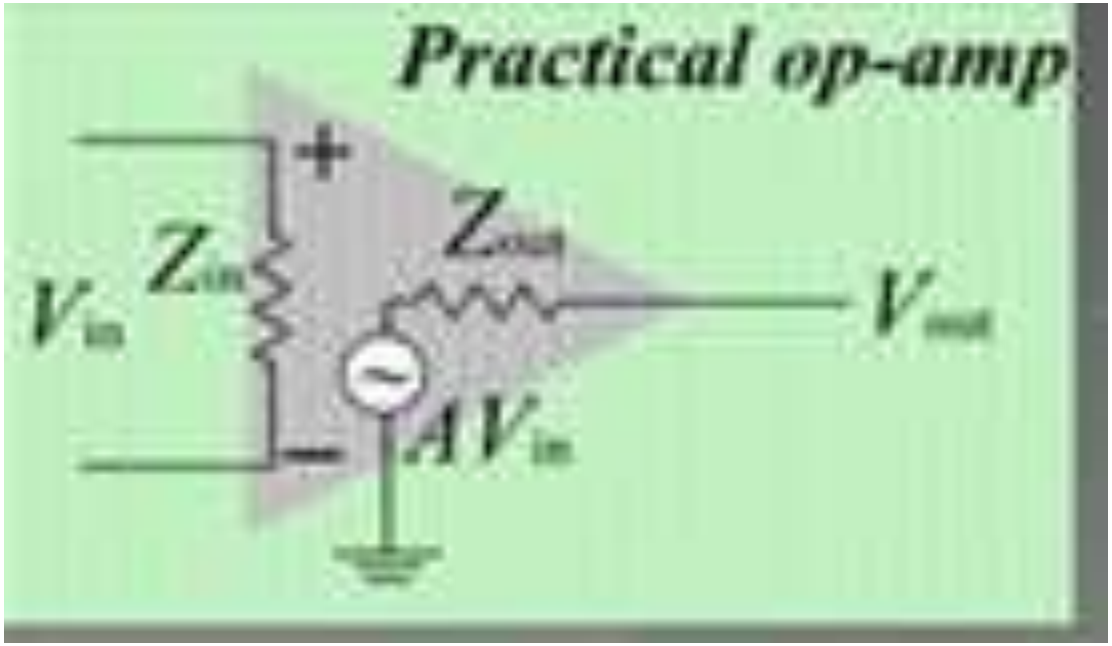


AN IDEAL OP AMP CHARACTERISTICS

An ideal op amp has the following characteristics:

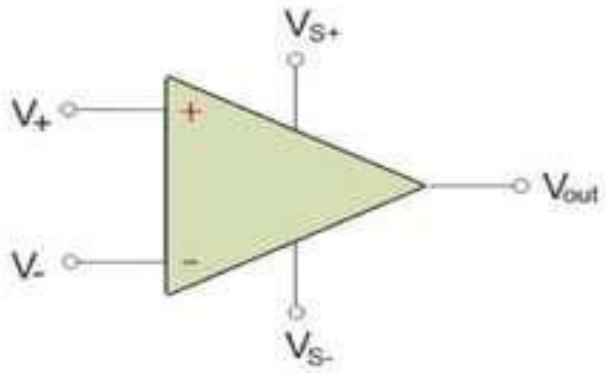
- Infinite open-loop voltage gain, $A_V \approx \infty$.
- Infinite input resistance, $R_i \approx \infty$.
- Zero output resistance, $R_o \approx 0$.
- Infinite CMRR, $\rho = \infty$
- The output voltage Vo=0; when $V_d = V_2 - V_1 = 0$
- Change of output with respect to input, slew rate = ∞
- Change in out put voltage with Temp., $\partial V_o / \partial V_i = 0$

PRACTICAL OP-AMP



PRACTICAL OP-AMP CHARACTERISTICS

Operational amplifier or op amps as they are usually referred are linear devices that can give ideal DC amplification. They are fundamentally voltage amplifying devices used with external feedback components like resistors or capacitors. An **op amp** is a three terminal device, with one terminal called the inverting input, other the non-inverting input and the last one is the output. Below is a diagram of a typical op amp:



V_+ = non-inverting input

V_- = inverting input

V_{out} = output

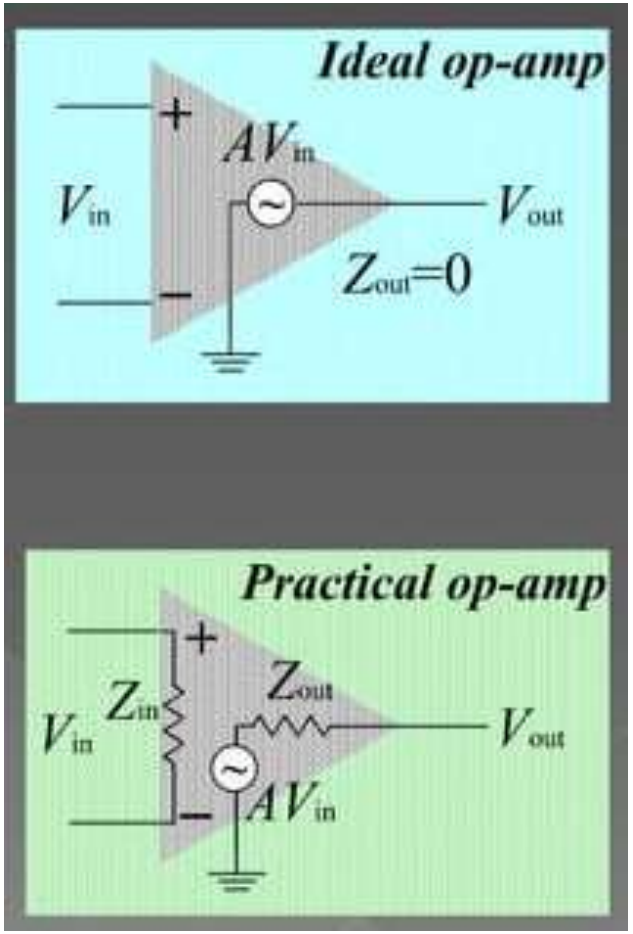
V_{S+} = positive power supply

V_{S-} = negative power supply

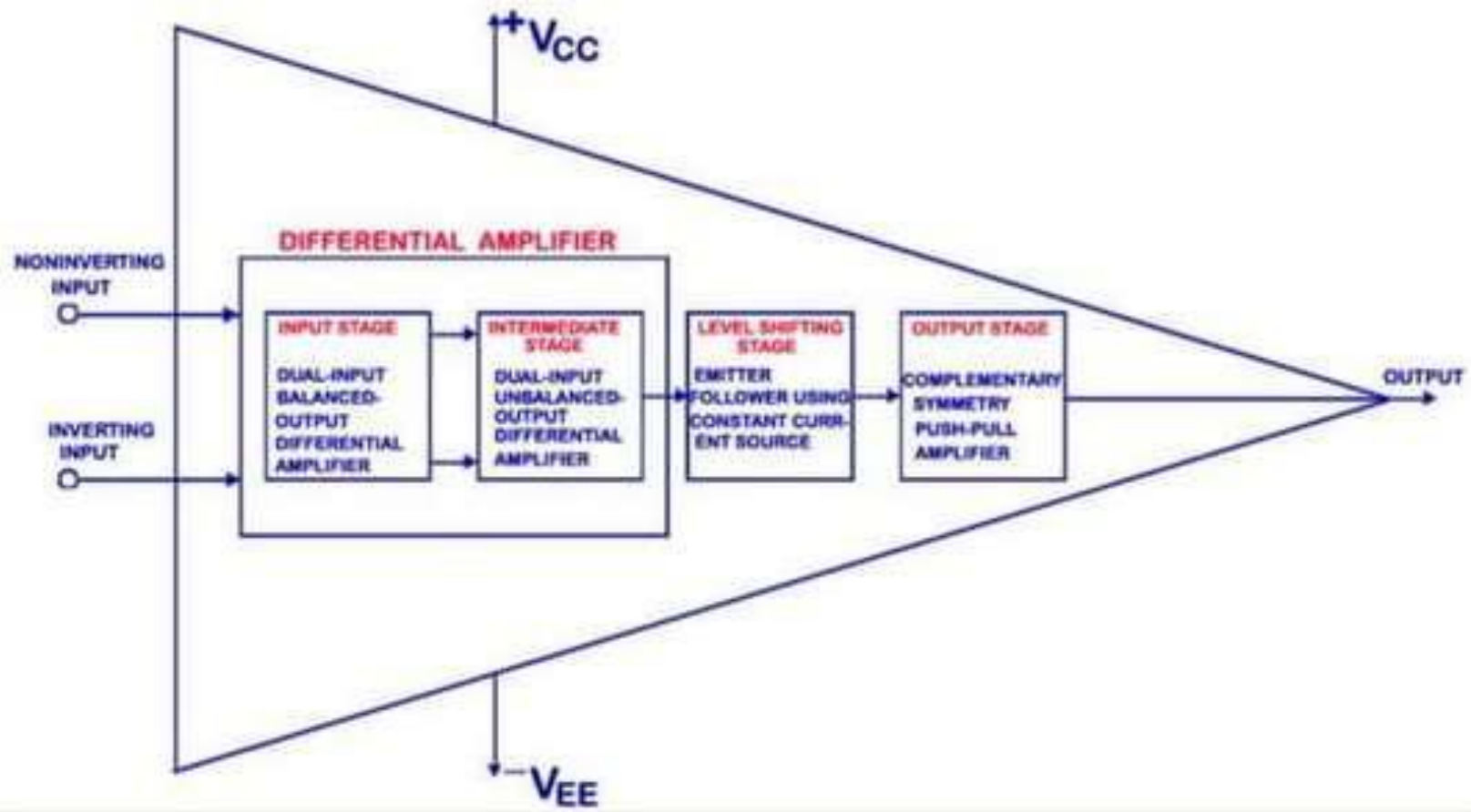
As you can see from the diagram, op amp has three terminals for input and output and 2 for power supply.

IDEAL Vs PRACTICAL OP-AMP

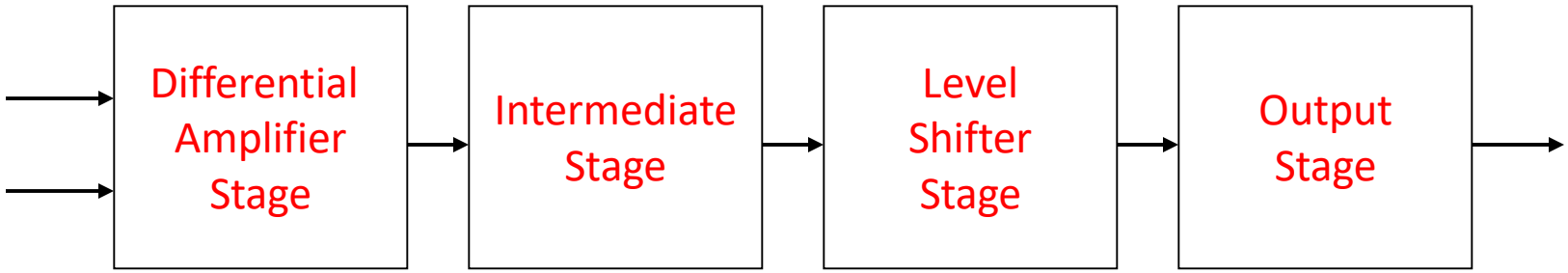
	Ideal	Practical
Open Loop gain *A*	∝	10^5
Bandwidth *BW*	∝	10-100Hz
Input Impedance Z_{in}	∝	>1MΩ
Output Impedance Z_{out}	0 Ω	10-100 Ω
Output Voltage V_{out}	Depends only on $V_d = (V_+ - V_-)$ Differential mode signal	Depends slightly on average input $V_c = (V_+ + V_-)/2$ Common-Mode signal
CMRR	∝	10-100dB



BLOCK DIAGRAM OF OPERATIONAL AMPLIFIER



INTERNAL BLOCK DIAGRAM



- Four stages can be identified –
- Input stage or differential amplifier stage can amplify difference between two input signals; Input resistance is very high; Draws zero current from the input sources

INTERNAL BLOCK DIAGRAM

- Intermediate stage (or stages) use direct coupling; provide very high gain
- Level shifter stage shifts the dc level of output voltage to zero (can be adjusted manually using two additional terminals)
- Output stage is a power amplifier stage; has very small output resistance; so output voltage is the same, no matter what is the value of load resistance connected to the output terminal

DC CHARACTERISTICS OF OP-AMP

- Input bias current
- Input offset current
- Input offset voltage
- Thermal drift

1. Input Offset Voltage

- The differential voltage that must be applied between the two input terminals of an op-amp, to make the output voltage zero.
- It is denoted as **Vios**
- For op-amp 741C the input offset voltage is 6mV

$$V_{io}=V_{dc1}-V_{dc2}$$

2. Input Offset Current

- The algebraic difference between the currents flowing into the two input terminals of the op-amp
- It is denoted as Iios = | Ib1 – Ib2 |
- For op-amp 741C the input offset current is 200nA

3. Input bias current

- The average value of the two currents flowing into the op-amp input terminals
- It is expressed mathematically as

$$\frac{I_{b1} + I_{b2}}{2}$$

- For 741C the maximum value of Ib is 500nA

4. Thermal Voltage Drift

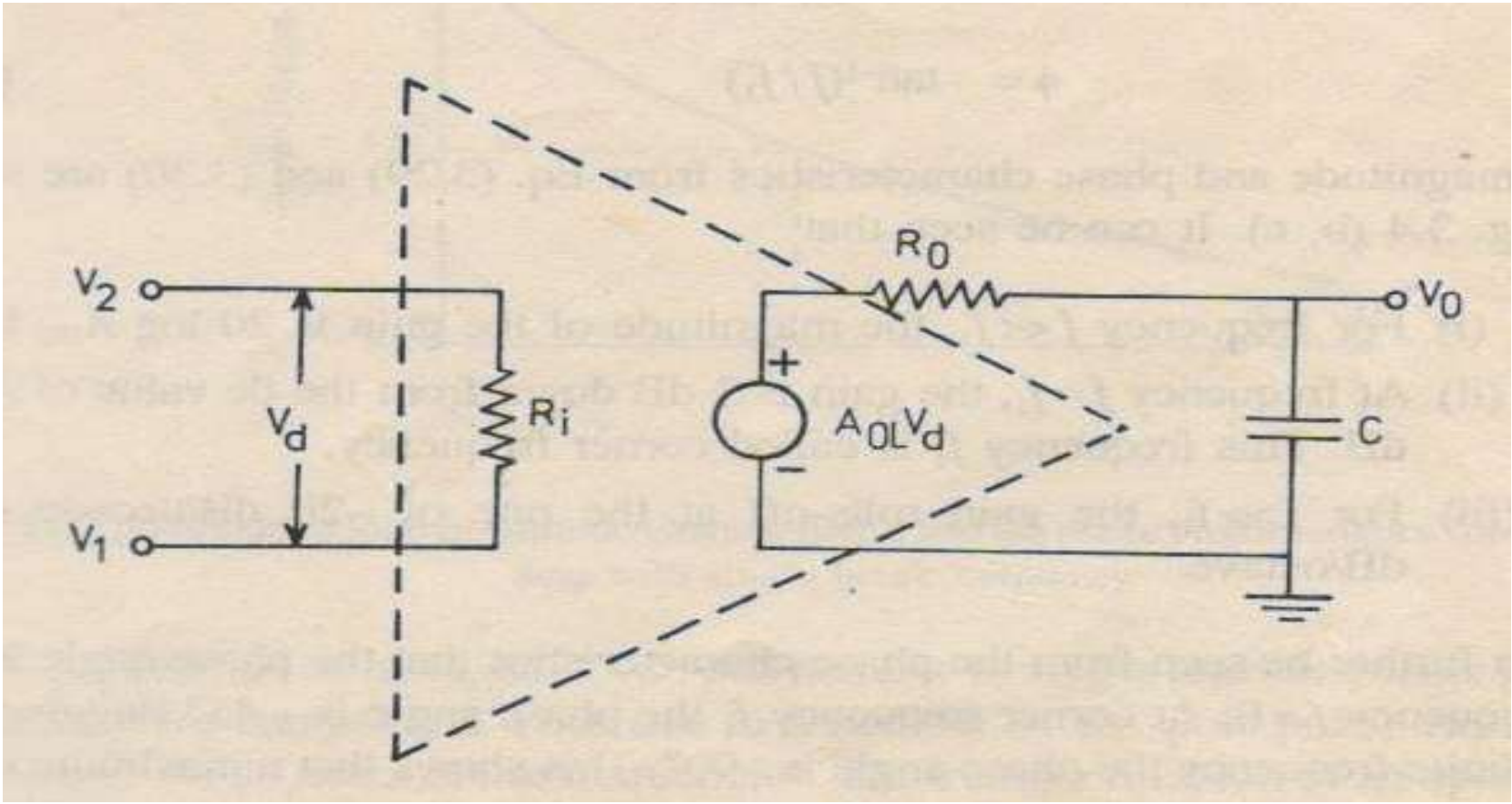
- It is defined as the average rate of change of input offset voltage per unit change in temperature.
- It is also called as input offset voltage drift.

$$\text{Input offset voltage drift} = \frac{\Delta V_{ios}}{\Delta T}$$

ΔV_{ios} = change in input offset voltage

ΔT = Change in temperature

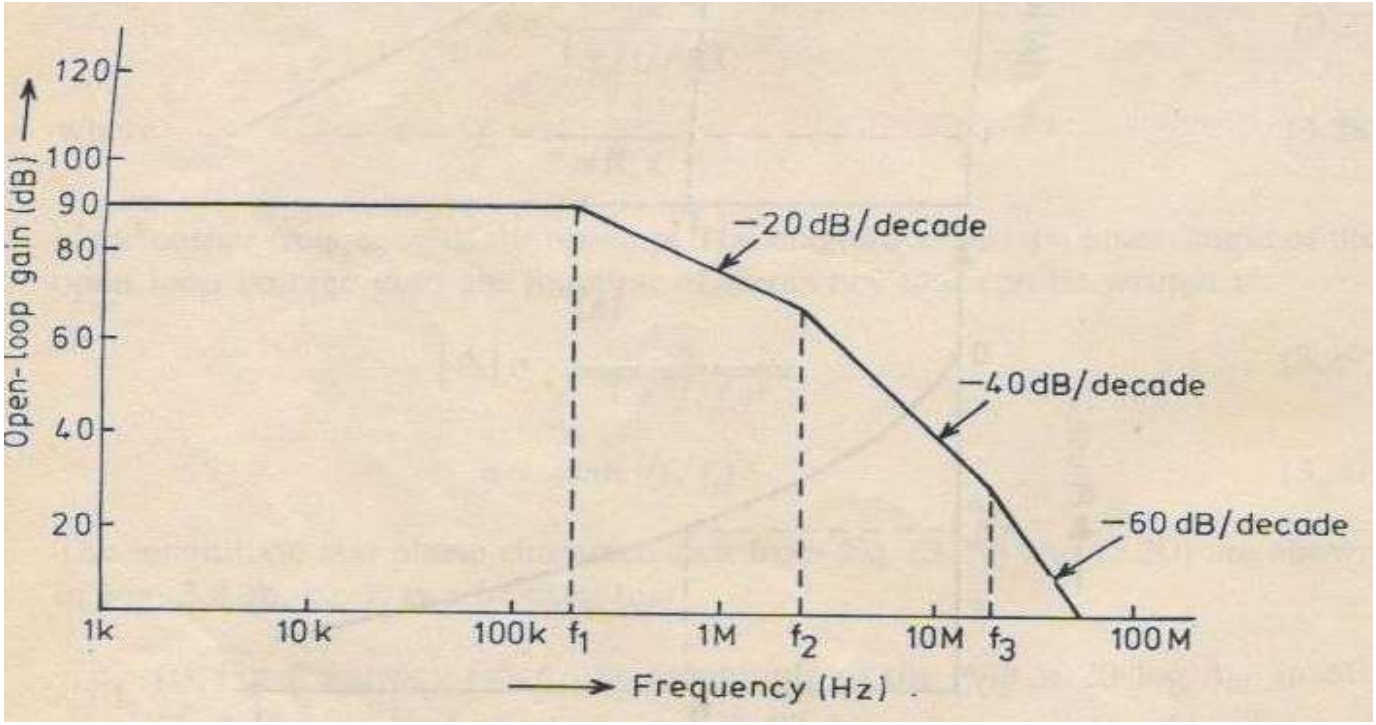
AC CHARACTERISTICS



HIGH FREQUENCY MODEL OF OPAMP

AC CHARACTERISTICS

1. Frequency Response



OPEN LOOP GAIN VS FREQUENCY

Need for frequency compensation in practical op-amps

- Frequency compensation is needed when large bandwidth and lower closed loop gain is desired.
- Compensating networks are used to control the phase shift and hence to improve the stability

Frequency compensation methods

- Dominant- pole compensation
- Pole- zero compensation

2. Slew Rate

It is defined as the maximum rate of change of output voltage with time. The slew rate is specified in V/μsec

$$\text{Slew rate} = S = dV_o / dt \big|_{max}$$

It is specified by the op-amp in unity gain condition.

The slew rate is caused due to limited charging rate of the compensation capacitor and current limiting and saturation of the internal stages of op-amp, when a high frequency large amplitude signal is applied.

Slew Rate

It is given by $dV_c/dt = I/C$

For large charging rate, the capacitor should be small or the current should be large.

$$\boxed{S = I_{max} / C}$$

For 741 IC the charging current is 15 μA and the internal capacitor is 30 pF. S= 0.5V/ μsec

Slew Rate

$V_s = V_m \sin\omega t$

$V_o = V_m \sin\omega t$

$$\frac{dVo}{dt} = V_m \omega \cos\omega t$$

$$\text{S = slew rate} = \left.\frac{dVo}{dt}\right|_{max}$$

$S = V_m \omega = 2 \pi f V_m$

$S = 2 \pi f V_m$ V / sec

This is also called **full power bandwidth** of the op-amp

For distortion free output, the maximum allowable input frequency f_m can be obtained as

$$f_m = \frac{S}{2 \Pi V_m}$$

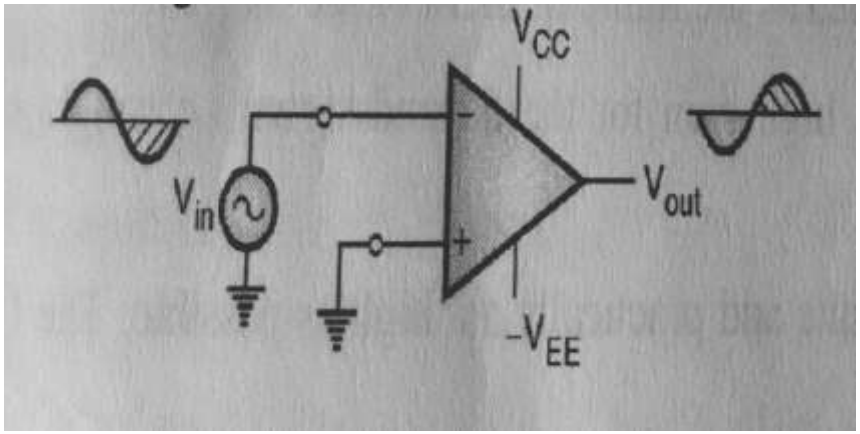
741 OP-AMP FEATURES

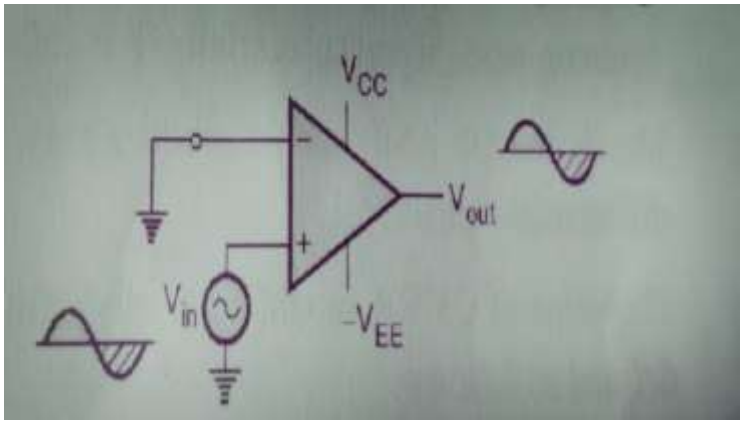
- No frequency compensation required.
- Short circuit protection.
- Offset voltage null capability.
- Large common mode and differential voltage ranges.
- No latch ups.

OP-AMP INPUT MODES

- **Single ended mode**

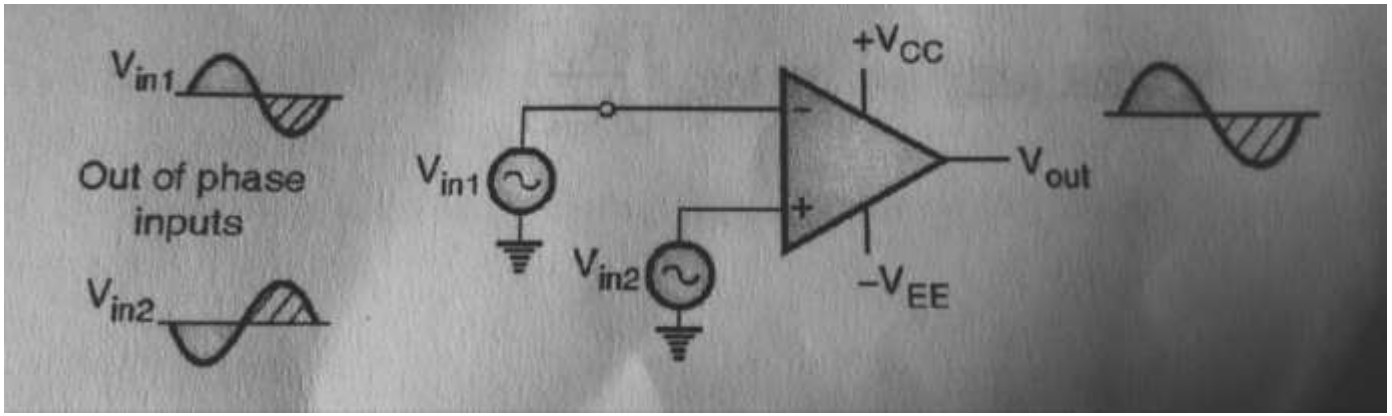
  If the input signal is applied to only one of the inputs and the other input terminal is connected to ground it is said to be operating in single ended mode.





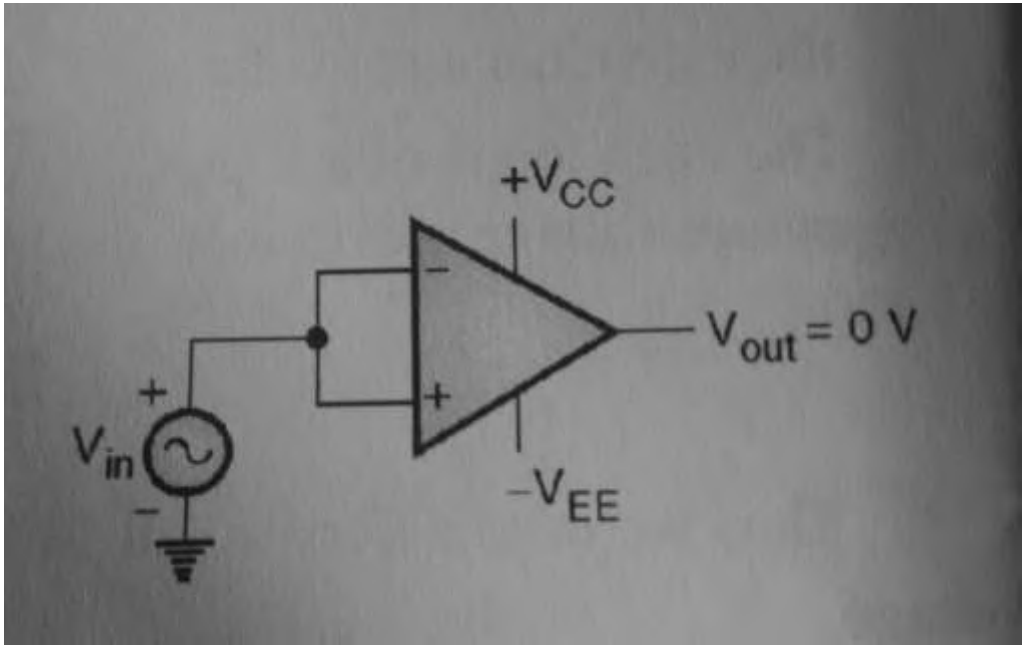
- **Differential mode/double ended**

  In differential mode ,two opposite polarity signal are applied to the two inputs of op amp. The difference between the input signal is amplified appears at the output.



- **Common mode**

  In the common mode of operation, the same input signal is applied to both the input terminals. Ideally a zero voltage should be produced by the op amp.



THE MODES OF USING AN OP-AMP

- ***Open Loop :*** (The output assumes one of the two possible output states, that is $+V_{sat}$ or $-V_{sat}$ and the amplifier acts as a switch only).
- ***Closed Loop:*** (The utility of an op-amp can be greatly increased by providing negative feed back. The output in this case is not driven into saturation and the circuit behaves in a linear manner).

Open Loop Configuration Of Op-amp

- The voltage transfer curve indicates the inability of op-amp to work as a linear small signal amplifier in the open loop mode
- Such an open loop behavior of the op-amp finds some rare applications like voltage comparator, zero crossing detector etc.

Open Loop Op-amp Configurations

- The configuration in which output depends on input, but output has no effect on the input is called open loop configuration.
- No feed back from output to input is used in such configuration.
- The op-amp works as high gain amplifier
- The op-amp can be used in three modes in open loop configuration they are

  Differential amplifier

  Inverting amplifier

  Non inverting amplifier

Why op-amp is generally not used in open loop mode?

- As open loop gain of op-amp is very large, very small input voltage drives the op-amp voltage to the saturation level. Thus in open loop configuration, the output is at its positive saturation voltage ($+V_{sat}$) or negative saturation voltage ($-V_{sat}$) depending on which input V_1 or V_2 is more than the other. For a.c. input voltages, output may switch between positive and negative saturation voltages

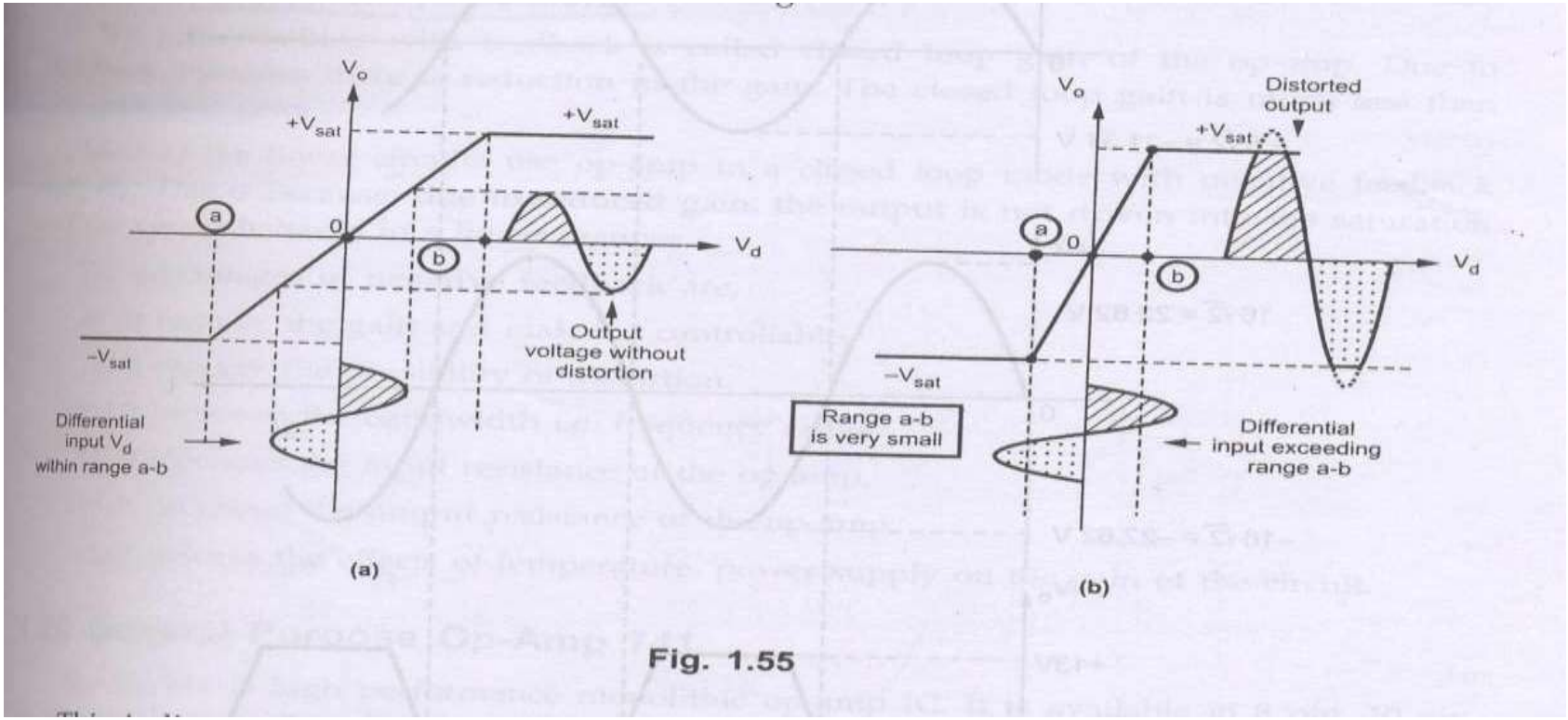


Fig. 1.55

This indicates the inability of op-amp to work as a linear small signal amplifier in the open loop mode.Hence the op-amp in open loop configuration is not used for the linear applications.

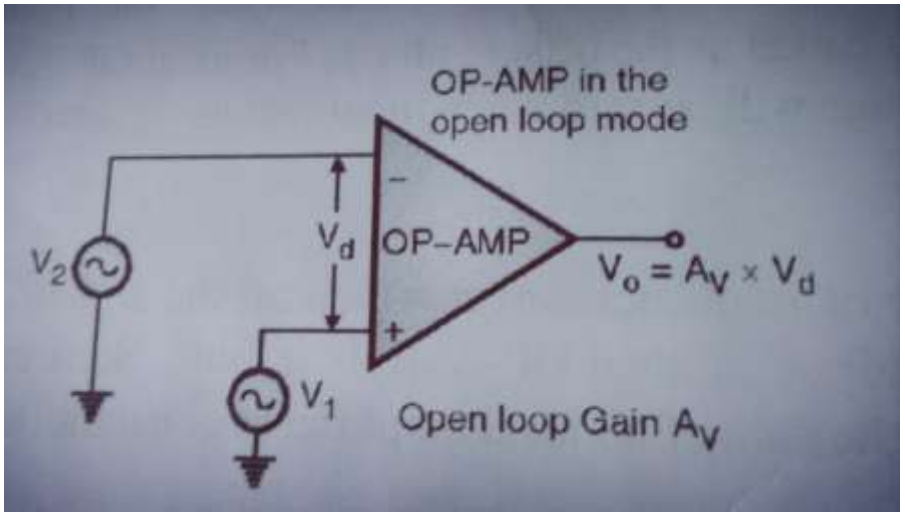
CONFIGURATION OF OP-AMP

- Open loop configuration

  In open loop configuration , there is no feedback from output to input.

- The differential signal present between the inputs will be amplified by it's open loop gain.($Av=2\times10^5$)

•Therefore even for very small magnitude of differential voltage output will reach positive or negative saturation.



Closed Loop Operation of Op-amp

- The utility of the op-amp can be increased considerably by operating in closed loop mode.
- The closed loop operation is possible with the help of feedback. The feedback allows to feed some part of the output back to the input terminals. In the linear applications, the op-amp is always used with negative feedback.
- The negative feedback helps in controlling gain, which otherwise drives the op-amp out of its linear range, even for a small noise voltage at the input terminals.

- In close loop configuration , a feedback is introduced

i.e. a part of output is fed back to the input.

The feedback can be of the following two types:

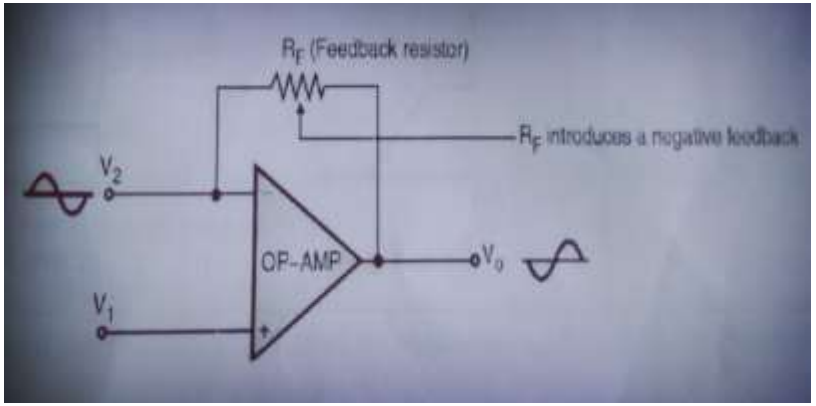
1. Positive feedback/regenerative feedback

2.Negative feedback/degenerative feedback

POSITIVE FEEDBACK

- If the feedback signal and the input signal are in phase with each other then it is called as the positive feedback.
- It is used in application such as oscillators and schmitt trigger or regenerative comparators.

NEGATIVE FEEDBACK



•If the signal fed back to the input and the original input signal are 180º out of phase, then it is called as the negative feedback.

•In application of op amp as an amplifier, the negative feedback is used.

DIFFERENTIAL AMPLIFIER

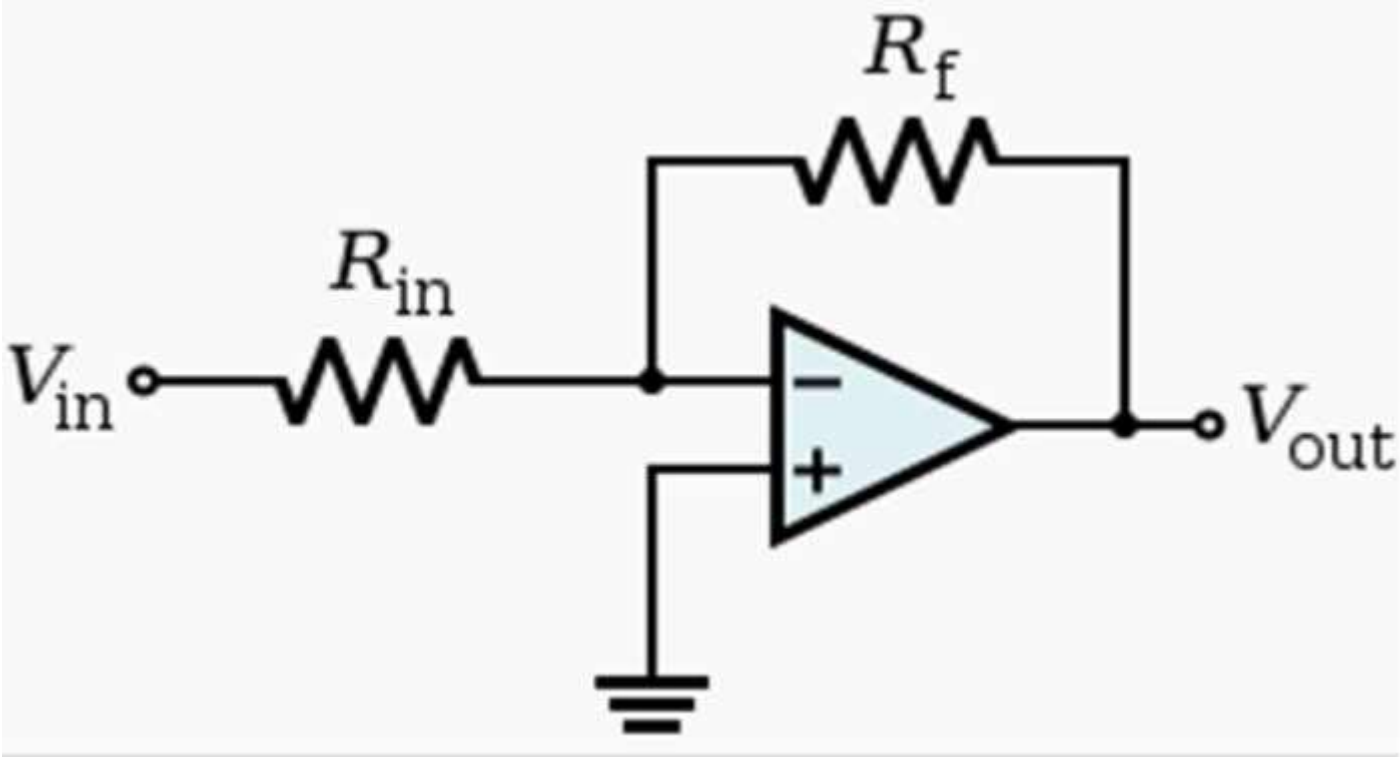
- The amplifier which amplifies the difference between the two input
- voltages is called differential amplifier.
- $V_o = A_{OL} V_d = A_{OL}(V_1 - V_2) = A_{OL}(V_{in1} - V_{in2})$
- Keypoint: The negative sign indicates that there is phase shift of 180^o
- between input and output i.e. output is inverted with respect to input.

INVERTING AMPLIFIER

- Uses negative feedback to invert and amplify a voltage (multiplies by a negative constant)

$$V_{\text{out}} = -\frac{R_{\text{f}}}{R_{\text{in}}} V_{\text{in}}$$

INVERTING AMPLIFIER

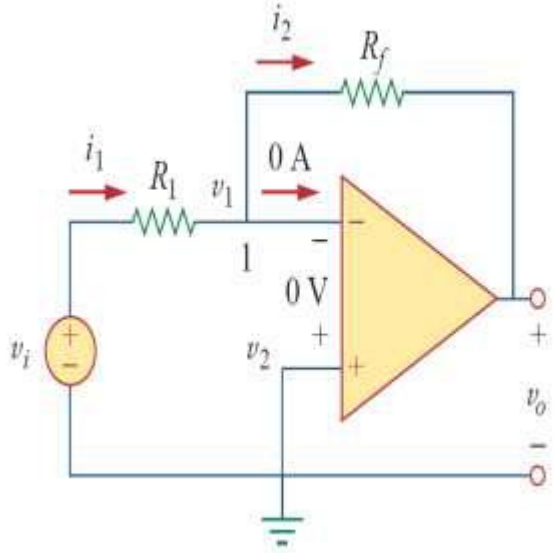


INVERTING OP-AMP

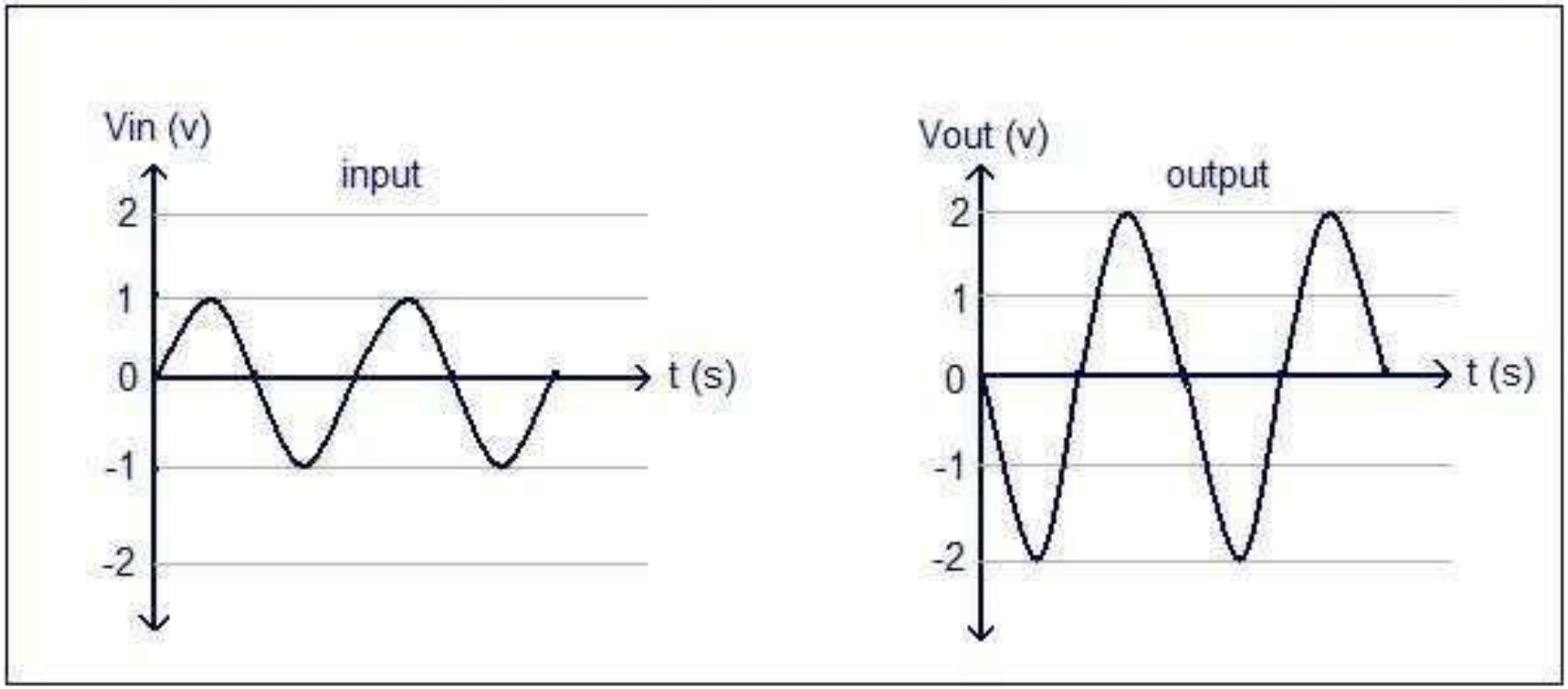
- By applying KCL
- $i_1=i_2$
- $(V_i-V_1)/R_1=(V_1-V_0)/R_f$------(1)
- $v_{1=}v_{2=}0$ then eq (1) becomes
- $V_i/R_1= -V_o/R_f$

Then the voltage gain

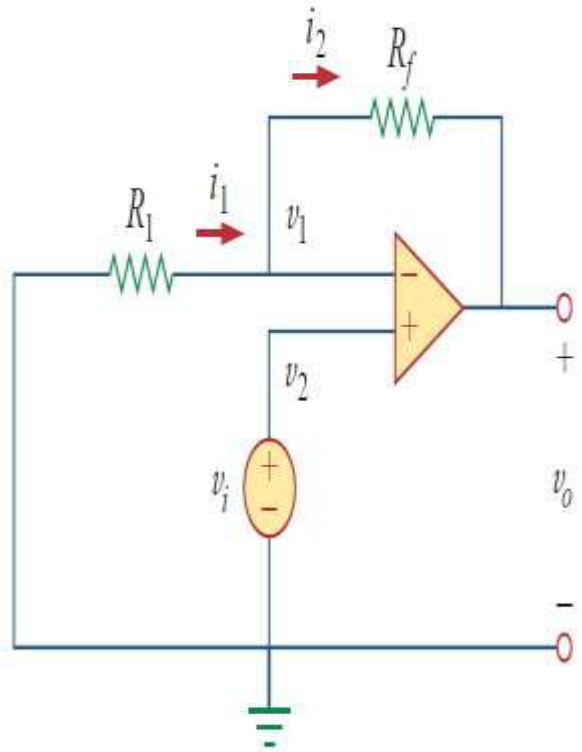
$A_v=V_o/V_i= -R_f/R_1$



INVERTING OP-AMP INPUT AND OUTPUT WAVE FORM



NON INVERTING OP-AMP



or

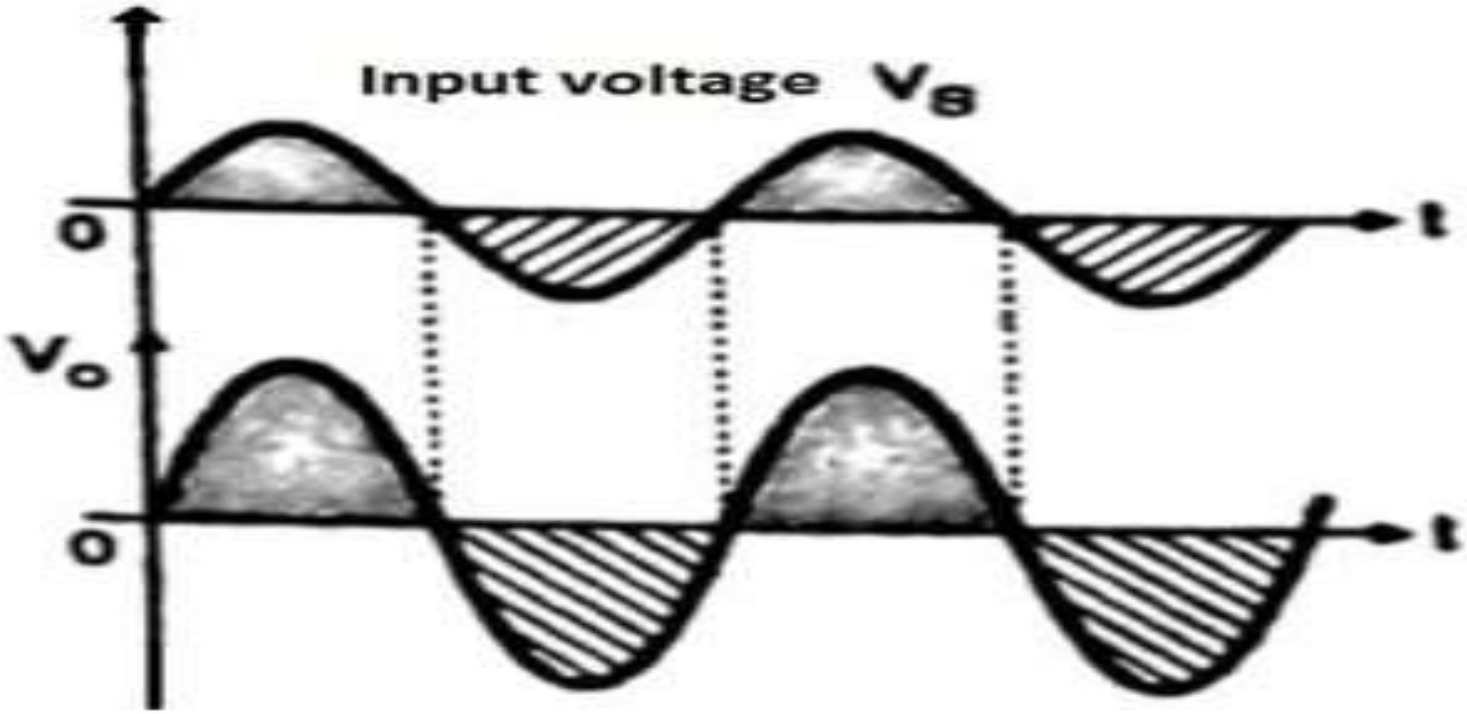
$$i_1 = i_2 \Rightarrow \frac{0 - v_1}{R_1} = \frac{v_1 - v_o}{R_f}$$

But $v_1 = v_2 = v_i$.

$$\frac{-v_i}{R_1} = \frac{v_i - v_o}{R_f}$$

$$v_o = \left(1 + \frac{R_f}{R_1}\right) v_i$$

NON INVERTING OP-AMP INPUT AND OUTPUT WAVE FORM

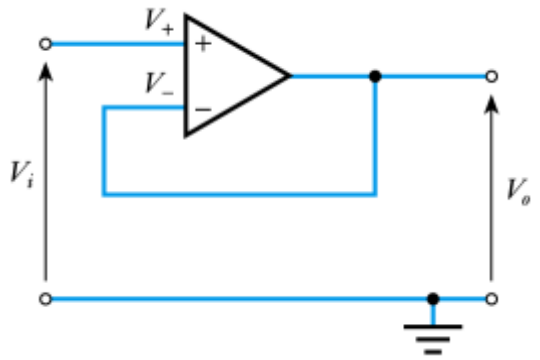


UNITY GAIN AMPLIFIER

- A unity gain buffer amplifier Analysis

  This is a special case of the non-inverting amplifier with $R_1 = 0$ and $R_2 = \infty$

  Hence $$G = \frac{R_1 + R_2}{R_2} = \frac{R_1}{R_2} + 1 = \frac{0}{\infty} + 1 = 1$$



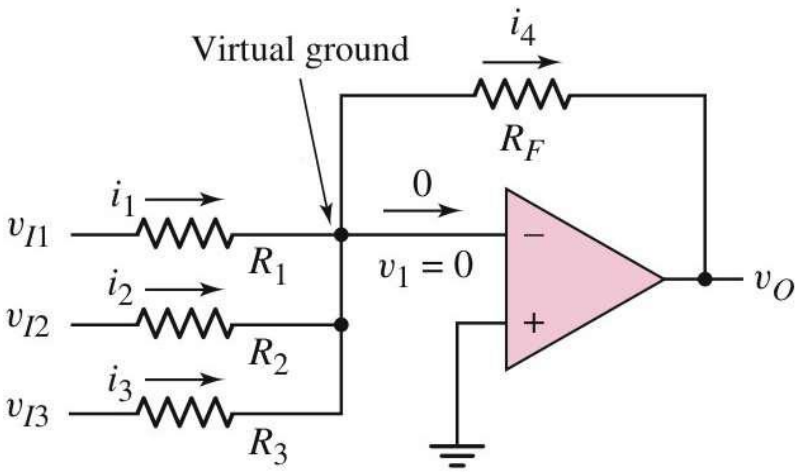
  Thus the circuit has a gain of unity

- At first sight this might not seem like a very useful circuit, however it has a high input resistance and a low output resistance and is therefore useful as a buffer amplifier

BASIC APPLICATIONS OF OP-AMP

- Summer
- Subtractor
- Instrumentation Amplifier
- AC Amplifier
- V to I and I to V converters
- Sample & Hold Circuits
- Multiplier and Divider
- Differentiator & Integrator
- Comparator
- Schmitt Trigger
- Multivibrator

SUMMING AMPLIFIER



Similarly,

Using KCL at the input node

$$i_1 + i_2 + i_3 - i_4 - 0 = 0$$

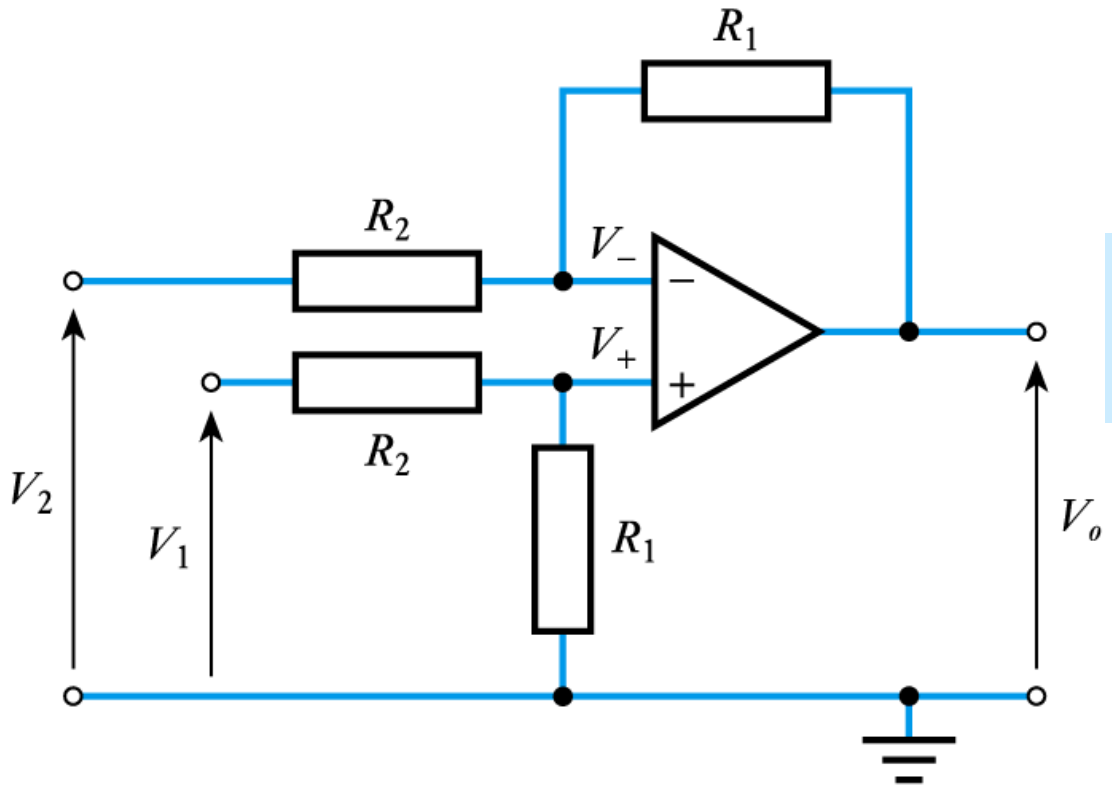
Output voltage

$$V_0 = -R_F\left(\frac{V_{i1}}{R_1} + \frac{V_{i2}}{R_2} + \frac{V_{i3}}{R_3}\right)$$

Example 8.2

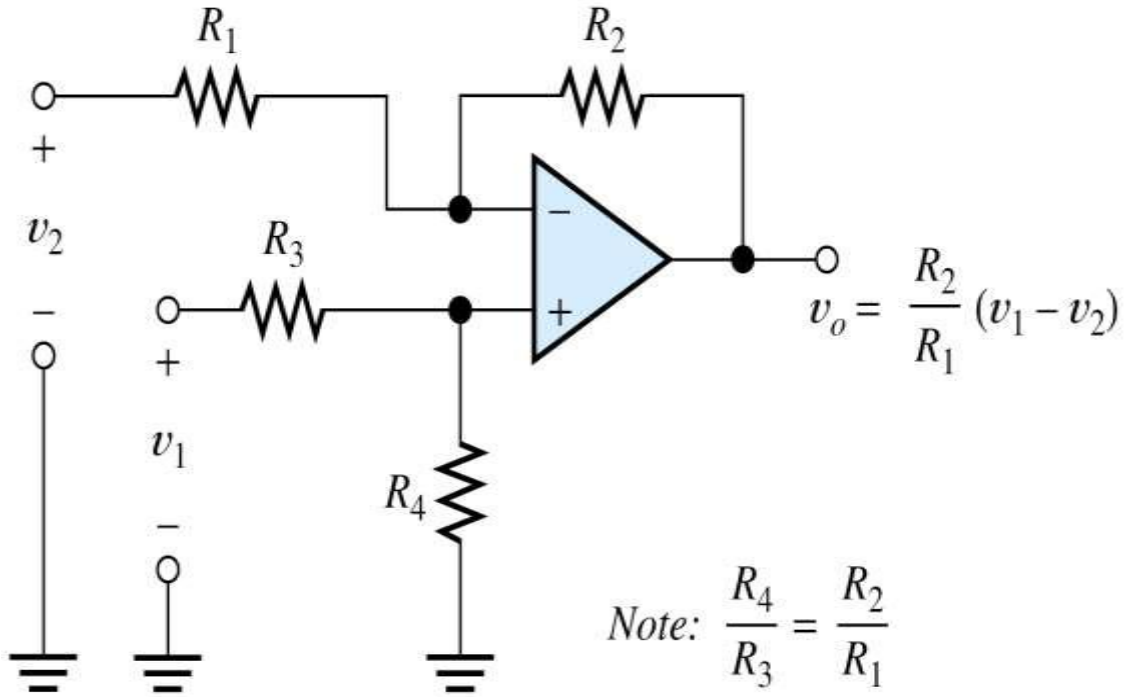
Design a summing amplifier as shown in figure to produce a specific output signal, such that $v_o = 1.25 - 2.5 \cos \omega t$ volt. Assume the input signals are $v_{I1} = -1.0$ V, $v_{I2} = 0.5 \cos \omega t$ volt. Assume the feedback resistance $R_F = 10\ k\Omega$

A DIFFERENTIAL AMPLIFIER (OR SUBTRACTOR)



$$V_o = (V_1 - V_2)\frac{R_1}{R_2}$$

INSTRUMENTATION AMPLIFIER



•Differential amplifiers are widely used in engineering instrumentation.

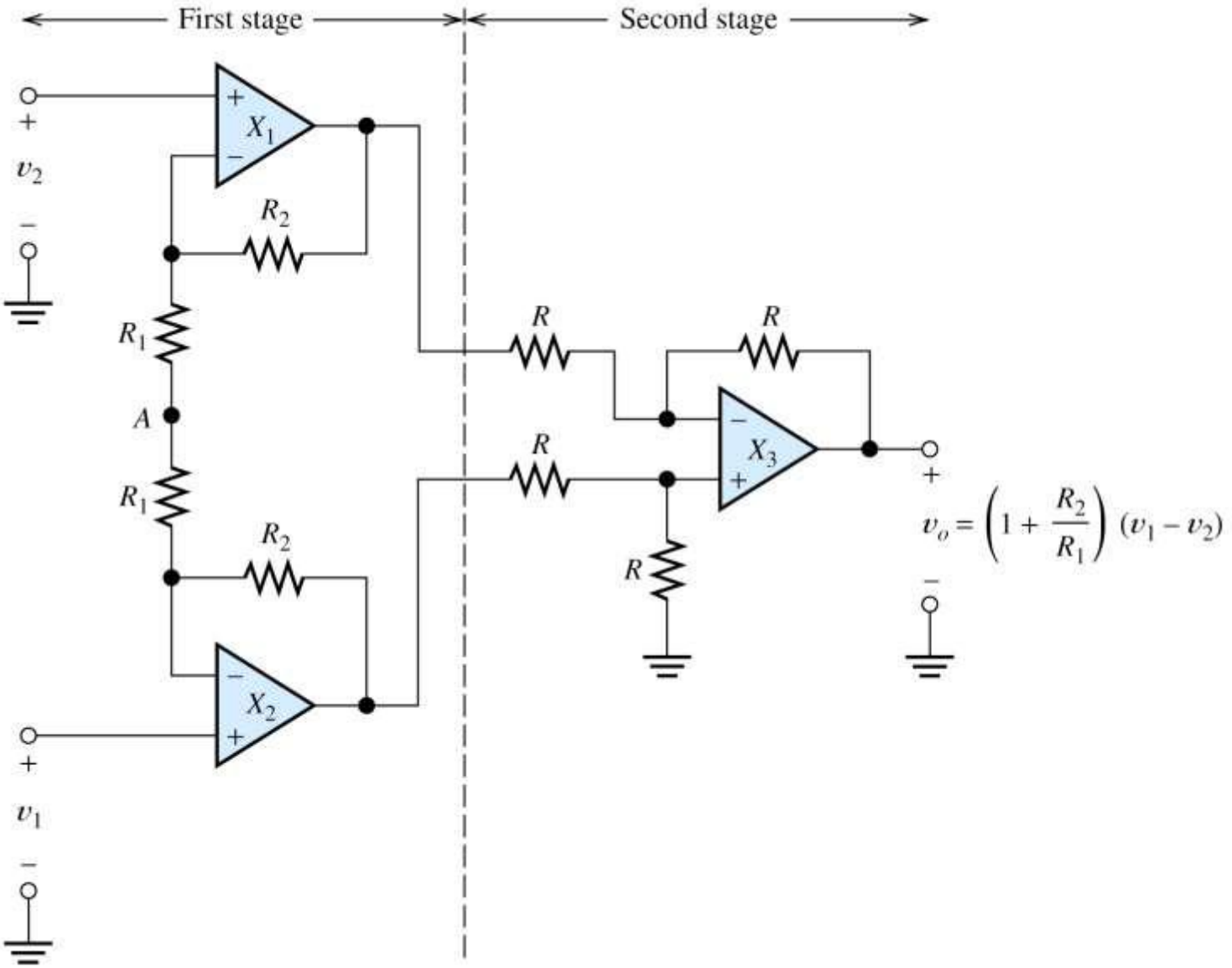
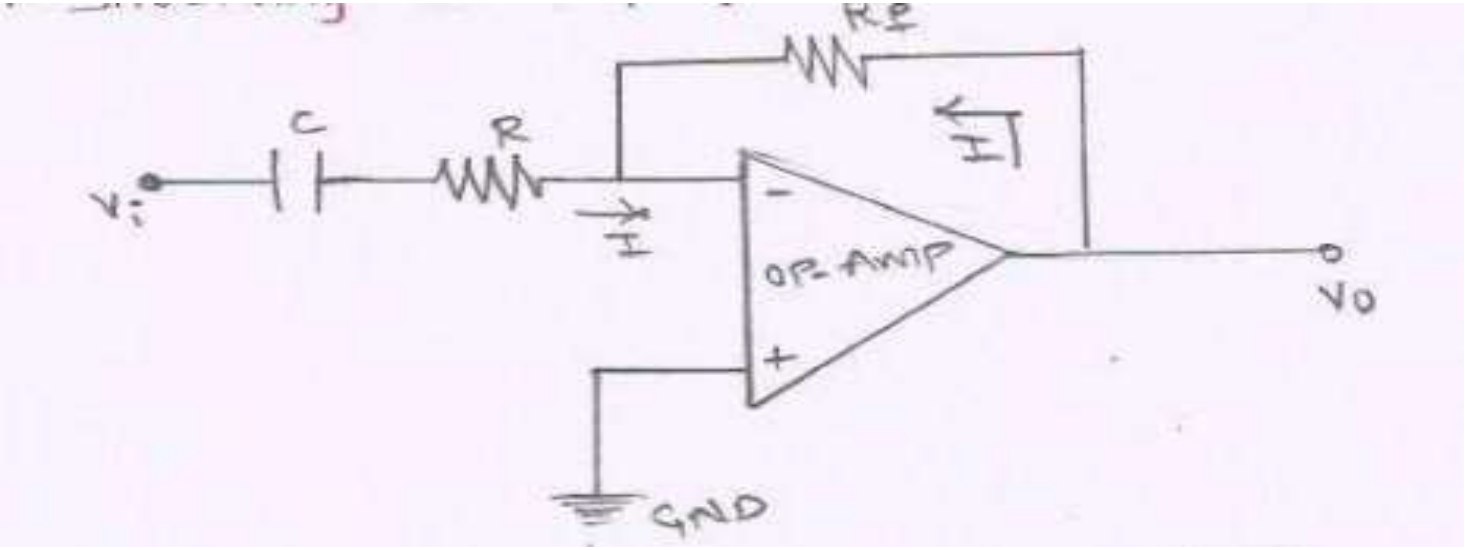


Figure 14.34 Instrumentation-quality differential amplifier.

FEATURES OF INSTRUMENTATION AMPLIFIER

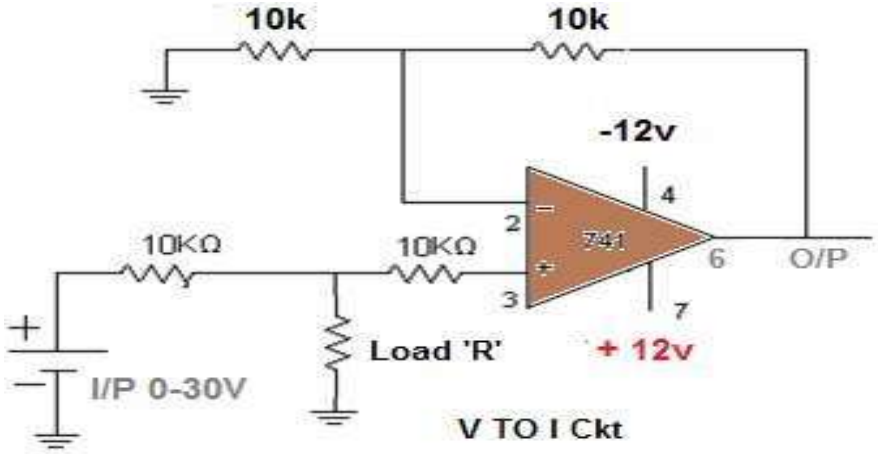
1. high gain accuracy
2. high CMRR
3. high gain stability with low temperature co- efficient
4. low dc offset
5. low output impedance

AC AMPLIFIER



$$V_o = -I R_f$$

VOLTAGE-TO-CURRENT CONVERTER



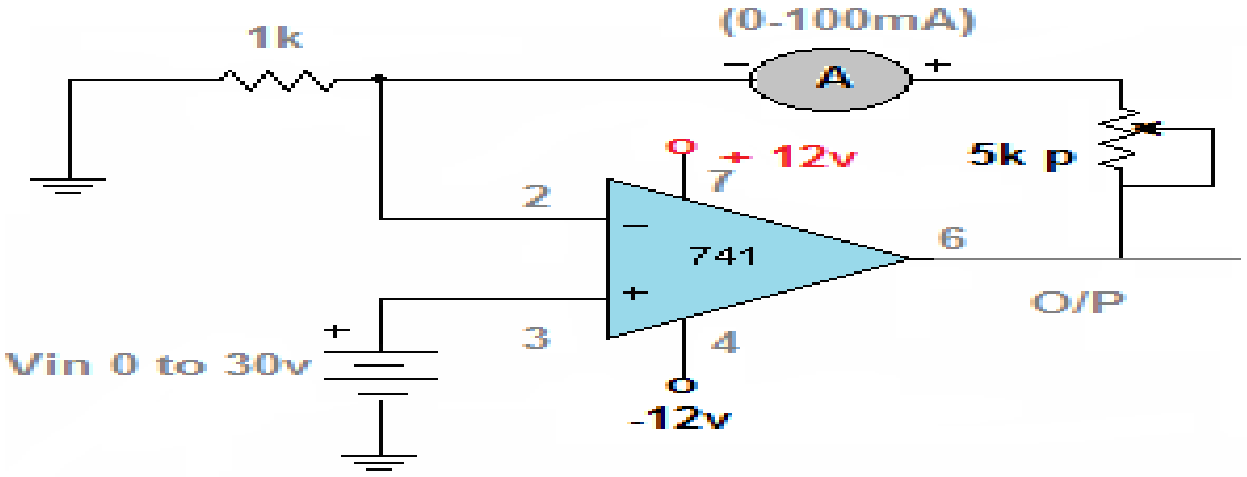
Formula: Grounded load:- V – I converter.

$V_{in} = V_{id} + V_f$ where V_{id} is input difference voltage and V_f is the feedback voltage

But $V_{id} = 0$

$V_{in} = V_f = R_1 R_L$

$I_L = V_{in}/R_L$



Formula: Floating load V – I converter.

$I_1+I_2=I_L$

$(V_{in}-V_1)/R+(V_o-V_1)/R=I_L$

$V_{in}+V_o-2V_i=I_LR$

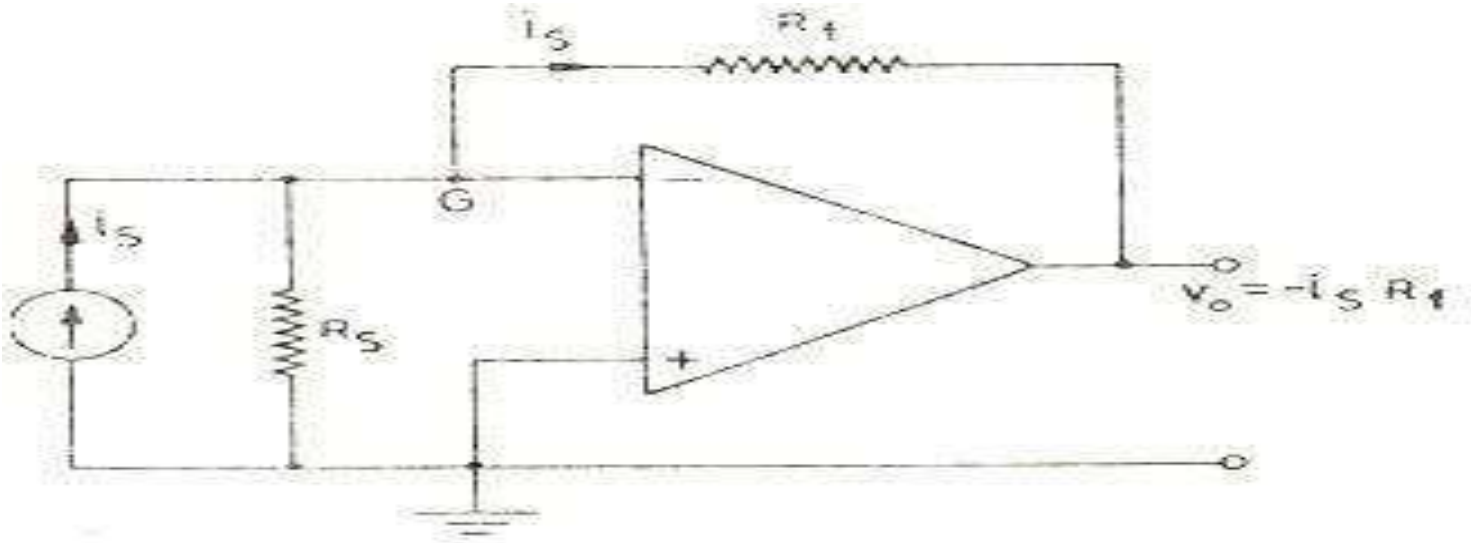
Since op-amp is non inverting

Gain=1+(R/R)=2

Vo=2Vi

V_{in}=Vo-Vo+I_LR $I_L=V_{in}/R$

CURRENT-TO-VOLTAGE CONVERTER



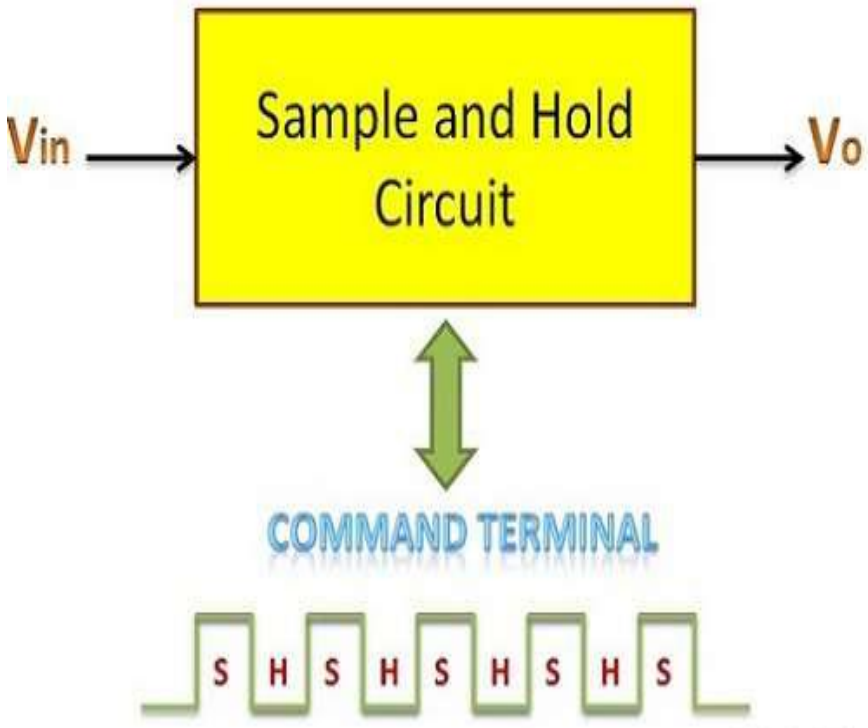
$$V_o = -i_s R_f$$

SAMPLE AND HOLD CIRCUIT

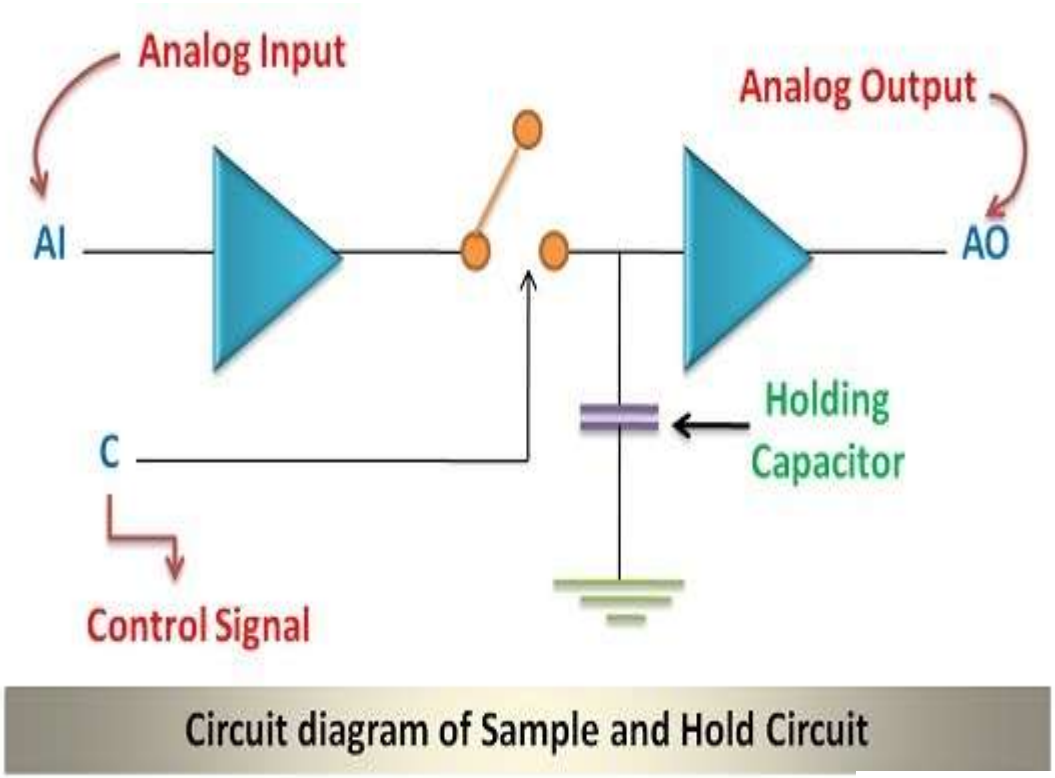
- The time during which sample and hold circuit generates the sample of the input signal is called **sampling time.**
- Similarly, the time duration of the circuit during which it holds the sampled value is called **holding time.**
- Sampling time is generally between **1µs to 14 µs** while the holding time can assume any value as required in the application.
- Capacitor is the heart of sample and hold circuit. The capacitor charges to its peak value when the switch is closed, i.e. during sampling and holds the sampled voltage when the switch is open.

- The N-channel Enhancement MOSFET is used as the switching element.
- Input voltage is applied through its drain terminal and control voltage to its gate terminal.
- When the positive pulse of the control voltage is applied, the MOSFET will be switched to ON state - it acts as a closed switch.
- On the contrary, when the control voltage is zero then the MOSFET will be switched to OFF state - acts as an open switch.
- When the switch is closed, the analog signal applied to it through the drain terminal is fed to the capacitor.
- The capacitor charges to its peak value.
- When the MOSFET switch is opened, then the capacitor stops charging. Due to the high impedance operational amplifier connected at the end of the circuit, the capacitor experiences high impedance due to this it cannot get discharged.
- Charge is held by the capacitor for a definite amount of time - **holding period.**
- Time in which samples of the input voltage is generated **- sampling period.**

SAMPLE AND HOLD CIRCUIT

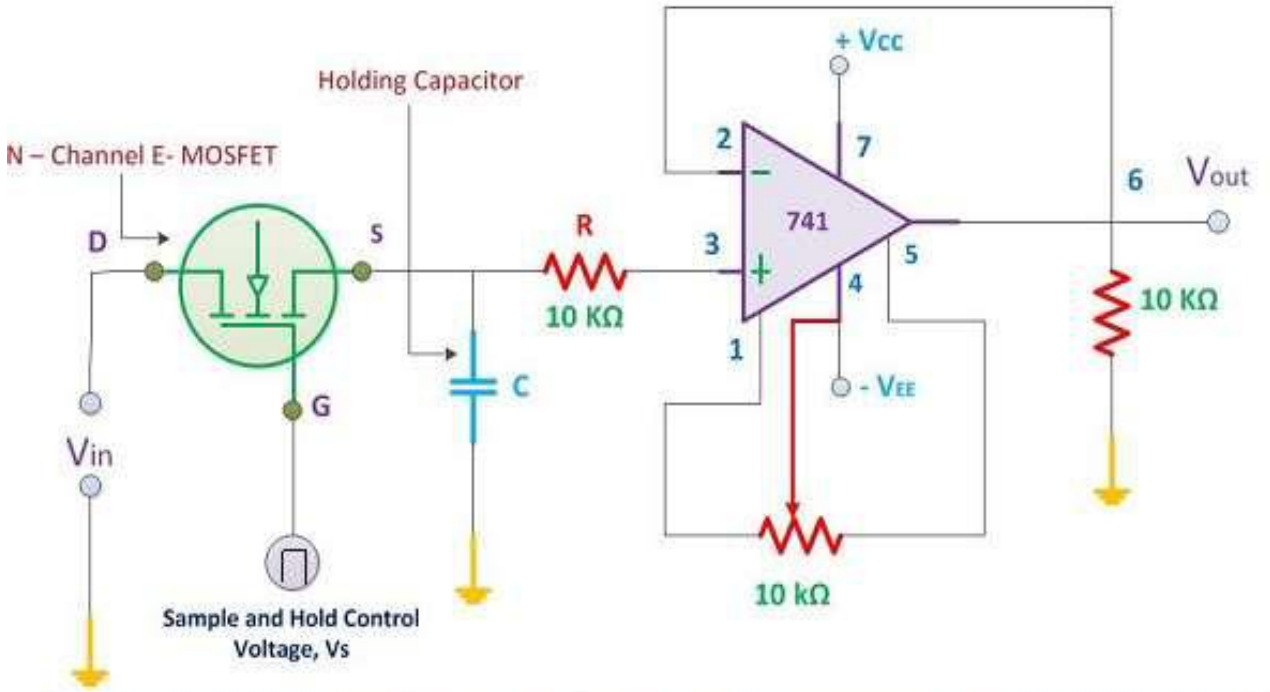


Sample and Hold Circuit Diagram



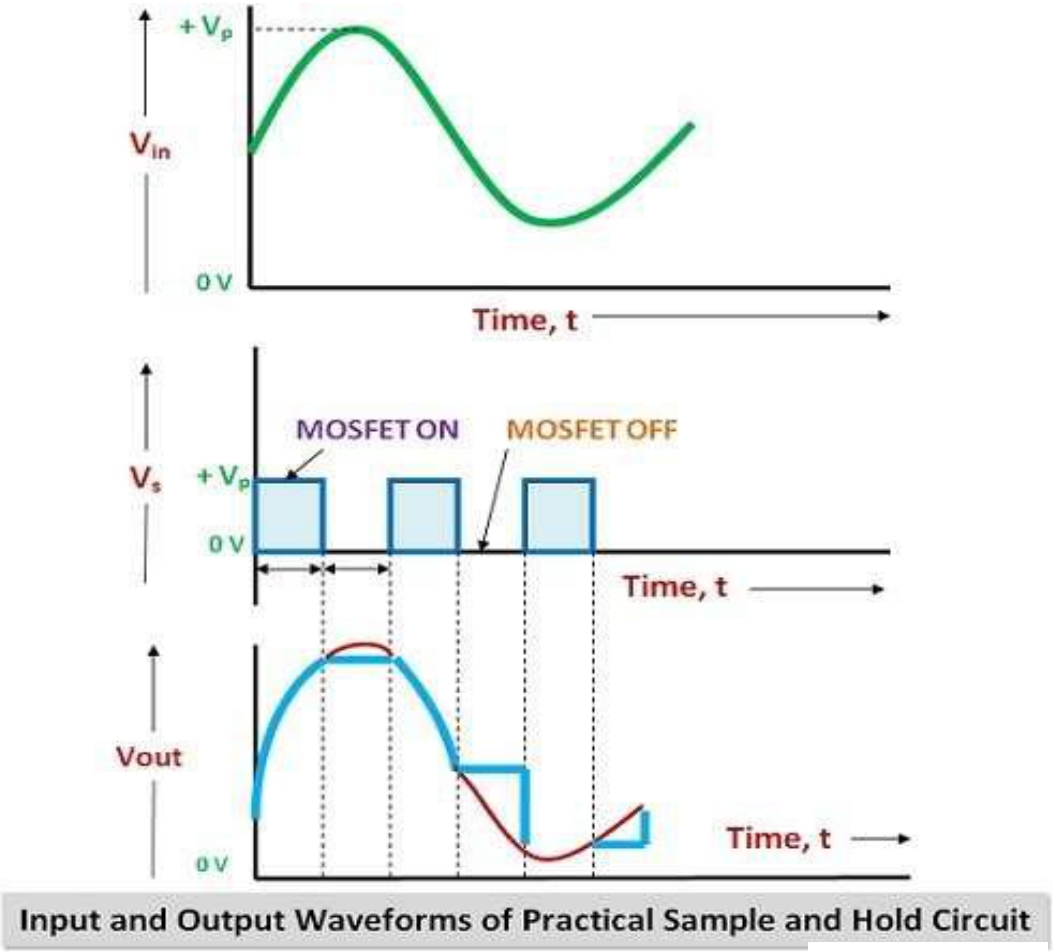
Circuit diagram of Sample and Hold Circuit

Circuit Diagram



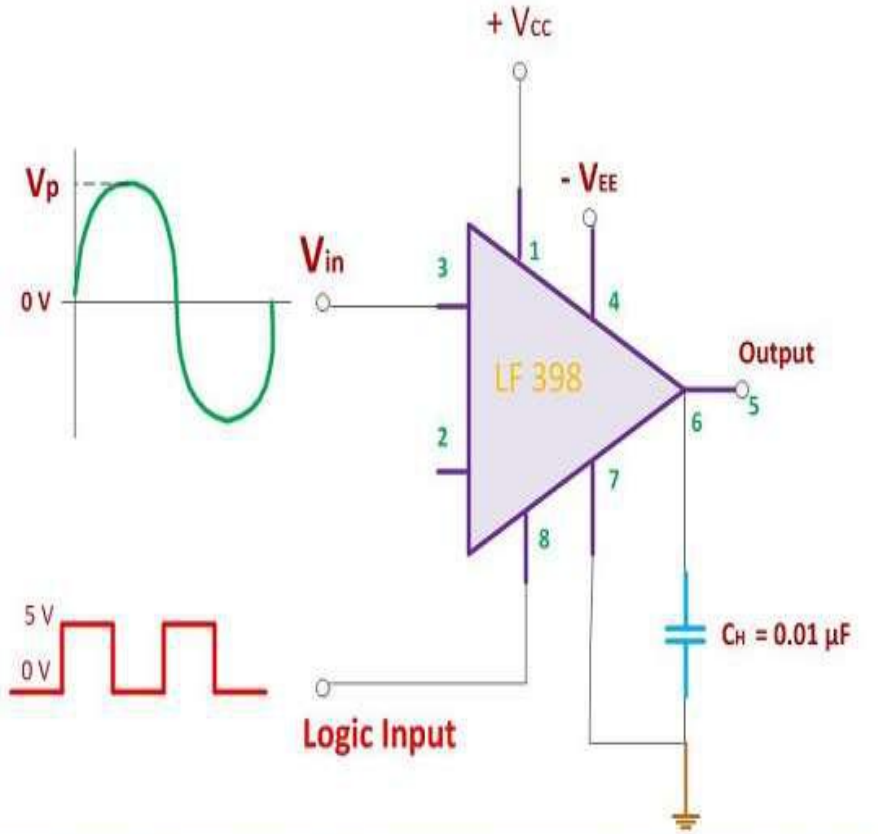
Practical Circuit of Sample and Hold Circuit

Input-Output Waveform



Input and Output Waveforms of Practical Sample and Hold Circuit

LF 398

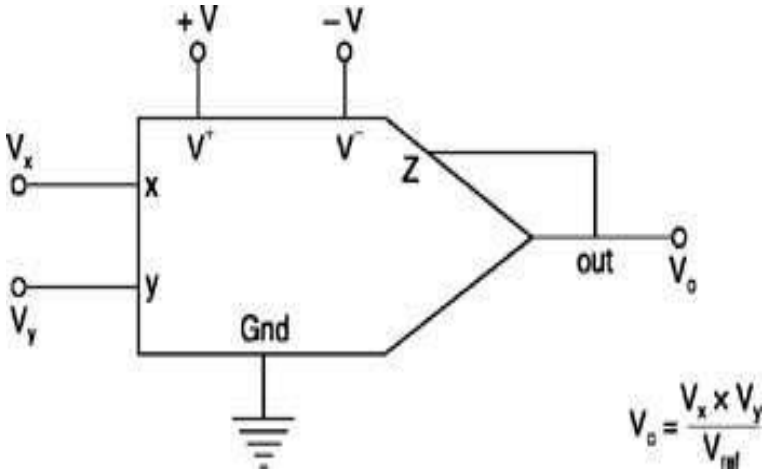


Typical Connection Diagram of Sample and Hold Circuit

APPLICATIONS OF SAMPLE AND HOLD CIRCUIT

- Data Distribution System
- Sampling Oscilloscopes
- Data Conversion System
- Digital Voltmeters
- Analog Signal Processing
- Signal Constructional Filters

MULTIPLIER AND DIVIDER



Symbol for a multiplier.

The output voltage can be written as $V_o = \frac{V_x \times V_y}{V_{ref}}$

- where V_x and V_y are input signals
- V_{ref} is a reference voltage that is normally set to 10 volts. As long as $V_x < V_{ref}$ and $V_y < V_{ref}$, output will be less than V_{ref}.
- If both inputs are positive, then the multiplier is called a one-quadrant multiplier. If one input is kept at a positive value and the other input is allowed to take either a positive or negative value, then it is called a two-quadrant multiplier. If both the inputs are allowed to take either positive or negative values, then it is called a four-quadrant multiplier.

- The applications of multipliers include frequency doubling, frequency shifting, phase angle detection, real power computation, and squaring signals.

DIVIDER

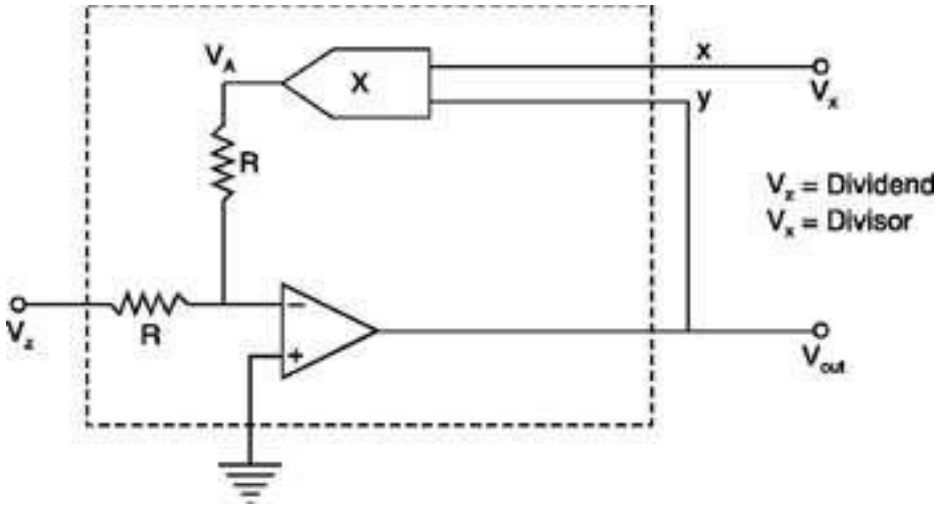


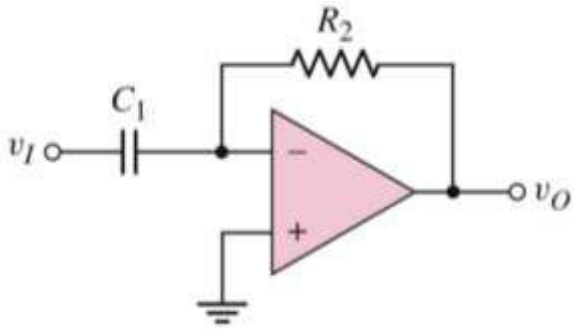
Figure 4.13: Divider.

Vout can be written as $V_{out} = -V_{ref}\frac{V_z}{V_x}$

The applications of dividers include taking square root and dividing one number by another.

DIFFERENTIATOR

Output voltage, $v_0 = -R_2 C_1 \frac{dv_I}{dt}$



Differentiator circuit

EXAMPLE 8.4

Determine the output voltage of a differentiator circuit as shown in figure, assume that the input voltage $v_I = 3.5\ \cos(100\pi\, t)$ volt and the time constant RC = 1.5 ms.

Solution: output voltage

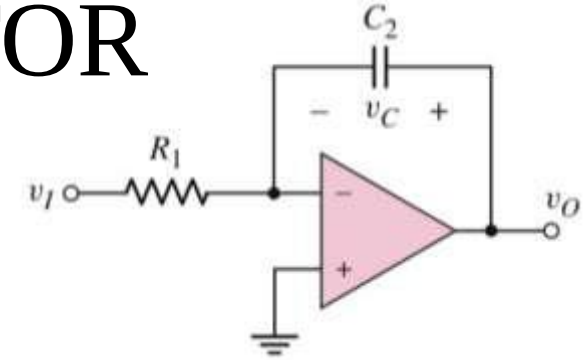
$$v_0 = -R_2 C_1 \frac{dv_I}{dt} = -(1.5 \times 10^{-3}) \frac{d[3.5\ \cos(100\pi\, t)]}{dt}$$

Or, $v_0 = -(1.5 \times 10^{-3})[-3.5 \times 100\pi \times \sin(100\pi\, t)]$

Or, $v_0 = 1.65 \sin(100\pi\, t)$ volt

INTEGRATOR

Output voltage, $v_0 = -\frac{1}{R_1 C_2}\int v_I \, dt$



Integrator circuit

If the capacitor has some initially voltage, V_C

$$v_0 = V_C - \frac{1}{R_1 C_2}\int v_I \, dt$$

EXAMPLE 8.3

An integrator circuit as shown in figure has a voltage $V_C = -1.4$ V across the capacitor at time $t = 0$. A step input voltage $v_I = -2$ V is applied at time $t = 0$. Determine the *RC* time constant necessary such that the output voltage reaches +10.2 V at time $t = 5$ ms.

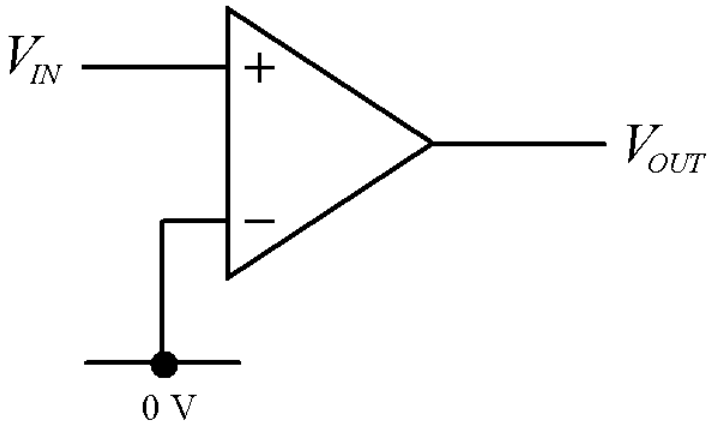
Solution: output voltage

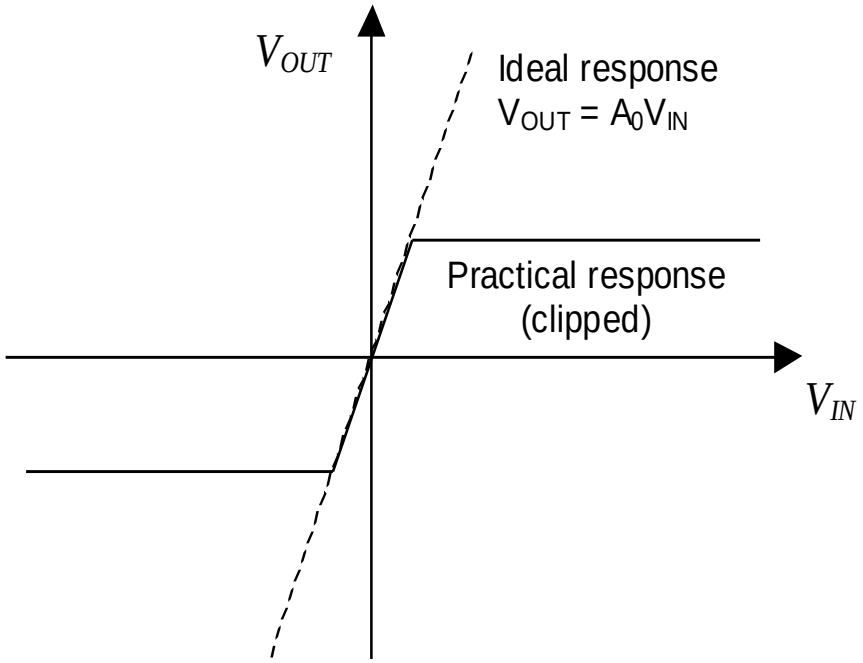
$$v_0 = V_C - \frac{1}{R_1 C_2}\int v_I \, dt = V_C - \frac{1}{R_1 C_2}\int_0^5 v_I \, dt$$

Or, $$10.2 = -1.4 - \frac{(-2)}{R_1 C_2}\int_0^5 dt = -1.4 + \frac{2}{R_1 C_2}[5]$$

Or, $$R_1 C_2 = 0.862 \text{ ms.}$$

COMPARATOR





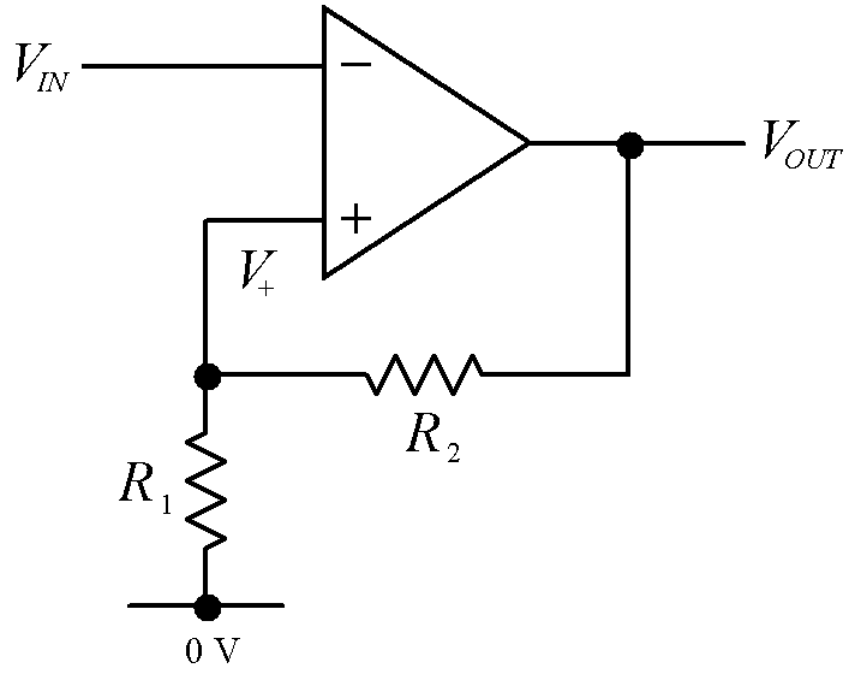
If A_0 is large, practical response can be approximated as :

$$V_{IN} > 0 \Rightarrow V_+ > V_- \Rightarrow V_{OUT} = +V_{SAT}$$

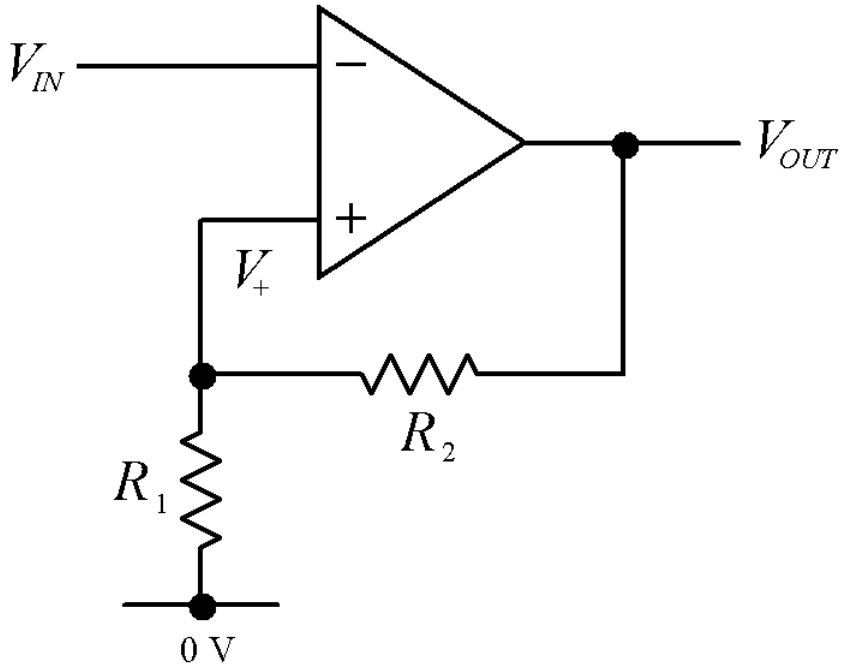
$$V_{IN} < 0 \Rightarrow V_+ < V_- \Rightarrow V_{OUT} = -V_{SAT}$$

SCHMITT TRIGGER

- The Schmitt trigger is an op-amp comparator circuit featuring hysteresis.
- The inverting variety is the most commonly used.



SCHMITT TRIGGER ANALYSIS



Switching occurs when:

$$V_{IN} = V_- = V_+ = V_{OUT}\frac{R_1}{R_1 + R_2}$$

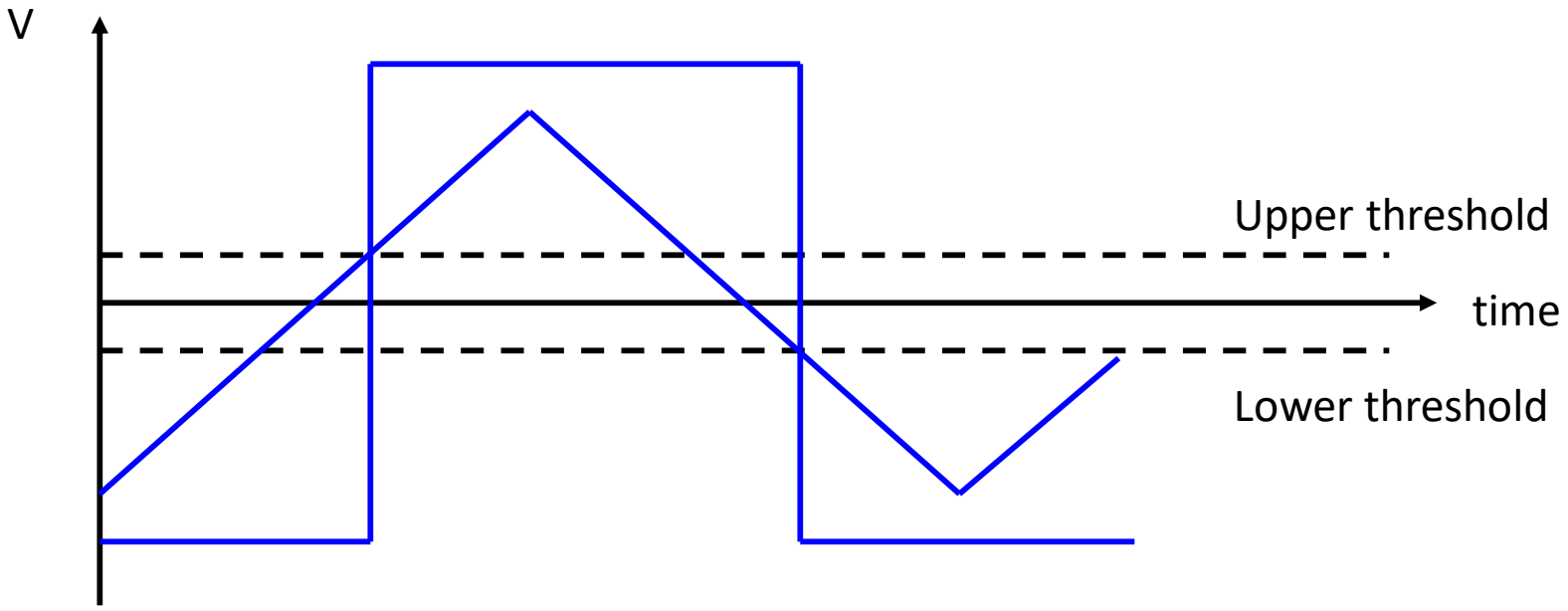
But,

$$V_{OUT} = \pm V_{SAT}$$

$$\therefore V_{THRESH} = \pm V_{SAT}\frac{R_1}{R_1 + R_2}$$

HYSTERESIS

- A comparator with hysteresis has a ‘safety margin’.
- One of two thresholds is used depending on the current output state.



MULTIVIBRATOR

Multivibrators are a group of regenerative circuits that are used extensively in timing applications. It is a wave shaping circuit which gives symmetric or asymmetric square output. It has two states either stable or quasi- stable depending on the type of multivibrator

MONOSTABLE MULTIVIBRATOR

Monostable multivibrator is one which generates a single pulse of specified duration in response to each external trigger signal. It has only one stable state. Application of a trigger causes a change to the quasi-stable state.An external trigger signal generated due to charging and discharging of the capacitor produces the transition to the original stable state

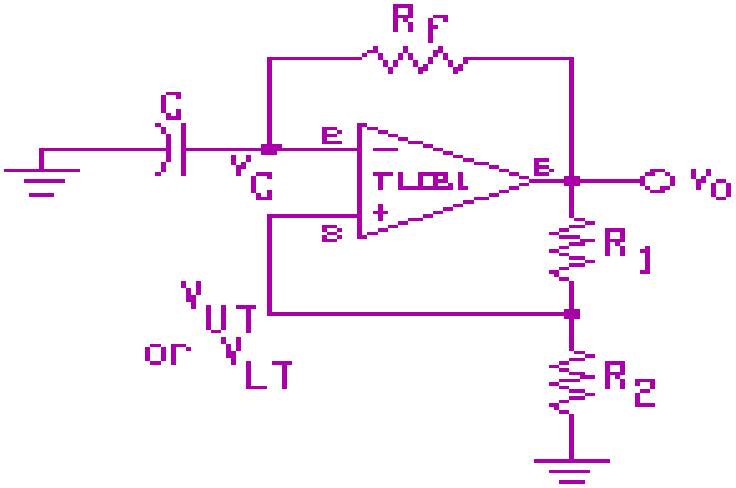
ASTABLE MULTIVIBRATOR

- Astable multivibrator is a free running oscillator having two quasi- stable states. Thus, there is oscillations between these two states and no external signal are required to produce the change in state

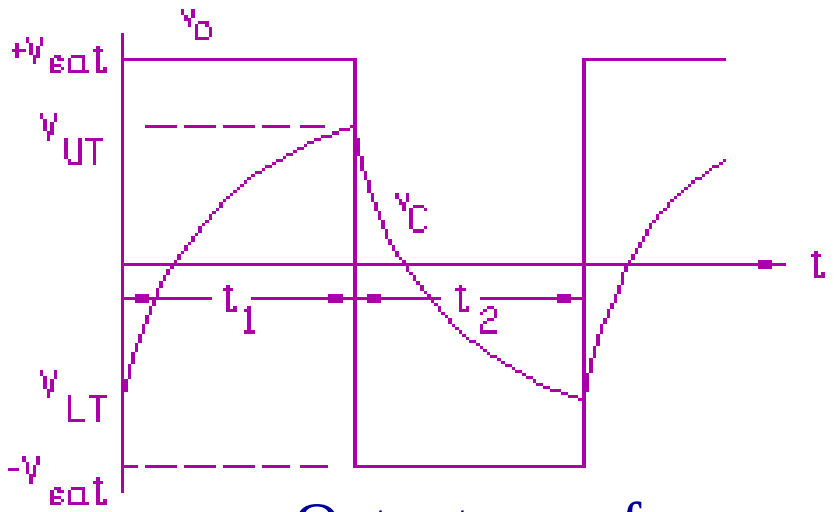
ASTABLE MULTIVIBRATOR

- Astable multivibrator is one that maintains a given output voltage level unless an external trigger is applied . Application of an external trigger signal causes a change of state, and this output level is maintained indefinitely until an second trigger is applied Thus, it requires two external triggers before it returns to its initial state

ASTABLE MULTIVIBRATOR OR RELAXATION OSCILLATOR



Circuit



Output waveform

Equations for Astable Multivibrator

$$V_{UT} = \frac{+V_{sat} R_2}{R_1 + R_2}; \quad V_{LT} = \frac{-V_{sat} R_2}{R_1 + R_2}$$

Assuming $|+V_{sat}| = |-V_{sat}|$

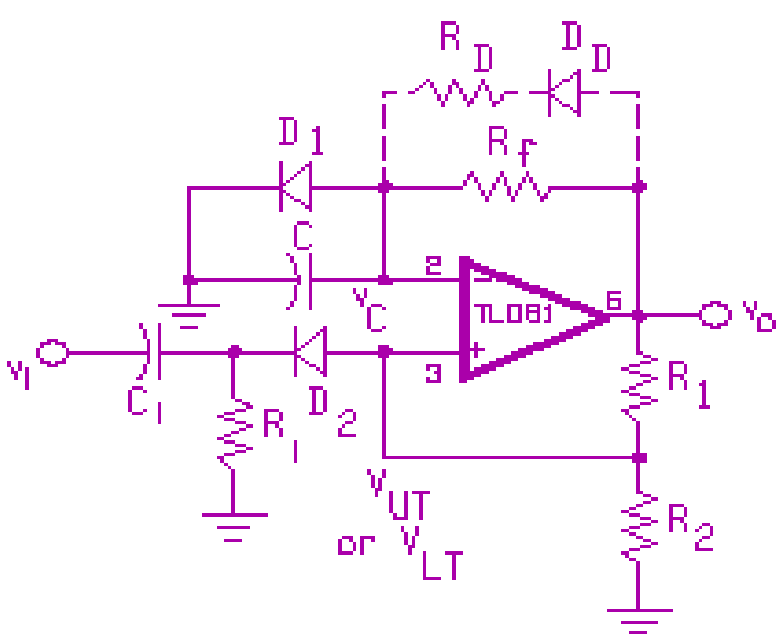
$$T = t_1 + t_2 = 2\tau \ln\left|\frac{R_1 + 2R_2}{R_1}\right|$$

where ☺ = $R_f C$

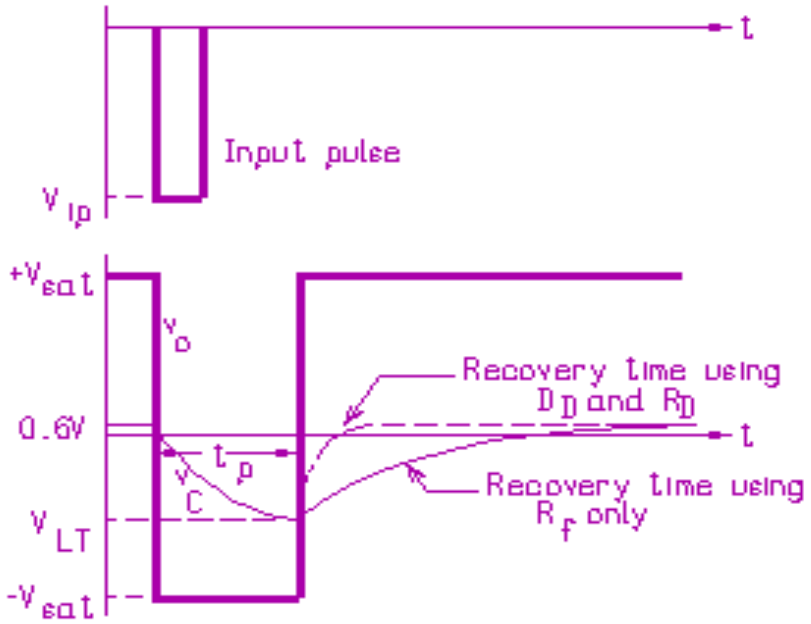
If R_2 is chosen to be $0.86R_1$, then $T = 2R_f C$ and

$$f = \frac{1}{2R_f C}$$

MONOSTABLE (ONE-SHOT) MULTIVIBRATOR



Circuit



Waveforms

NOTES ON MONOSTABLE MULTIVIBRATOR

- Stable state: $v_o = +V_{sat}$, $V_C = 0.6$ V
- Transition to timing state: apply a -ve input pulse such that $|V_{ip}| > |V_{UT}|$; $v_o = -V_{sat}$. Best to select R_iC_i ✂
  Timing state: C charges $t_p = R_f C \ln\left(\frac{|V_{sat}| + 0.6}{|V_{sat}| + V_{LT}}\right)$ through R_f. Width of timing pulse is: $0.1R_fC$.

- If we pick $R_2 = R_1/5$, then $t_p = R_fC/5$.
- Recovery state: $v_o = +V_{sat}$; circuit is not ready for retriggering until $V_C = 0.6$ V. The *recovery time* ☜ t_p. To speed up the recovery time, R_D ($= 0.1R_f$) & C_D can be added.

UNIT-2
TIMERS, A-D & D-A CONVERTERS

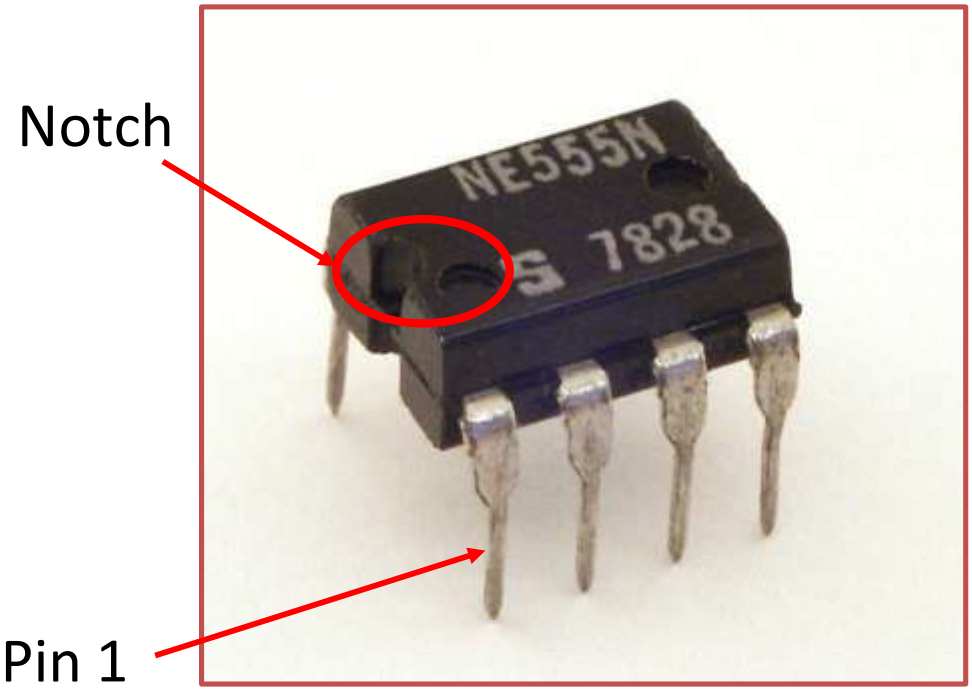
555 TIMER

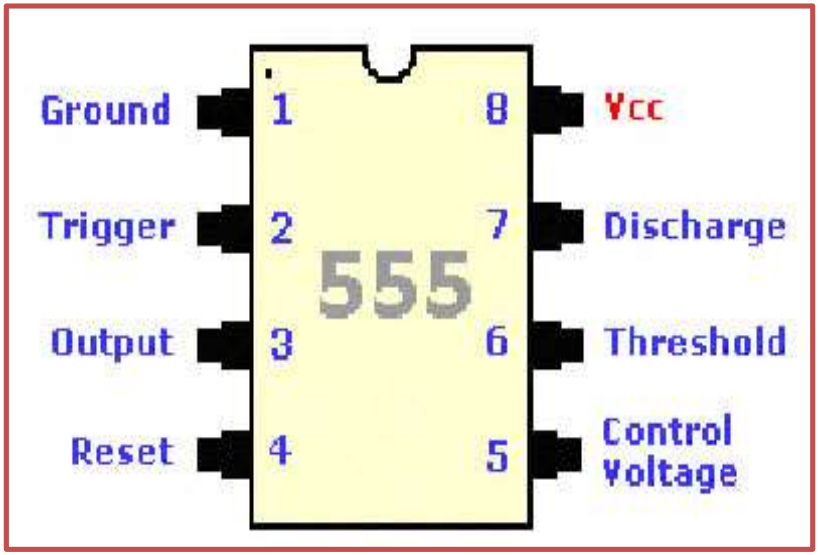
Introduction:

- The 555 Timer is one of the most popular and versatile integrated circuits ever produced!
- “Signetics” Corporation first introduced this device as the SE/NE 555 in early 1970.
- It is a combination of digital and analog circuits.
- It is known as the “time machine” as it performs a wide variety of timing tasks.
- Applications for the 555 Timer include:
  - Ramp and Square wave generator
  - Frequency dividers
  - Voltage-controlled oscillators
  - Pulse generators and LED flashers

555 TIMER- PIN DIAGRAM

The 555 timer is an 8-Pin D.I.L. Integrated Circuit or ‘chip’





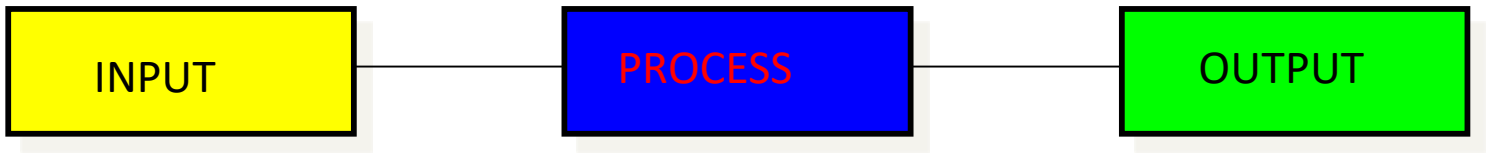
555 TIMER- PIN DESCRIPTION

Pin	Name	Purpose
1	GND	Ground, low level (0 V)
2	TRIG	OUT rises, and interval starts, when this input falls below 1/3 V_{CC}.
3	OUT	This output is driven to approximately 1.7V below $+V_{CC}$ or GND.
4	RESET	A timing interval may be reset by driving this input to GND, but the timing does not begin again until RESET rises above approximately 0.7 volts. Overrides TRIG which overrides THR.
5	CTRL	"Control" access to the internal voltage divider (by default, 2/3 V_{CC}).
6	THR	The interval ends when the voltage at THR is greater than at CTRL.
7	DIS	Open collector output; may discharge a capacitor between intervals. In phase with output.
8	V+, V_{CC}	Positive supply voltage is usually between 3 and 15 V.

555 TIMER

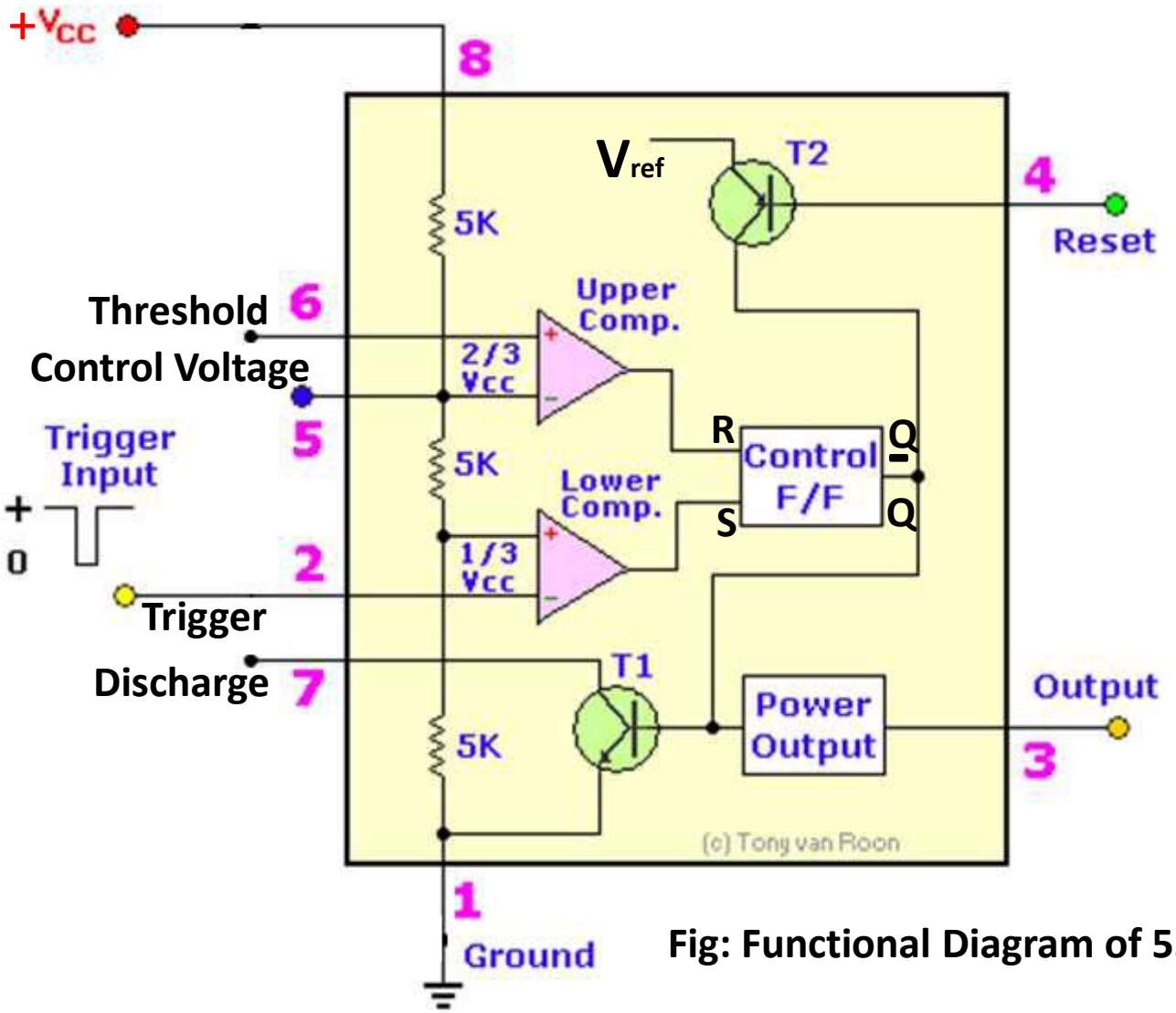
Description:

- Contains 25 transistors, 2 diodes and 16 resistors
- Maximum operating voltage 16V
- Maximum output current 200mA
- Best treated as a single component with required input and output



If you input certain signals they will be processed / controlled in a certain manner and will produce a known output.

FUNCTIONAL DIAGRAM OF 555 TIMER



Truth Table

S	R	Q	Q
0	0	No Change	
0	1	0	1
1	0	1	0
1	1	X	X

Fig: Functional Diagram of 555 Timer

FUNCTIONAL DIAGRAM OF 555 TIMER

Operation:

- The voltage divider has three equal 5K resistors. It divides the input voltage (V_{cc}) into three equal parts.
- The two comparators are op-amps that compare the voltages at their inputs and saturate depending upon which is greater.
  - The Threshold Comparator saturates when the voltage at the Threshold pin (pin 6) is greater than (2/3)V_{cc}.
  - The Trigger Comparator saturates when the voltage at the Trigger pin (pin 2) is less than (1/3)V_{cc}

FUNCTIONAL DIAGRAM OF 555 TIMER

- The flip-flop is a bi-stable device. It generates two values, a “high” value equal to V_{cc} and a “low” value equal to 0V.
  - When the Threshold comparator saturates, the flip flop is Reset (R) and it outputs a low signal at pin 3.
  - When the Trigger comparator saturates, the flip flop is Set (S) and it outputs a high signal at pin 3.
- The transistor is being used as a switch, it connects pin 7 (discharge) to ground when it is closed.
  - When Q is low, Q bar is high. This closes the transistor switch and attaches pin 7 to ground.
  - When Q is high, Q bar is low. This open the switch and pin 7 is no longer grounded

USES OF 555 TIMER

What the 555 timer is used for:

- To switch on or off an output after a certain time delay i.e. Games timer, Childs mobile, Exercise timer.

- To continually switch on and off an output i.e. warning lights, Bicycle indicators.

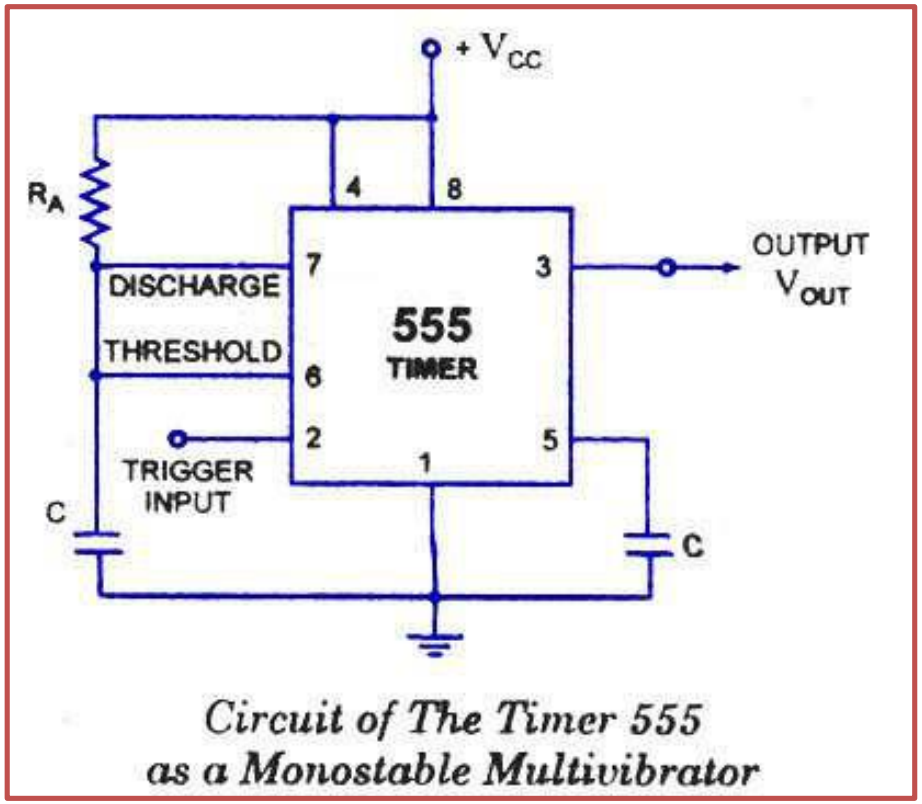
- As a pulse generator i.e. To provide a series of clock pulses for a counter.

555 TIMER OPERATING MODES

- The 555 has three operating modes:

    1. Monostable Multivibrator
    2. Astable Multivibrator
    3. Bistable Multivibratior

555 TIMER AS MONOSTABLE MULTIVIBRATOR



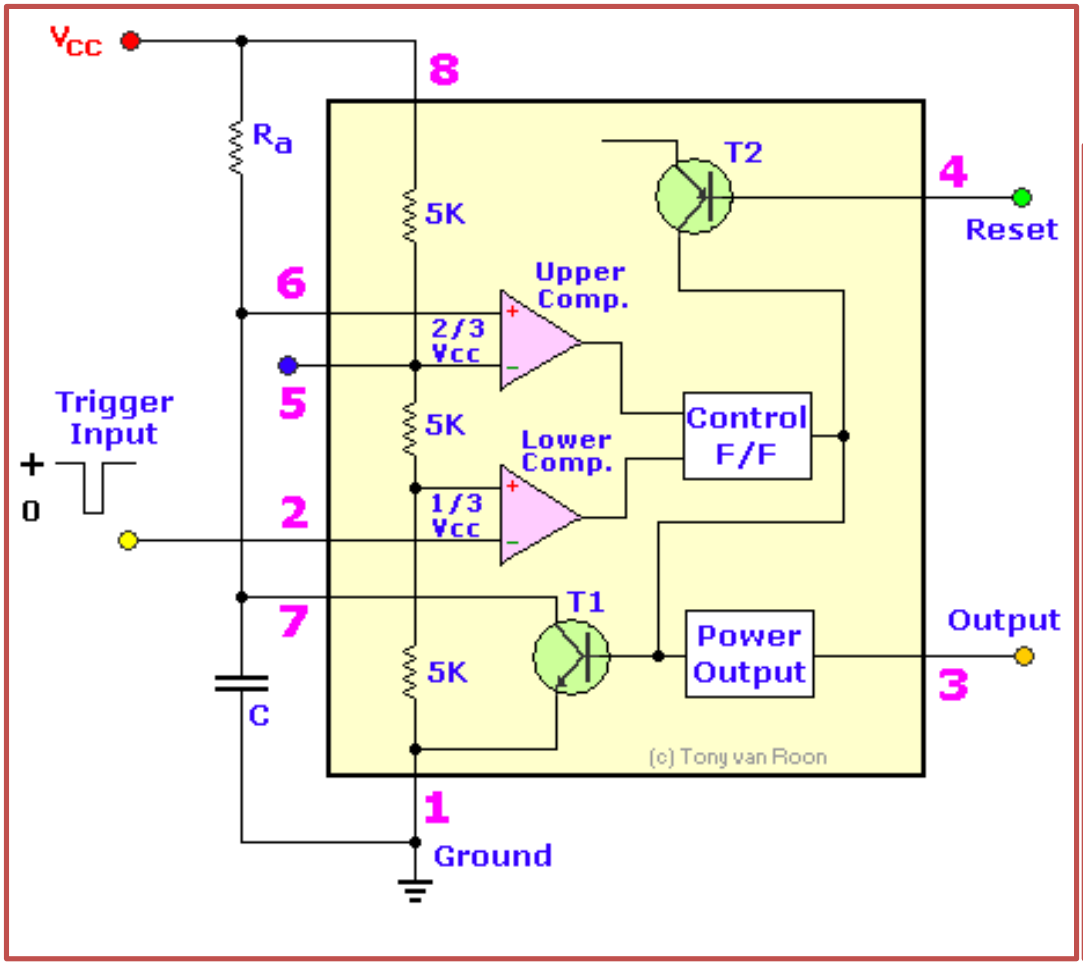
Circuit of The Timer 555 as a Monostable Multivibrator

Description:

- In the standby state, FF holds transistor Q**1** ON, thus clamping the external timing capacitor C to ground. The output remains at ground potential. i.e. Low.

- As the trigger passes through Vcc/3, the FF is set, i.e. Q bar=0, then the transistor Q_1 OFF and the short circuit across the timing capacitor C is released. As Q bar is low , output goes HIGH.

555 TIMER AS MONOSTABLE MULTIVIBRATOR



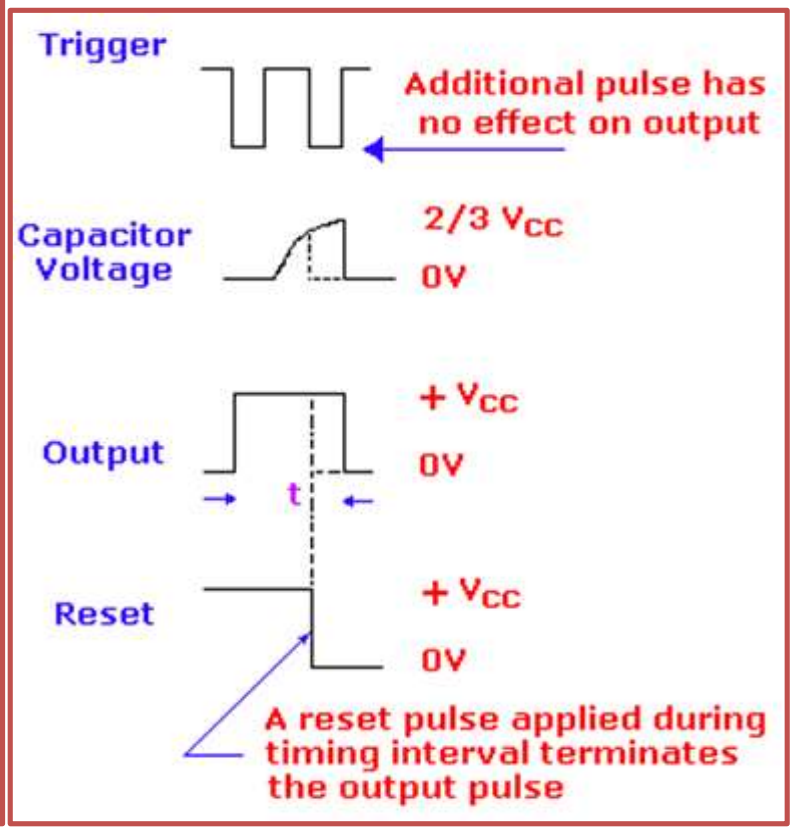


Fig (a): Timer in Monostable Operation with Functional Diagram
Fig (b): Output wave Form of Monostable

MONOSTABLE MULTIVIBRATOR-DESCRIPTION

- Voltage across it rises exponentially through R towards V_{cc} with a time constant RC.
- After Time Period T, the capacitor voltage is just greater than $2V_{cc}/3$ and the upper comparator resets the FF, i.e. R=1, S=0. This makes Q bar =1, C rapidly to ground potential.
- The voltage across the capacitor as given by,

$$v_C = V_{CC}(1 - e^{-t/RC})$$

at $t = T, v_C = \frac{2}{3}V_{CC}$

$$\frac{2}{3}V_{CC} = V_{CC}(1 - e^{-T/RC})$$

$$T = RC\ln(\frac{1}{3}) \Rightarrow T = 1.1RC\,\text{sec}$$

- If –ve going reset pulse terminal (pin 4) is applied, then transistor Q_2-> OFF, Q_1-> ON & the external timing capacitor C is immediately discharged.

BEHAVIOR OF THE MONOSTABLE MULTIVIBRATOR

- The monostable multivibrator is constructed by adding an external capacitor and resistor to a 555 timer.
- The circuit generates a single pulse of desired duration when it receives a trigger signal, hence it is also called a one-shot.
- The time constant of the resistor-capacitor combination determines the length of the pulse.

Uses of the Monostable Multivibrator

- Used to generate a clean pulse of the correct height and duration for a digital system
- Used to turn circuits or external components on or off for a specific length of time.
- Used to generate delays.
- Can be cascaded to create a variety of sequential timing pulses. These pulses can allow you to time and sequence a number of related operations.

Monostable Multivibrator

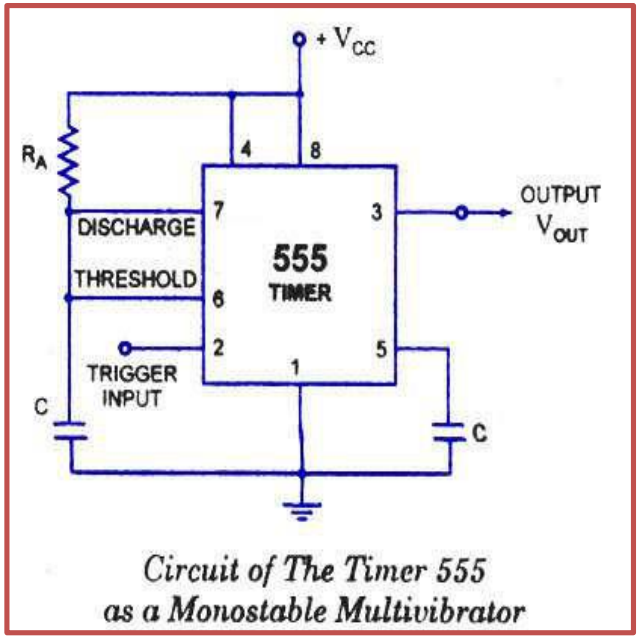
Problem:

In the monostable multivibrator of fig, R=100kΩ and the time delay T=100ms. Calculate the value of C ?

Solution:

$$T=1.1RC$$

$$\Rightarrow C=\frac{T}{1.1R}=\frac{100x10^{-3}}{1.1x100x10^{-3}}=0.9\mu F$$



Circuit of The Timer 555 as a Monostable Multivibrator

Applications in Monostable Mode

1. Missing Pulse Detector.
2. Linear Ramp Generator.
3. Frequency Divider.
4. Pulse Width Modulation.

1.Missing Pulse Detector

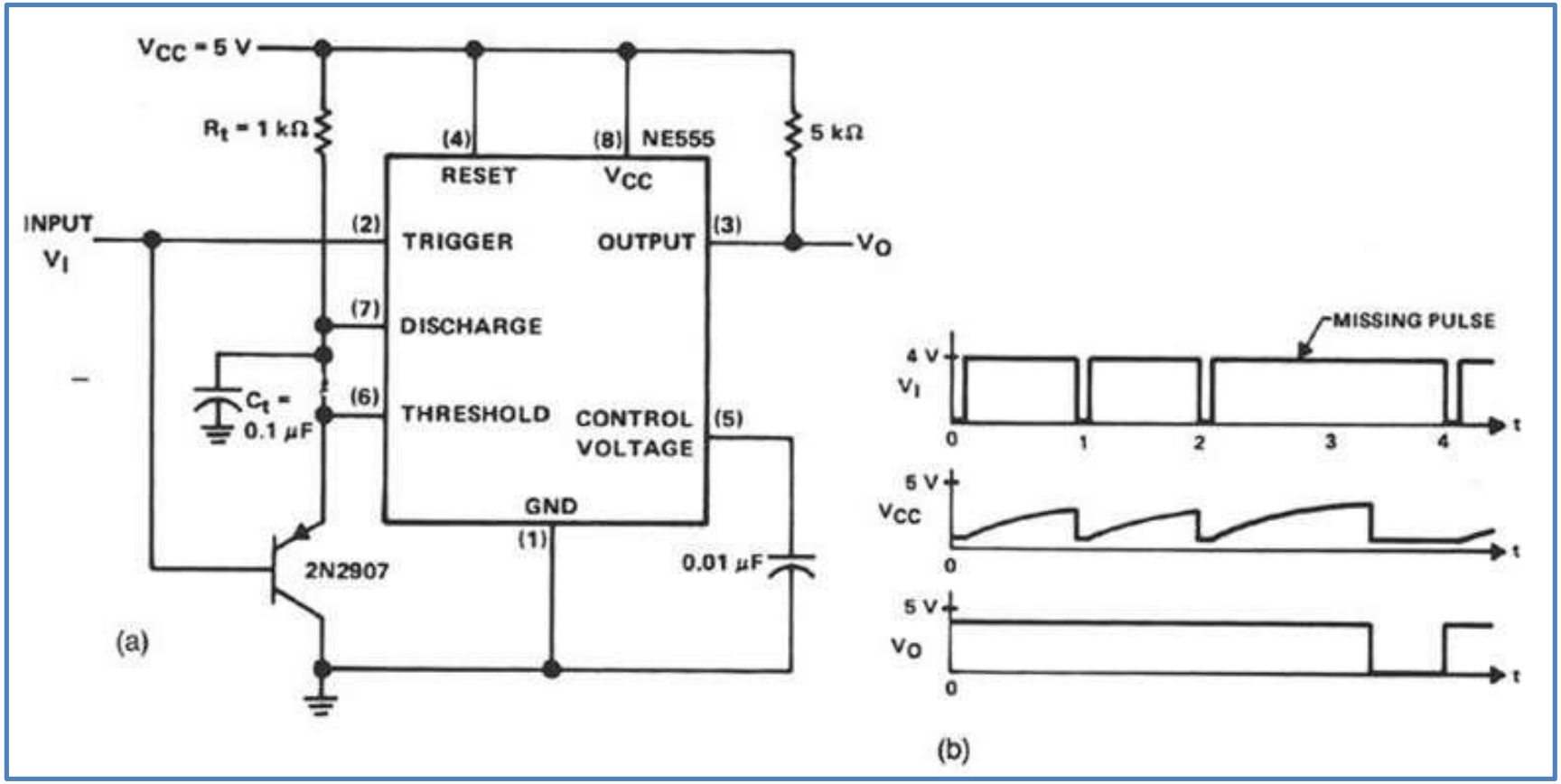


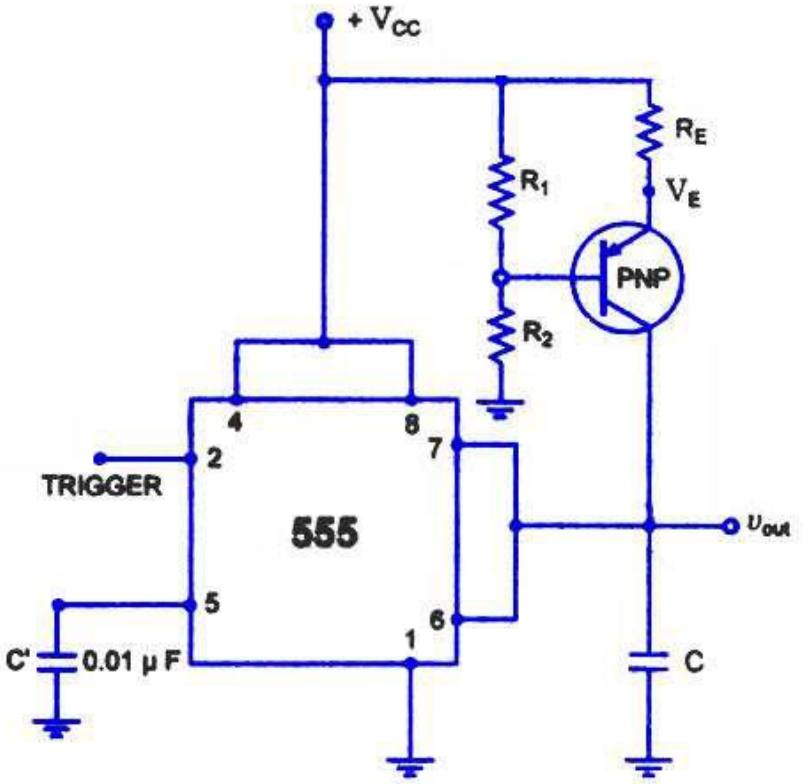
Fig (a) : A missing Pulse Detector Monostable Circuit

Fig (b) : Output of Missing Pulse Detector

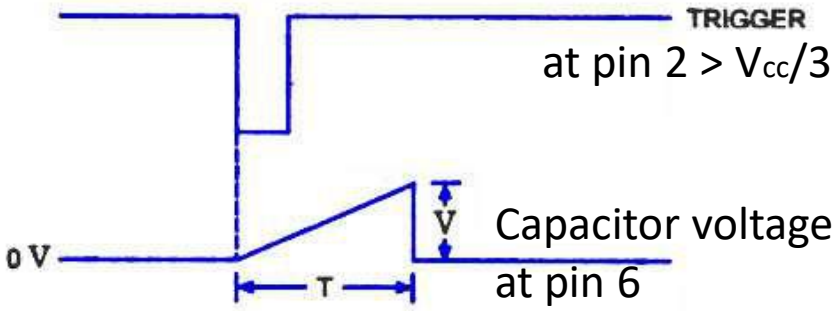
Missing Pulse Detector- Description

- When input trigger is Low, emitter-base diode of Q is forwarded biased capacitor is clamped to 0.7v(of diode), output of timer is HIGH width of T o/p of timer > trigger pulse width.
- T=1.1RC select R & C such that T > trigger pulse.
- Output will be high during successive coming of input trigger pulse. If one of the input trigger pulse missing trigger i/p is HIGH, Q is cut off, timer acts as normal monostable state.
- It can be used for speed control and measurement.

2.Linear Ramp Generator



Circuit

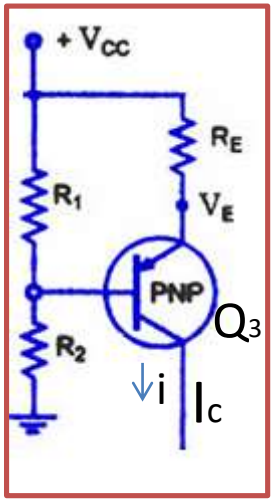


Trigger and Ramp Waveforms

Ramp Generator Using The Timer 555

Linear Ramp Generator- Description

Analysis:



Applying KVL around base-emitter loop of Q_3

$$\frac{R_1}{R_1+R_2}V_{CC}-V_{BE}=I_E R_E=(I_C+I_B)R_E=(I_B\beta+I_B)R_E=(1+\beta)I_B R_E=\beta I_B R_E\approx I_C R_E=i R_E$$

$$(\because I_C=i)$$

$$i R_E=\frac{R_1V_{CC}-V_{BE}(R_1+R_2)}{R_1+R_2}\Rightarrow i=\frac{R_1V_{CC}-V_{BE}(R_1+R_2)}{R_E(R_1+R_2)}$$

Voltage Capacitor,

$$v_c=\frac{1}{C}\int_0^t idt=\frac{1}{C}\int_0^t\{\frac{R_1V_{CC}-V_{BE}(R_1+R_2)}{R_E(R_1+R_2)}\}dt=\frac{1}{C}\{\frac{R_1V_{CC}-V_{BE}(R_1+R_2)}{R_E(R_1+R_2)}\}t$$

When v_c becomes $\frac{2}{3}V_{CC}$ at T,

$$\frac{2}{3}V_{CC}=\frac{R_1V_{CC}-V_{BE}(R_1+R_2)}{CR_E(R_1+R_2)}T\quad\Rightarrow\quad\therefore T=\frac{\frac{2}{3}V_{CC}CR_E(R_1+R_2)}{R_1V_{CC}-V_{BE}(R_1+R_2)}$$

3.Frequency Divider

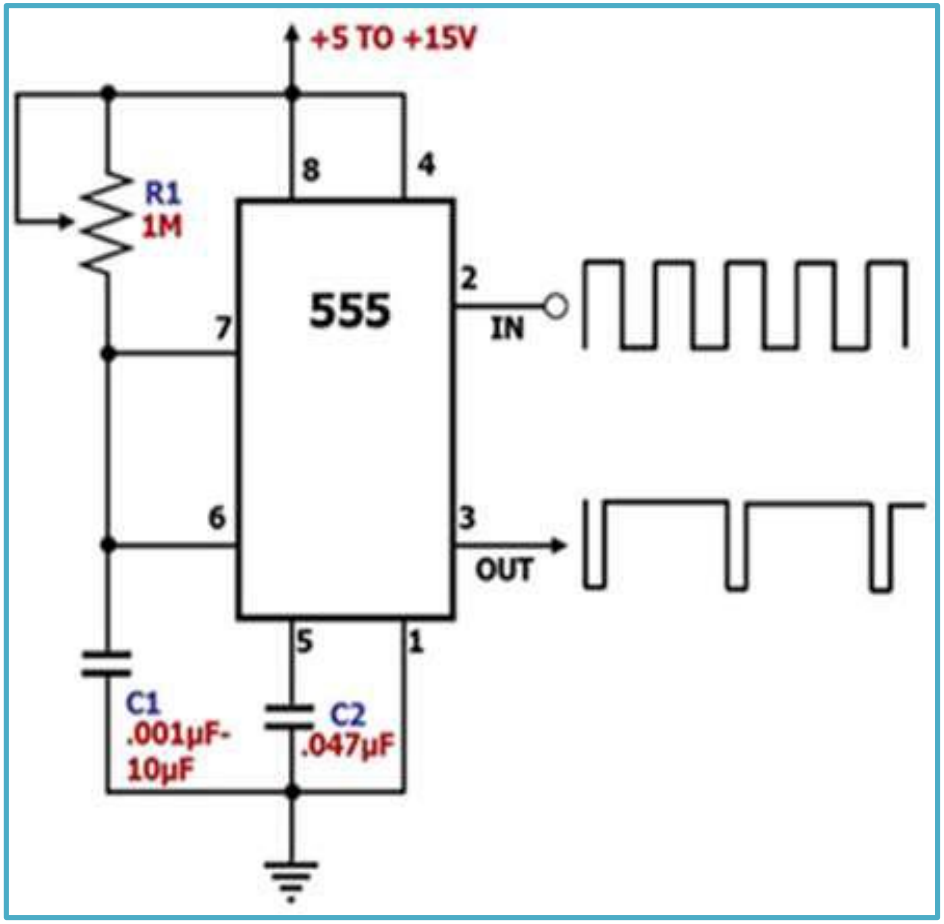


Fig: Diagram of Frequency Divider

Description:

A continuously triggered monostable circuit when triggered by a square wave generator can be used as a frequency divider, if the timing interval is adjusted to be longer than the period of the triggering square wave input signal.

The monostable multivibrator will be triggered by the first negative going edge of the square wave input but the output will remain HIGH(because of greater timing interval) for next negative going edge of the input square wave as shown fig.

4.Pulse Width Modulation

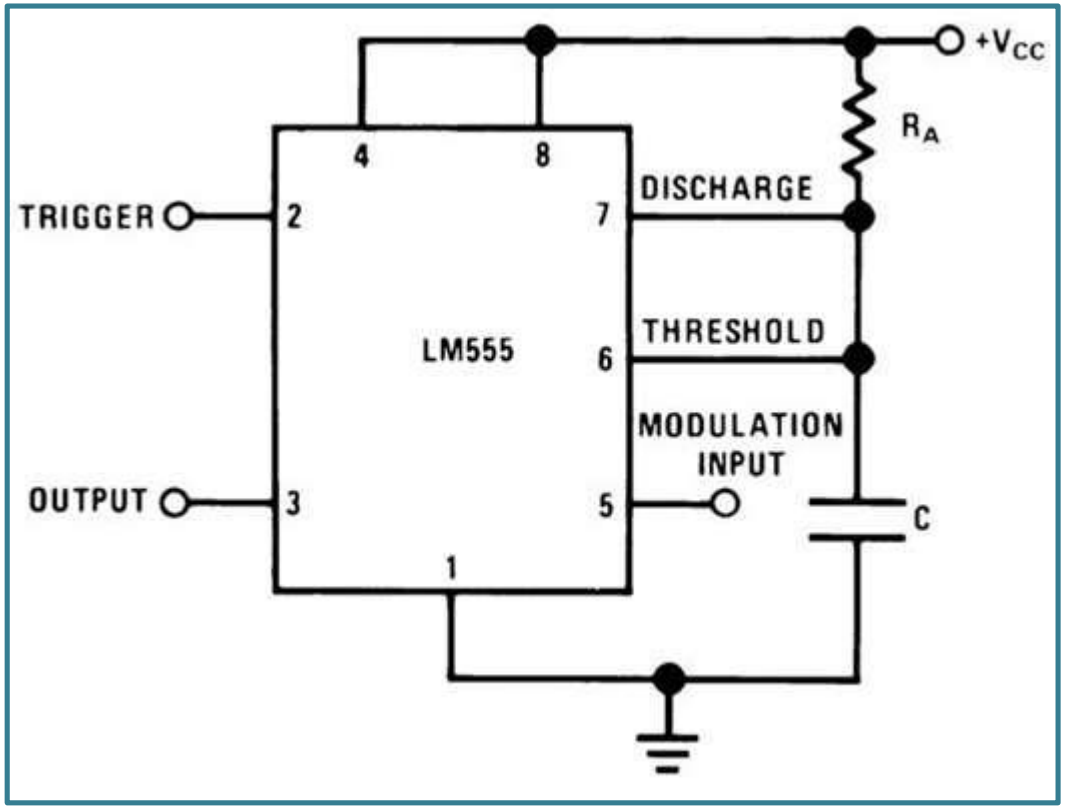


Fig a: Pulse Width Modulation

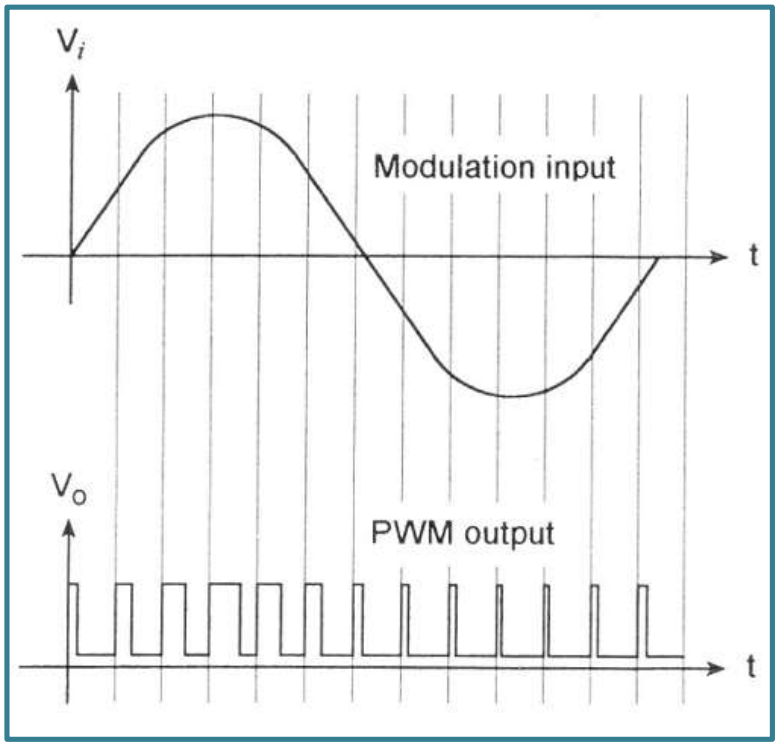


Fig b: PWM Wave Forms

Pulse Width Modulation- Description

- The charging time of capacitor is entirely depend upon $2V_{cc}/3$. When capacitor voltage just reaches about $2V_{cc}/3$ output of the timer is coming from HIGH to Low level.
- We can control this charging time of the capacitor by adding continuously varying signal at the pin-5 of the 555 timer which is denoted as control voltage point. Now each time the capacitor voltage is compared control voltage according to the o/p pulse width change. So o/p pulse width is changing according to the signal applied to control voltage point. So the output is pulse width modulated form.

Pulse Width Modulation

Practical Representation

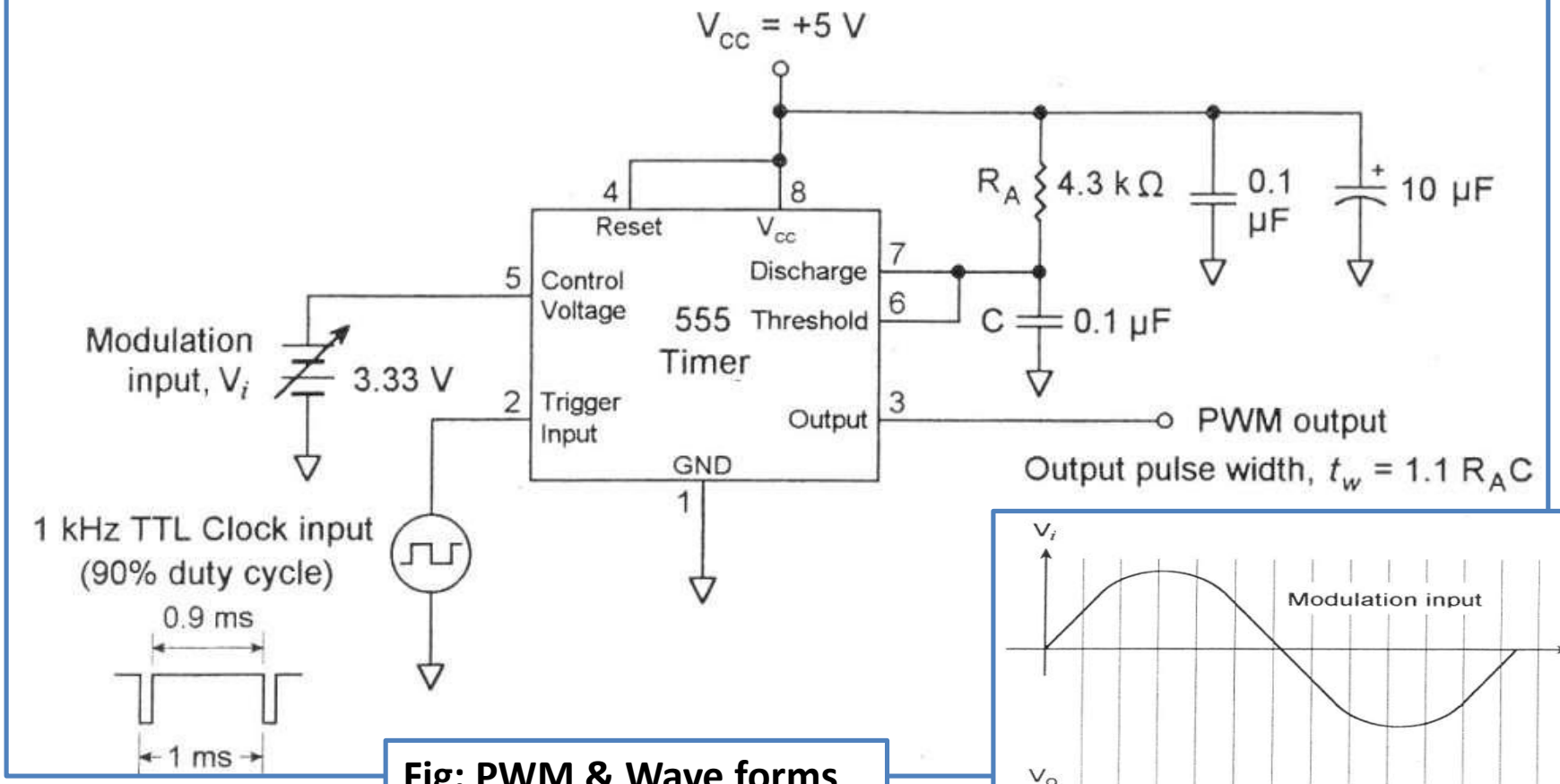


Fig: PWM & Wave forms

Astable Multivibrator

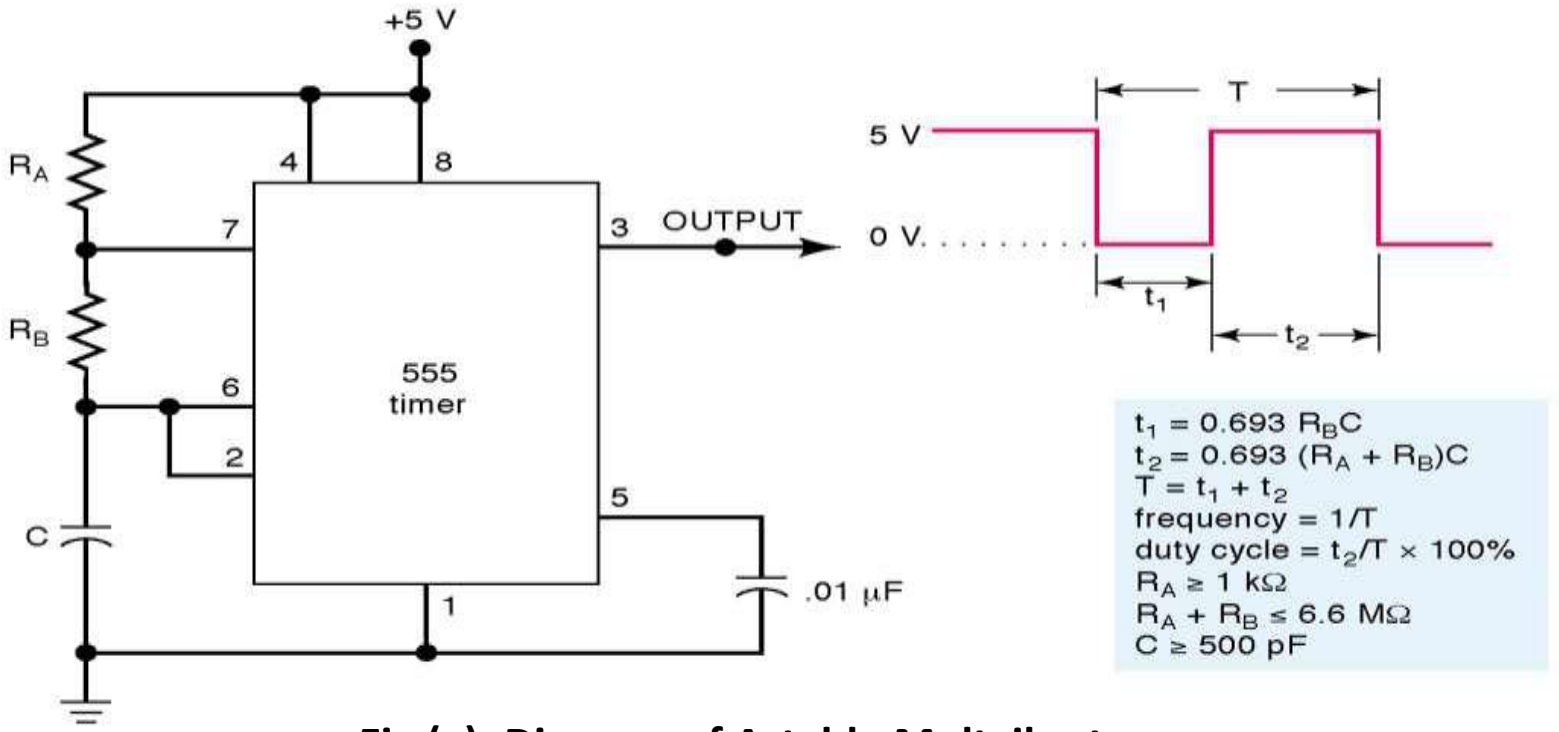


Fig (a): Diagram of Astable Multvibrator

1 – Ground
2 – Trigger
3 – Output
4 – Reset (Set HIGH for normal operation)
5 – FM Input (Tie to gnd via bypass cap)
6 – Threshold
7 – Discharge
8 – Voltage Supply (+5 to +15 V)

Astable Multivibrator

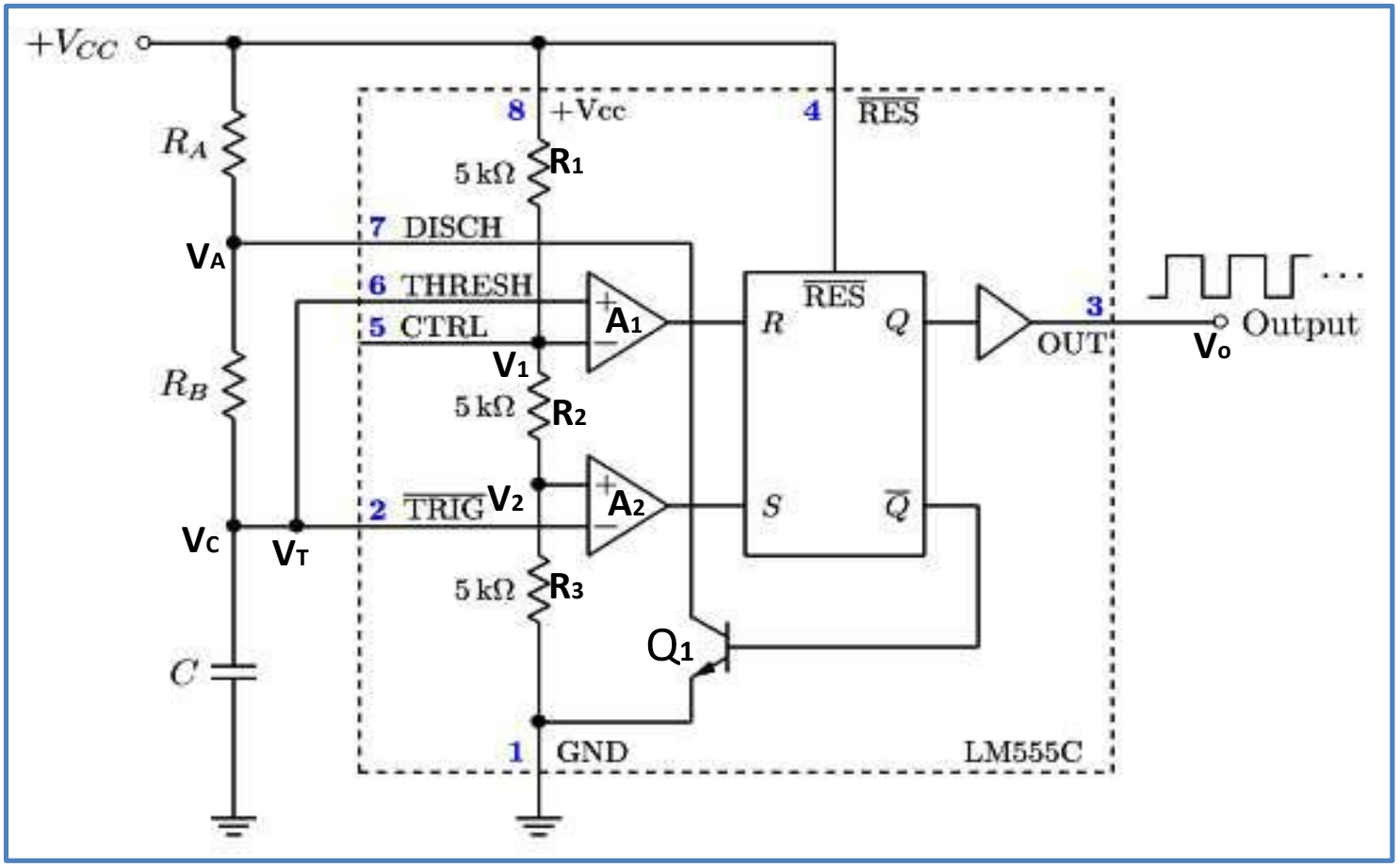


Fig (b): Functional Diagram of Astable Multivibrator using 555 Timer

Astable Multivibrator- Description

- Connect external timing capacitor between trigger point (pin 2) and Ground.
- Split external timing resistor R into R_A & R_B, and connect their junction to discharge terminal (pin 7).
- Remove trigger input, monostable is converted to Astable multivibrator.
- This circuit has no stable state. The circuits changes its state alternately. Hence the operation is also called free running oscillator.

Astable 555 Timer Block Diagram Contents

- Resistive voltage divider (equal resistors) sets threshold voltages for comparators

  $V_1 = V_{TH} = 2/3\ V_{CC}$ $\quad\quad$ $V_2 = V_{TL} = 1/3\ V_{CC}$

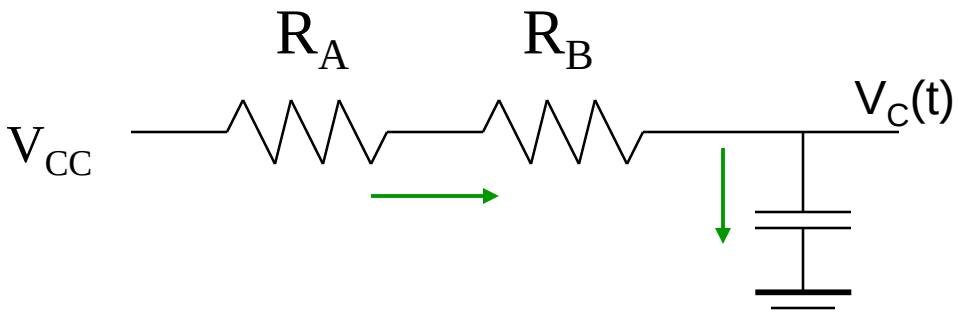
- Two Voltage Comparators
  - For A_1, if $V_+ > V_{TH}$ then R =HIGH
  - For A_2, if $V_- < V_{TL}$ then S = HIGH

- RS FF
  - If S = HIGH, then FF is SET, $\bar{Q}$ = LOW, Q_1 OFF, V_{OUT} = HIGH
  - If R = HIGH, then FF is RESET, $\bar{Q}$ = HIGH, Q_1 ON, V_{OUT} = LOW

- Transistor Q_1 is used as a Switch

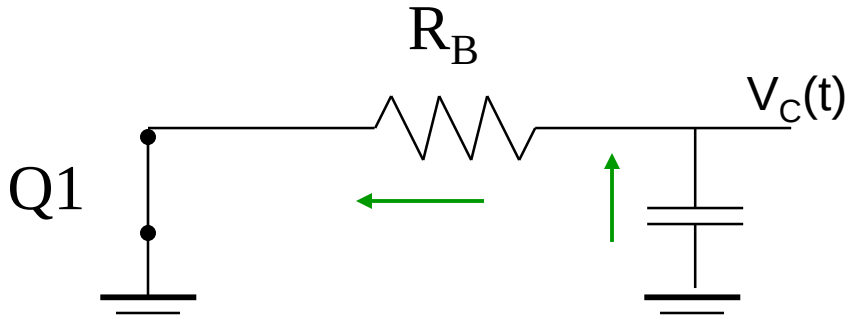
Operation of a 555 Astable

1) Assume initially that the capacitor is discharged.
   a) For A_1, $V_+ = V_C = 0V$ and for A_2, $V_- = V_C = 0V$, so R=LOW, S=HIGH, $\bar{Q}$ = LOW , Q1 OFF, $V_{OUT} = V_{CC}$
   b) Now as the capacitor charges through R_A & R_B, eventually $V_C > V_{TL}$ so R=LOW & S=LOW.
      FF does not change state.



Operation of a 555 Astable Continued……

2) Once $V_C \geq V_{TH}$
   a) R=HIGH, S=LOW, $\bar{Q}$= HIGH ,Q1 ON, $V_{OUT} = 0$
   b) Capacitor is now discharging through R_B and Q_1 to ground.
   c) Meanwhile at FF, R=LOW & S=LOW since $V_C < V_{TH}$.

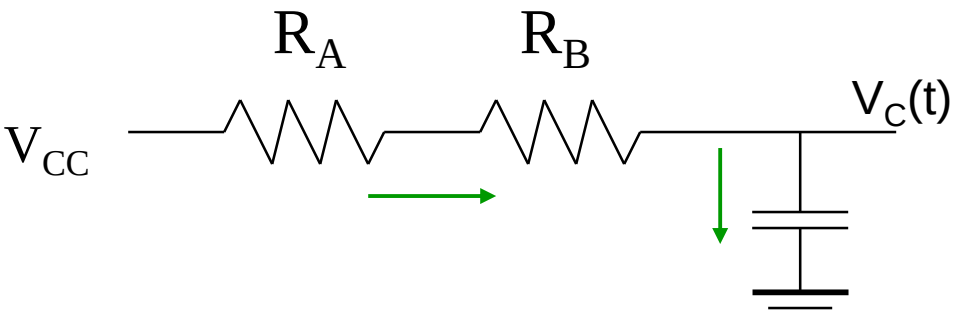


Operation of a 555 Astable Continued…..

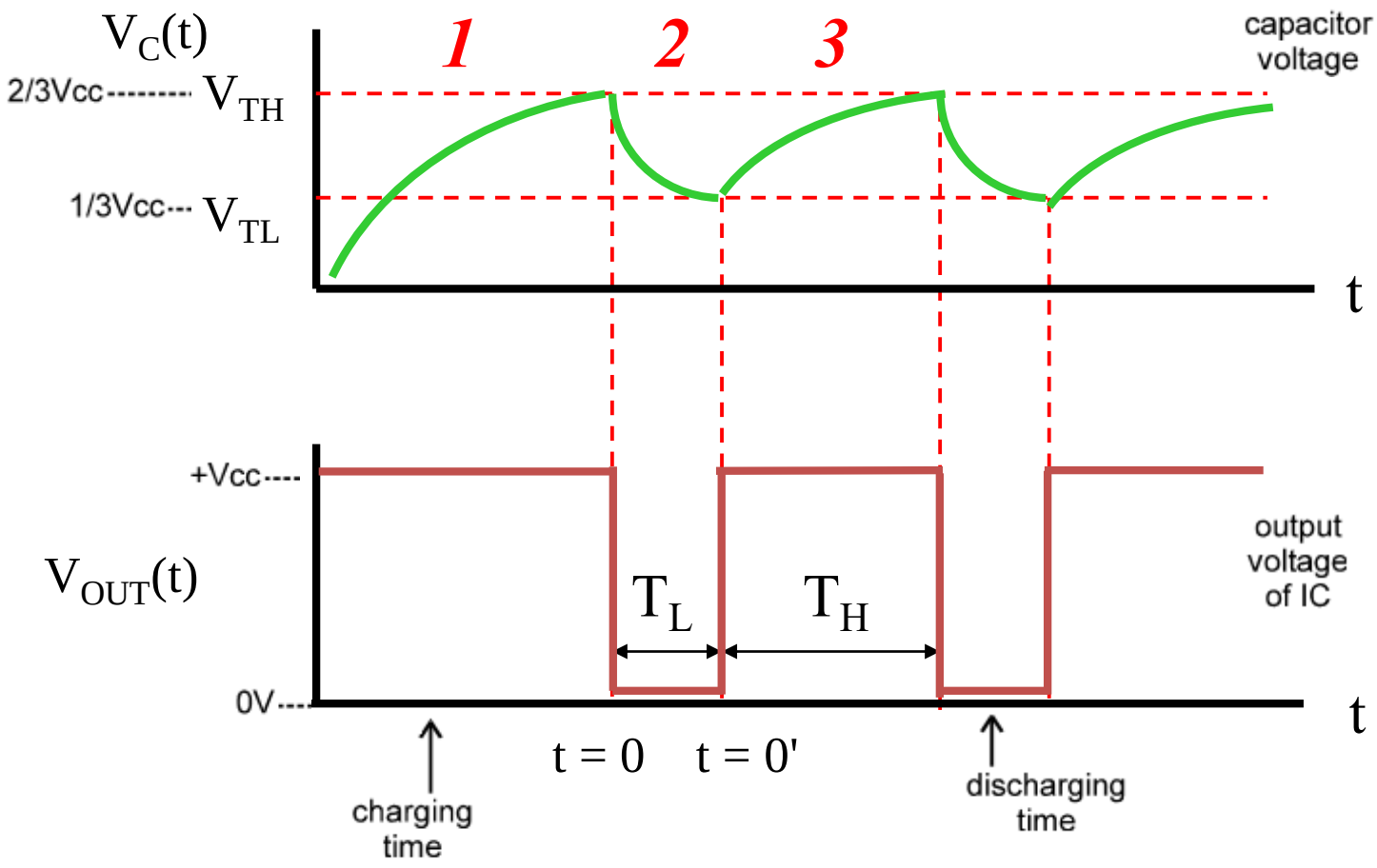
3) Once $V_C < V_{TL}$

   a) R=LOW, S=HIGH, $\overline{Q}$ = LOW , Q1 OFF, $V_{OUT} = V_{CC}$

   b) Capacitor is now charging through R_A & R_B again.



Timing Diagram of a 555 Astable



Astable Multivibrator- Analysis

The capacitor voltage for a low pass RC circuit subjected to a step input of V_{cc} volts is given by, $v_c = V_{CC}(1 - e^{-t/RC})$

The time t_1 taken by the circuit to change from 0 to $2V_{cc}/3$ is, $V_C = \frac{2}{3}V_{CC}$

$$\frac{2V_{CC}}{3} = V_{CC}(1 - e^{-t1/RC}) \Rightarrow t_1 = 1.09RC$$

The time t_2 to charge from 0 to $v_{cc}/3$ is $V_C = \frac{1}{3}V_{CC}$

$$\frac{V_{CC}}{3} = V_{CC}(1 - e^{-t2/RC}) \Rightarrow t_2 = 0.405RC$$

So the time to change from $V_{cc}/3$ to $2V_{cc}/3$ is, $t_{HIGH} = t_1 - t_2 = 1.09RC - 0.405RC = 0.69RC$

So, for the given circuit, $t_{HIGH} = 0.69(R_A + R_B)C$ ..... Charging time

The output is low while the capacitor discharges from $2V_{cc}/3$ to $V_{cc}/3$ and the voltage across the capacitor is given by, $\frac{V_{CC}}{3} = \frac{2}{3}V_{CC}e^{-t/RC}$

Contd….

Astable Multivibrator- Analysis

After solving, we get, t=0.69RC

For the given circuit, $t_{LOW} = 0.69\,R_B C$ ..... Discharging time

Both R_A and R_B are in the charge path, but only R_B is in the discharge path.

$\therefore$ The total time period,

$$T = t_{HIGH} + t_{LOW} = 0.69(R_A + R_B)C + 0.69\,R_B C$$

$$\Rightarrow T = 0.69[(R_A + R_B)C + R_B C] = 0.69(R_A + R_B + R_B)C = 0.69(R_A + 2R_B)C$$

Frequency, $f = \frac{1}{T} = \frac{1}{0.69(R_A + 2R_B)C} = \frac{1.45}{(R_A + 2R_B)C}$ .....1.45 is Error Constant

Duty Cycle,

$$\%D = \frac{t_{HIGH}}{T} X100 = \frac{0.69(R_A + R_B)C}{0.69(R_A + 2R_B)C} X100 = \frac{(R_A + R_B)}{(R_A + 2R_B)} X100$$

$$\%D = \frac{t_{LOW}}{T} X100 = \frac{0.69\,R_B C}{0.69(R_A + 2R_B)C} X100 = \frac{R_B}{(R_A + 2R_B)} X100$$

Behavior of the Astable Multivibrator

- The astable multivibrator is simply an oscillator. The astable multivibrator generates a continuous stream of rectangular off-on pulses that switch between two voltage levels.
- The frequency of the pulses and their duty cycle are dependent upon the RC network values.
- The capacitor C charges through the series resistors R_A and R_B with a time constant $(R_A + R_B)C$.
- The capacitor discharges through R_B with a time constant of R_BC

Uses of the Astable Multivibrator

- Flashing LED's
- Pulse Width Modulation
- Pulse Position Modulation
- Periodic Timers
- Uses include LEDs, pulse generation, logic clocks, security alarms and so on.

Applications in Astable Mode

1. Square Generator
2. FSK Generator
3. Pulse Position Modulator

1.Square Generator

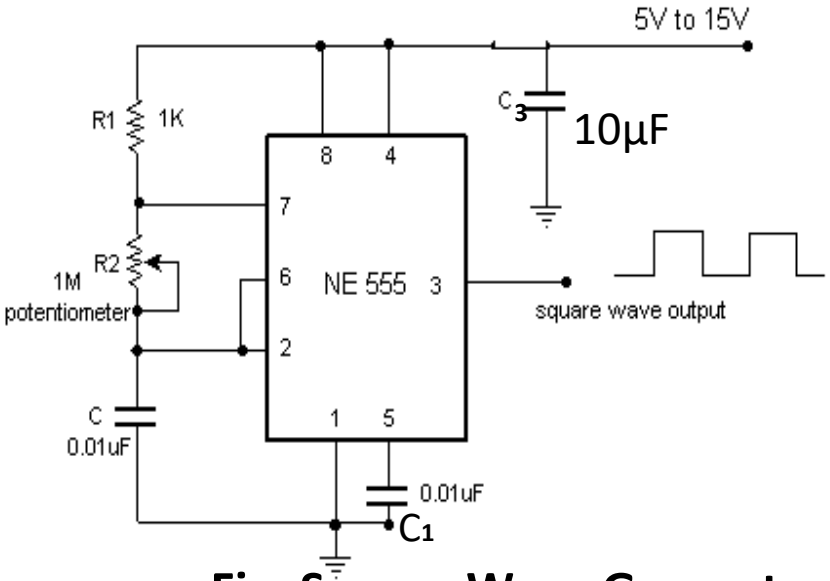


Fig: Square Wave Generator

$$DutyCycle = \frac{(R_1 + R_2)}{(R_1 + 2R_2)} X100 = 50\%$$

$$Here\ R_1 = 0$$

- To avoid excessive discharge current through Q_1 when $R_1=0$ connect a diode across R_2, place a variable R in place of R_1.
- Charging path R_1 & D; Discharging path R_2 & pin 7.

2. FSK Generator

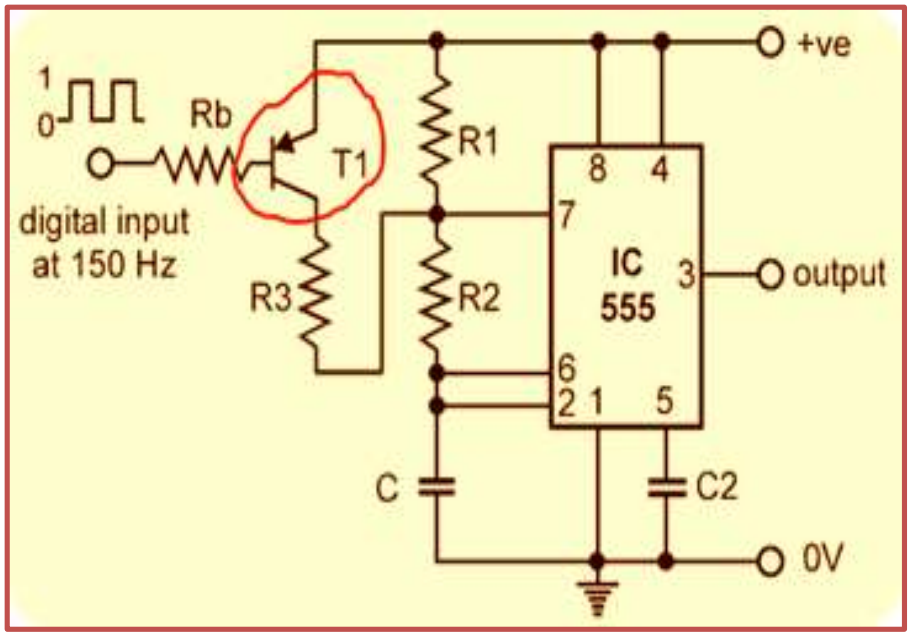


Fig: FSK Generator

Description:

- In digital data communication, binary code is transmitted by shifting a carrier frequency between two preset frequencies. This type of transmission is called Frequency Shift Keying (FSK) technique.

Contd…..

FSK Generator

- A 555 timer is astable mode can be used to generate FSK signal.
- When input digital data is HIGH, T_1 is OFF & 555 timer works as normal astable multivibrator.

The frequency of the output wave form given by,

$$f_o = \frac{1.45}{(R_1 + 2R_2)C}$$

When input digital is LOW, Q_1 is ON then R_3 parallel R_1

$$\therefore f_o = \frac{1.45}{(R_3 \| R_1 + 2R_2)C}$$

2. Pulse Position Modulator

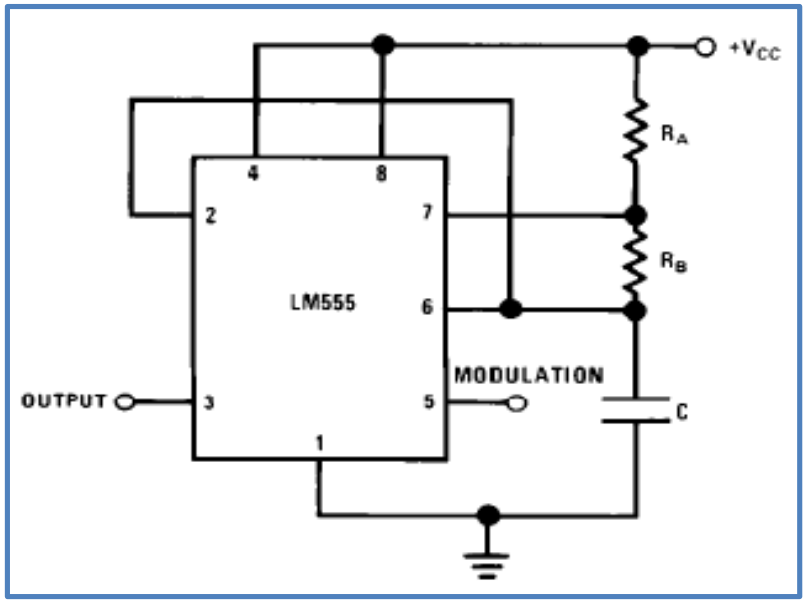


Fig (a): Pulse position Modulator

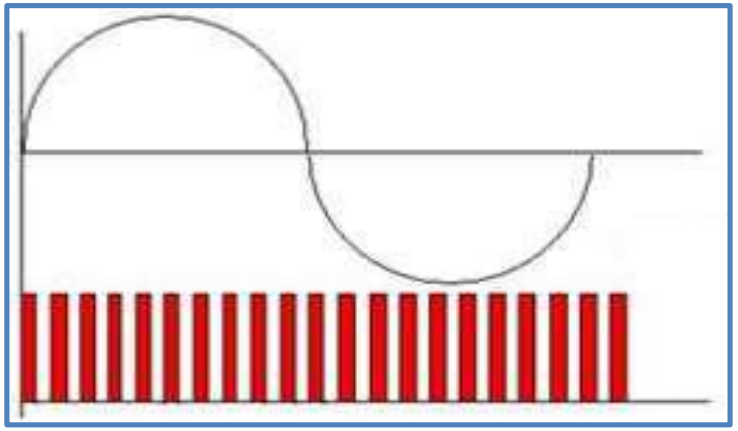


Fig (b): Output Wave Form of PPM

Description:

- The pulse position modulator can be constructed by applying a modulating signal to pin 5 of a 555 timer connected for astable operation.
- The output pulse position varies with the modulating signal, since the threshold voltage and hence the time delay is varied.
- The output waveform that the frequency is varying leading to pulse position modulation.

Astable Multivibrator

Problem:

In the astable multivibrator of fig, RA=2.2KΩ, RB=3.9K Ω and C=0.1μF. Determine the positive pulse width t_H, negative pulse width t_{Low}, and free-running frequency f_o.

Solution:

$$t_{HIGH} = 0.69(R_A + R_B)C = 0.69(2.2K\Omega + 3.9K\Omega)(0.1X10^{-6}) = 0.421ms$$

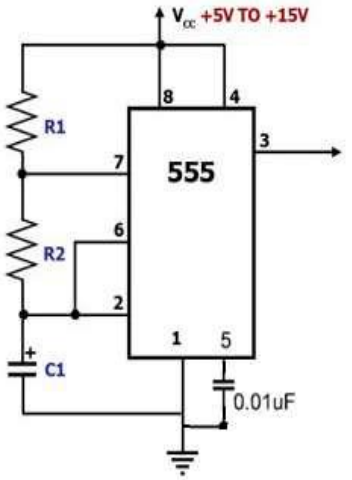
$$t_{LOW} = 0.69\,R_B C = 0.69(3.9K\Omega)(0.1X10^{-6}) = 0.269ms$$

$$f_o = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C} = ?$$

Duty Cycle,

$$\%D = \frac{t_{HIGH}}{T} X100 = \frac{(R_A + R_B)}{(R_A + 2R_B)} X100 = \frac{2.2K\Omega + 3.9\text{K}\Omega}{2.2K\Omega + 2X\,3.9K\Omega} X100 = ?$$

$$\%D = \frac{t_{LOW}}{T} X100 = \frac{R_B}{(R_A + 2R_B)} X100 = \frac{3.9\text{K}\Omega}{2.2K\Omega + 2X\,3.9K\Omega} X100 = ?$$



Example: Design a 555 Oscillator to produce an approximate square-wave at 40 KHz. Let C > 470 pF.

One Possible Solution:

F=40KHz; T=25µs; $t_1=t_2=12.5\mu s$

For a square-wave $\mathbf{R_A << R_B}$; Let R_A=1K and R_B=10K

$t_1=0.693(R_B)(C)$; 12.5µs=0.693(10K)(C); C=1800pF

$T=0.693(R_A+2R_B)C$: T=0.693(1K+20K)1800pF

T=26.2µs; F=1/T; F=38KHz (almost square-wave).

Example: A 555 oscillator can be combined with a J-K FF to produce a 50% duty-cycle signal. Modify the above circuit to achieve a 50% duty-cycle, 40 KHz signal.

One Possible Solution:

Reduce by half the 1800pF. This will create a T=13.1µs or F=76.35 KHz (almost square-wave). Now, take the output of the 555 Timer and connect it to the CLK input of a J-K FF wired in the toggle mode (J and K inputs connected to +5V). The result at the Q output of the J-K FF is a perfect 38.17 KHz square-wave.

Comparison of Multivibrator Circuits

Monostable Multivibrator	Astable Multivibrator
1. It has only one stable state	1. There is no stable state.
2. Trigger is required for the operation to change the state.	2. Trigger is not required to change the state hence called free running.
3. Two comparators R and C are necessary with IC 555 to obtain the circuit.	3. Three components R_A, R_B and C are necessary with IC 555 to obtain the circuit.
4. The pulse width is given by T=1.1RC Seconds	4. The frequency is given by, $f_o = \frac{1}{T} = \frac{1.45}{(R_A + 2R_B)C}$
5. The frequency of operation is controlled by frequency of trigger pulses applied.	5. The frequency of operation is controlled by R_A, R_B & C.
6. The applications are timer, frequency divider, pulse width modulation etc…	6. The applications are square wave generator, flasher, voltage controlled oscillator, FSK Generator etc..

Schmitt Trigger

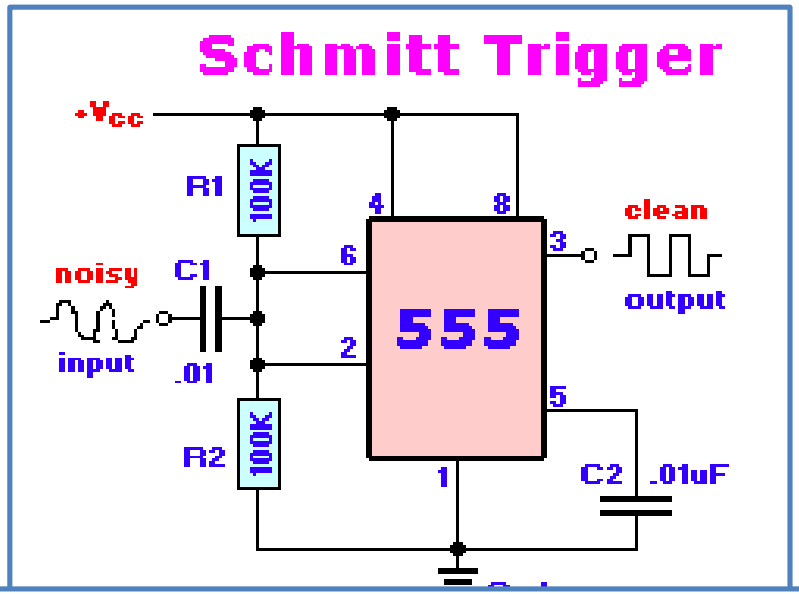


Fig (a): Circuit Diagram of Schmitt Trigger

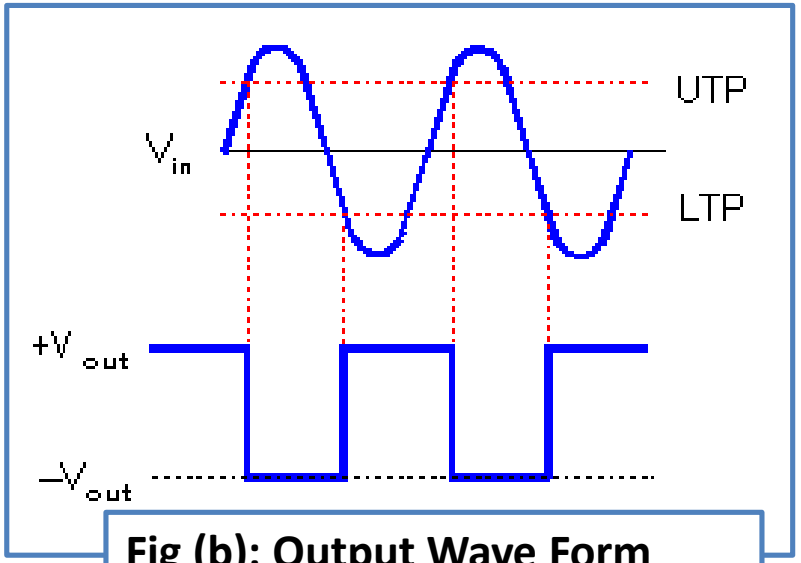


Fig (b): Output Wave Form

The use of 555 timer as a Schmitt trigger is shown in fig. Here the two internal comparators are tied together and externally biased at $V_{cc}/2$ through R_1 and R_2. Since the upper comparator will trip at $2V_{cc}/3$ and lower comparator at $V_{cc}/3$, the bias provided by R_1 and R_2 is centered within these two thresholds.

Features of IC 555 Timer

The Features of IC 555 Timer are:

1. The 555 is a monolithic timer device which can be used to produce accurate and highly stable time delays or oscillation. It can be used to produce time delays ranging from few microseconds to several hours.

2. It has two basic operating modes: monostable and astable.

3. It is available in three packages: 8-pin metal can, 8-pin mini DIP or a 14-pin. A 14-pin package is IC 556 which consists of two 555 times.

Features of IC 555 Timer

4. The NE 555(signetics) can operate with a supply voltage in the range of 4.5v to 18v and output currents of 200mA.

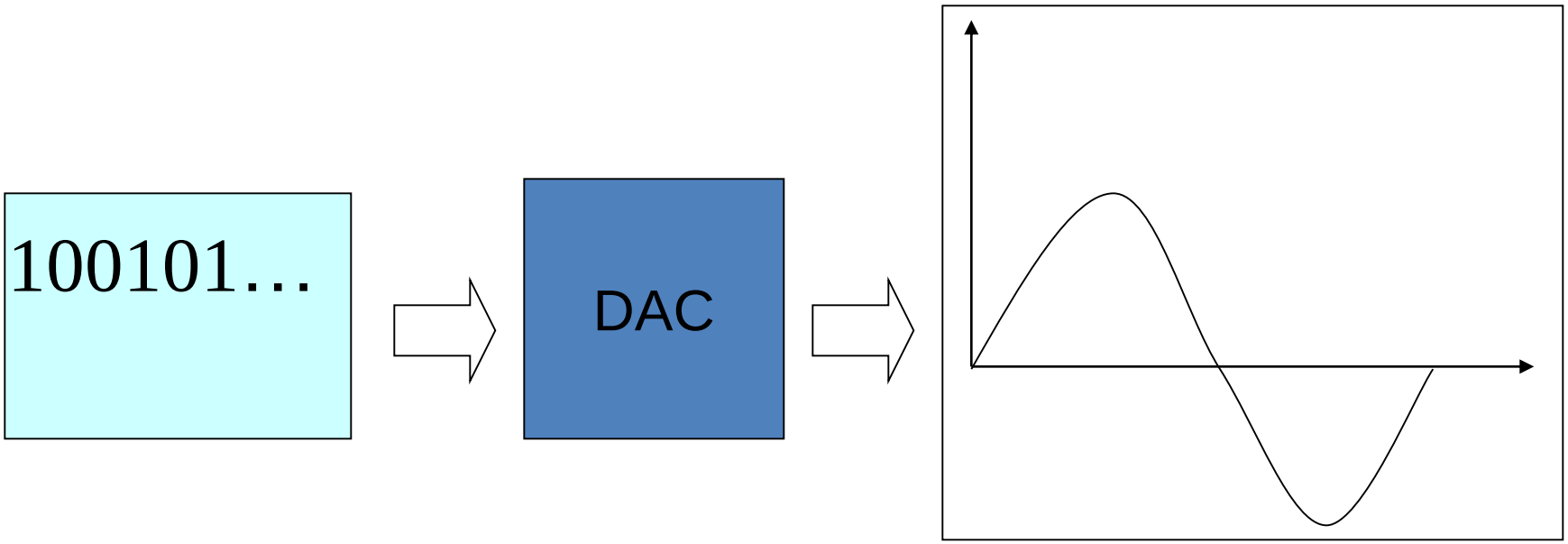
5. It has a very high temperature stability, as it is designed to operate in the temperature range of -55ºc to 125ºc.

6. Its output is compatible with TTL, CMOS and Op-Amp circuits.

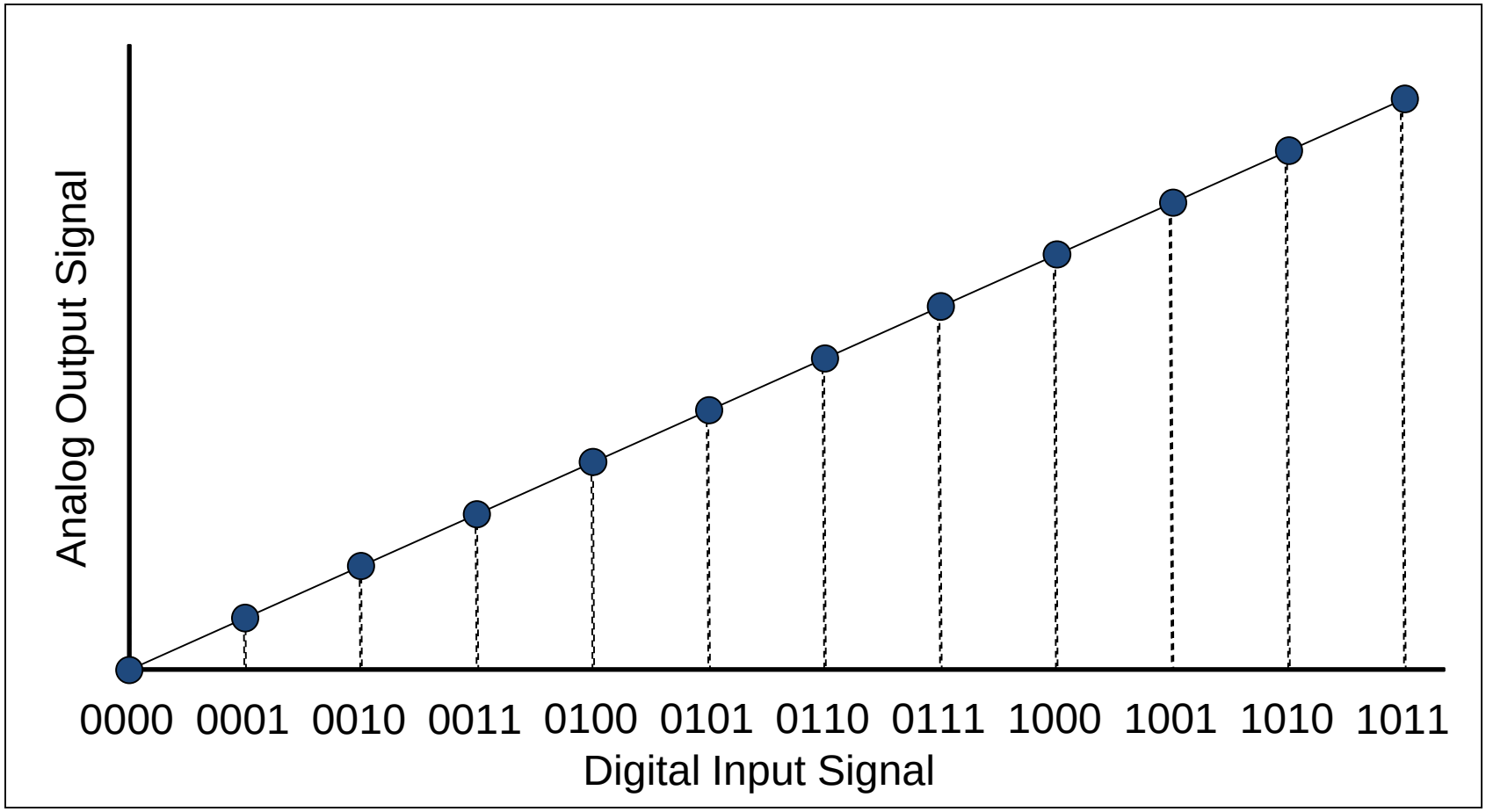
Digital to Analog Converters (DAC)

What is a DAC?

- A digital to analog converter (DAC) converts a digital signal to an analog voltage or current output.



What is a DAC?


Analog Output Signal
0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011
Digital Input Signal

Basic DAC techniques
Types of DACs

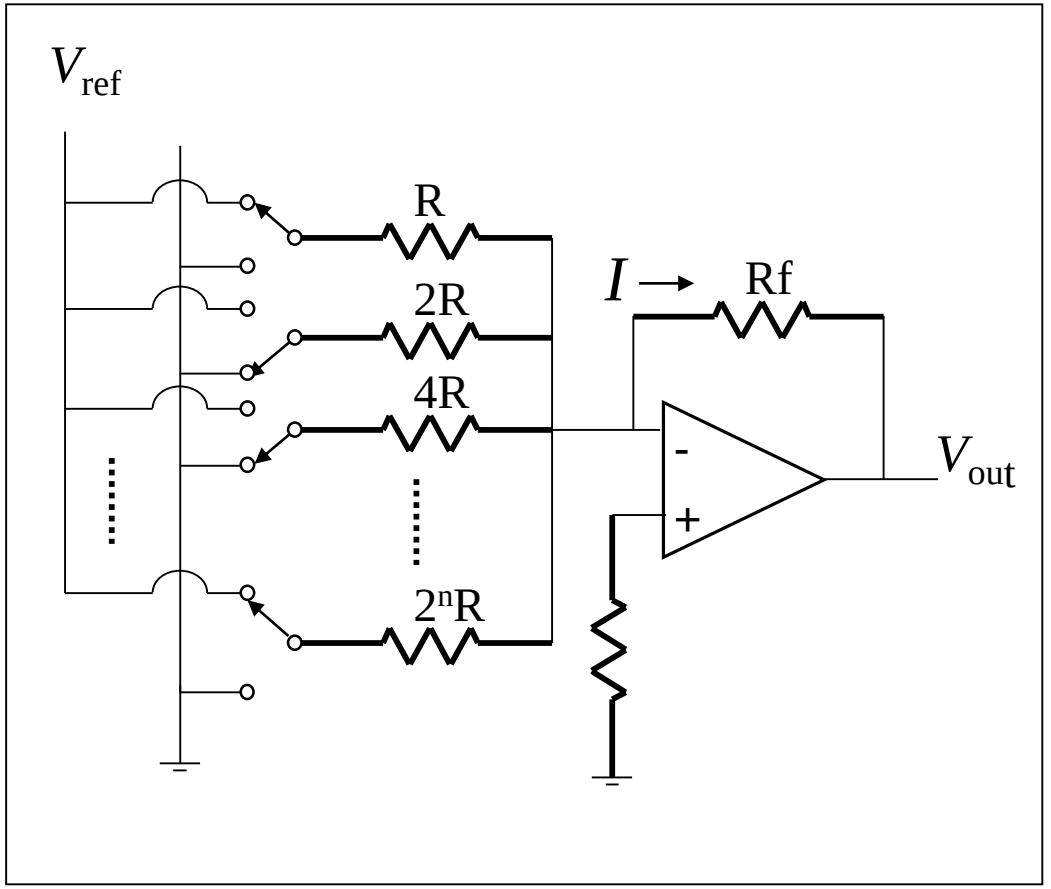
- Many types of DACs available.
- Usually switches, resistors, and op-amps used to implement conversion
- Two Types:
  - Binary Weighted Resistor
  - R-2R Ladder
  - Inverted R-2R DAC
  - IC 1408 DAC

Binary Weighted Resistor DAC

- Utilizes a summing op-amp circuit
- Weighted resistors are used to distinguish each bit from the most significant to the least significant
- Transistors are used to switch between V_{ref} and ground (bit high or low)

Binary Weighted Resistor DAC

- Assume Ideal Op-amp
- No current into op-amp
- Virtual ground at inverting input
- $V_{out} = -IR_f$

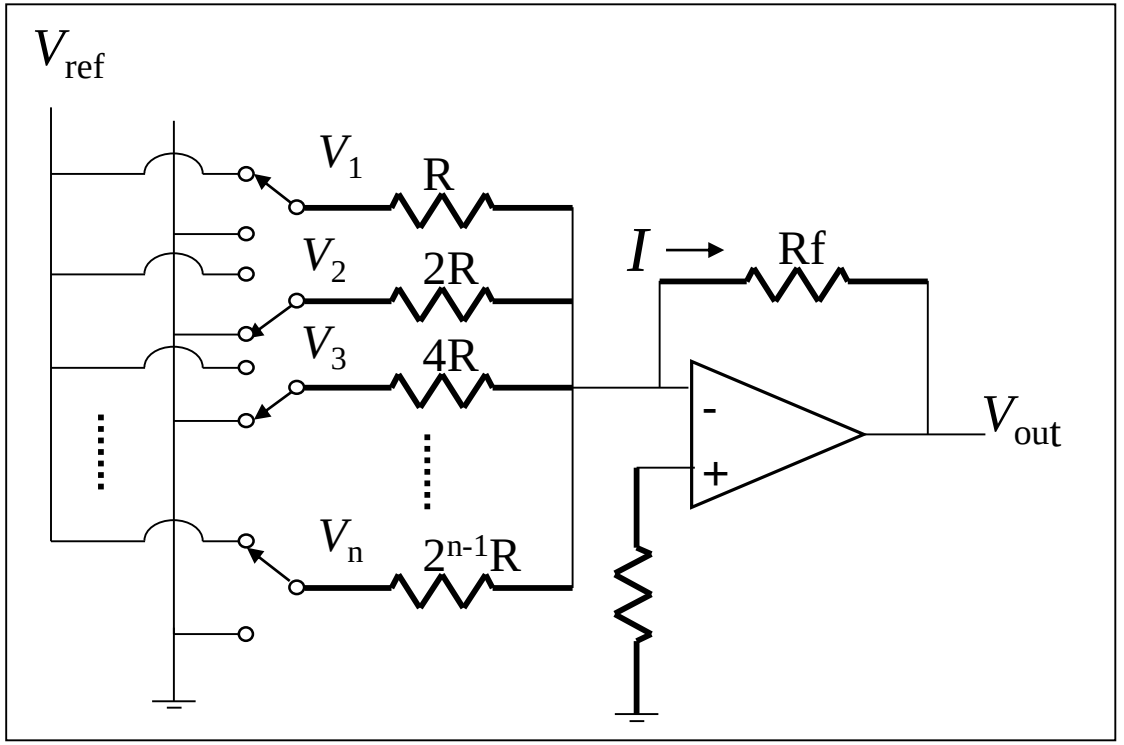


Binary Weighted Resistor DAC

Voltages V_1 through V_n are either V_{ref} if corresponding bit is high or ground if corresponding bit is low

V_1 is most significant bit

V_n is least significant bit



MSB

LSB

$$V_{out} = -IR_f = -R_f\left(\frac{V_1}{R} + \frac{V_2}{2R} + \frac{V_3}{4R} + \cdots \frac{V_n}{2^{n-1}R}\right)$$

Binary Weighted Resistor DAC

If $R_f = R/2$

$$V_{out} = -IR_f = -\left(\frac{V_1}{2} + \frac{V_2}{4} + \frac{V_3}{8} + \cdots \frac{V_n}{2^n} \right)$$

For example, a 4-Bit converter yields

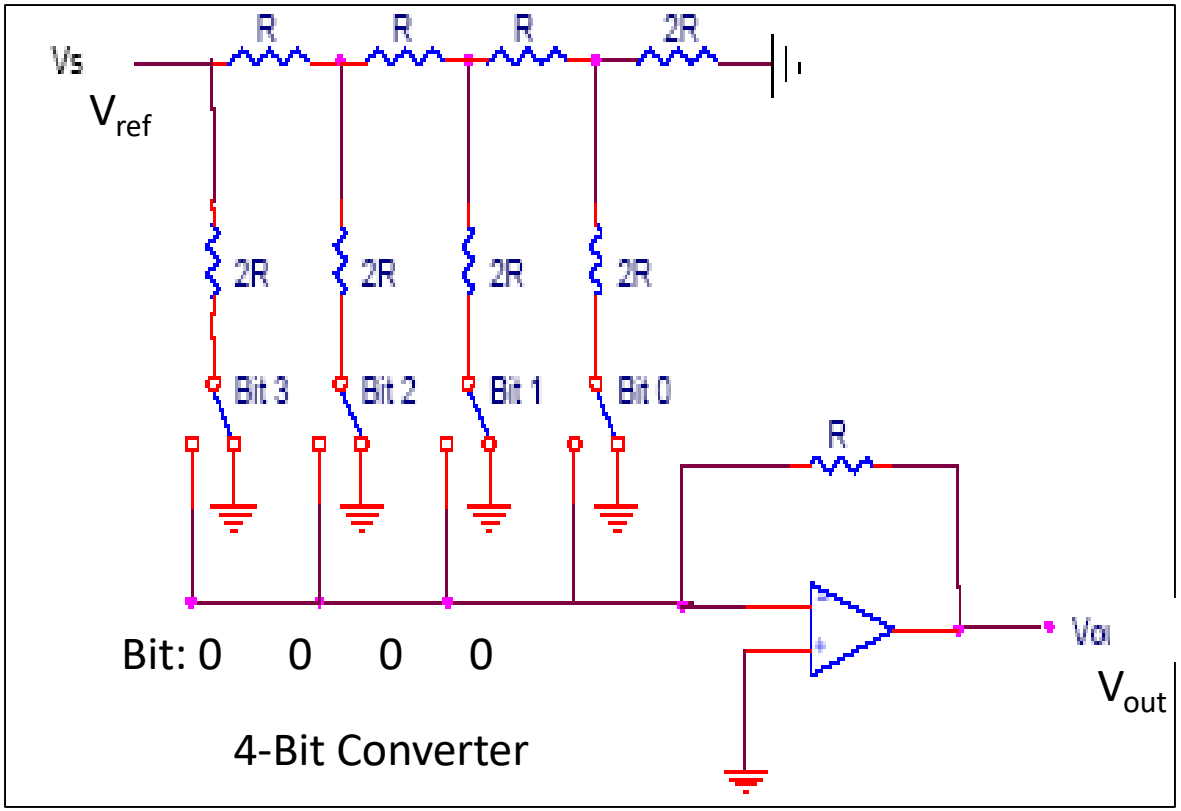
$$V_{out} = -V_{ref} \left(b_3 \frac{1}{2} + b_2 \frac{1}{4} + b_1 \frac{1}{8} + b_0 \frac{1}{16} \right)$$

Where b_3 corresponds to Bit-3, b_2 to Bit-2, etc.

Binary Weighted Resistor

- Advantages
  - Simple Construction/Analysis
  - Fast Conversion
- Disadvantages
  - Requires large range of resistors (2000:1 for 12-bit DAC) with necessary high precision for low resistors
  - Requires low switch resistances in transistors
  - Can be expensive. Therefore, usually limited to 8-bit resolution.

R-2R Ladder DAC

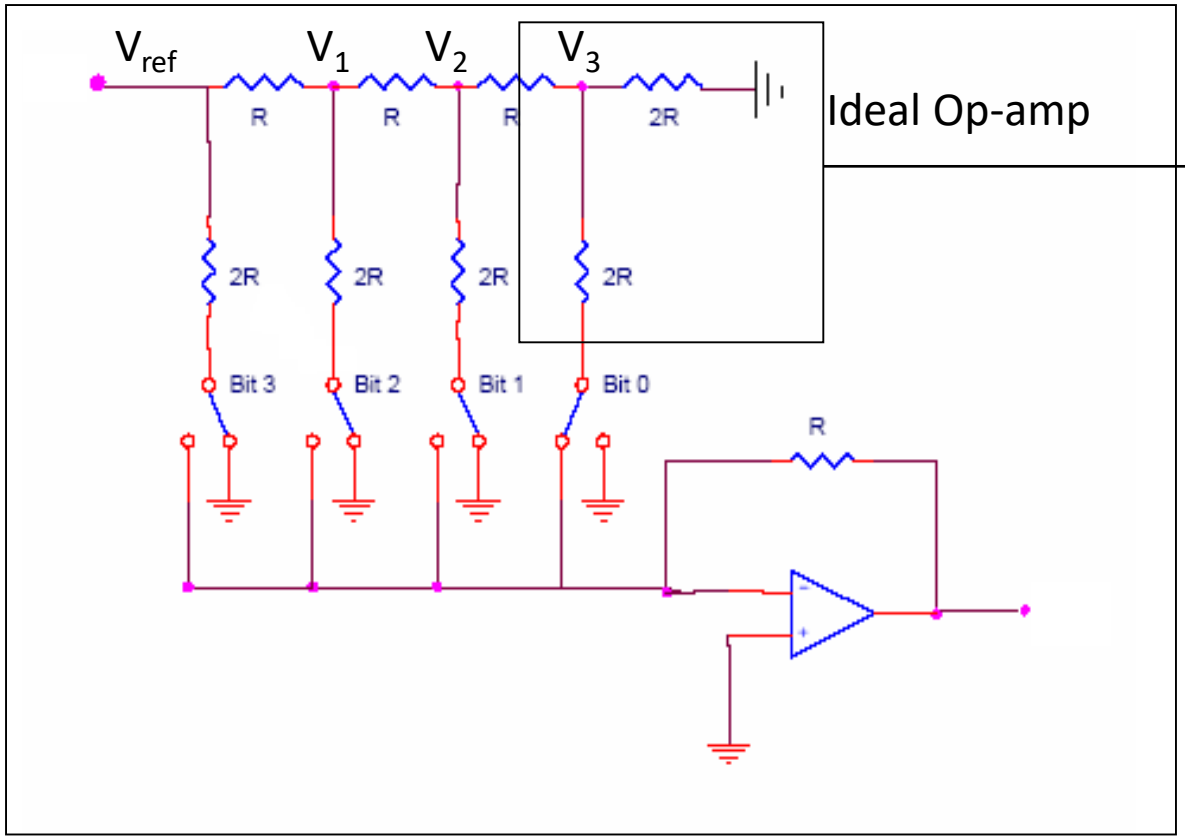


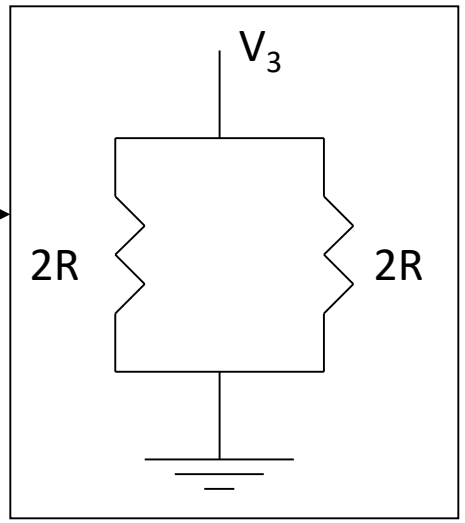
Each bit corresponds to a switch:

If the bit is high, the corresponding switch is connected to the inverting input of the op-amp.

If the bit is low, the corresponding switch is connected to ground.

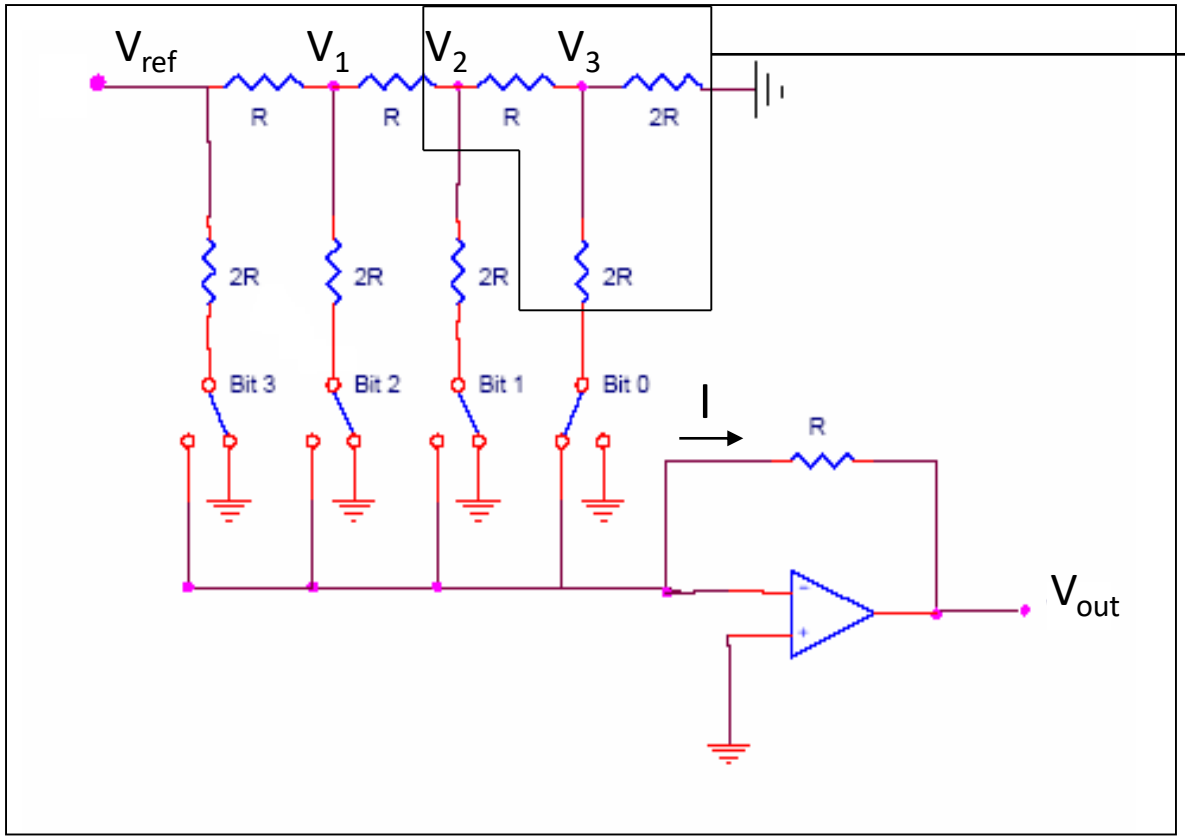
R-2R Ladder DAC

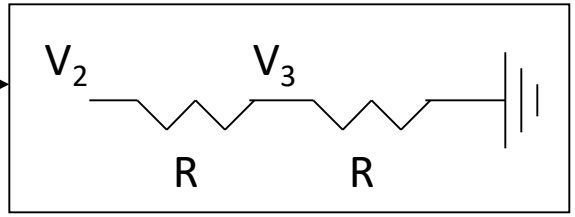




$$R_{eq} = \frac{(2R)(2R)}{(2R+2R)} = R$$

R-2R Ladder DAC





$$V_3 = \left(\frac{R}{R+R}\right)V_2 = \frac{1}{2}V_2$$

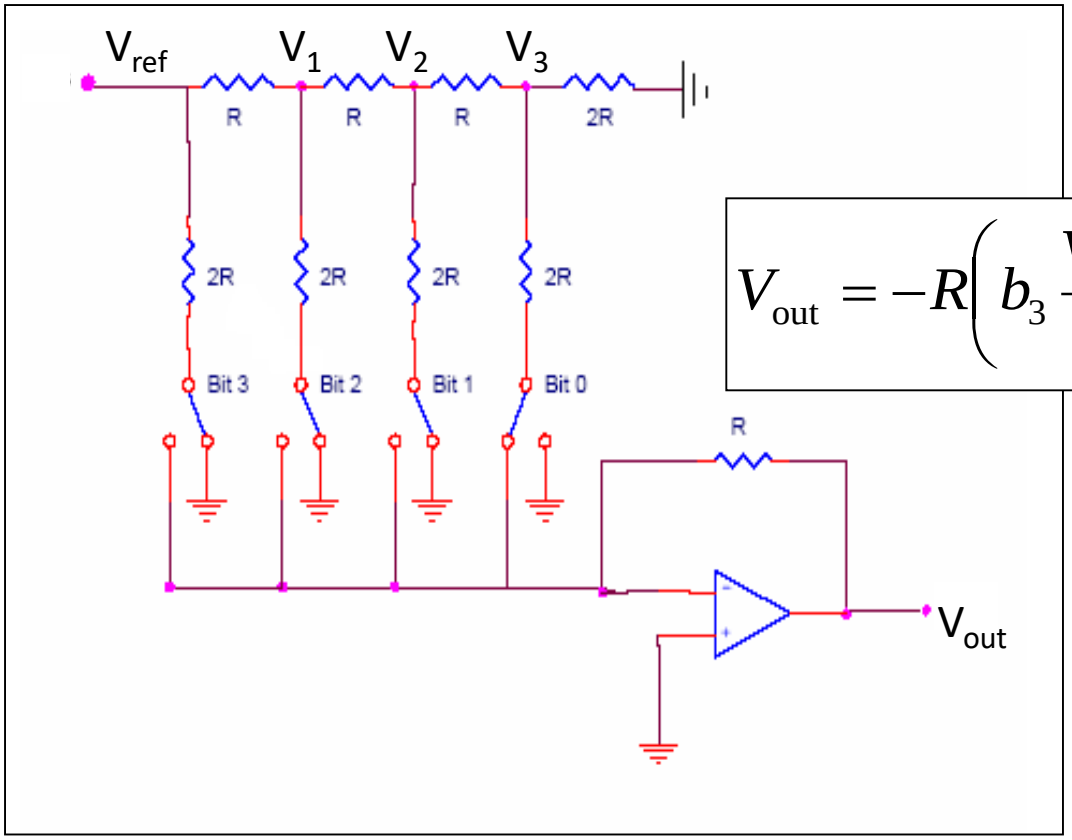
Likewise,

$$V_2 = \frac{1}{2}V_1$$

$$V_1 = \frac{1}{2}V_{\text{ref}}$$

$$V_{\text{out}} = -IR$$

R-2R Ladder DAC



Results:

$$V_3 = \frac{1}{8}V_{\text{ref}},\ V_2 = \frac{1}{4}V_{\text{ref}},\ V_1 = \frac{1}{2}V_{\text{ref}}$$

$$V_{\text{out}} = -R\left(b_3 \frac{V_{\text{ref}}}{2R} + b_2 \frac{V_{\text{ref}}}{4R} + b_1 \frac{V_{\text{ref}}}{8R} + b_0 \frac{V_{\text{ref}}}{16R} \right)$$

Where b_3 corresponds to bit 3, b_2 to bit 2, etc.

If bit n is set, b_n=1

If bit n is clear, b_n=0

R-2R Ladder DAC

For a 4-Bit R-2R Ladder

$$V_{\text{out}} = -V_{\text{ref}}\left(b_3 \frac{1}{2} + b_2 \frac{1}{4} + b_1 \frac{1}{8} + b_0 \frac{1}{16} \right)$$

For general n-Bit R-2R Ladder or Binary Weighted Resister DAC

$$V_{\text{out}} = -V_{\text{ref}} \sum_{i=1}^{n} b_{n-i} \frac{1}{2^i}$$

R-2R Ladder DAC

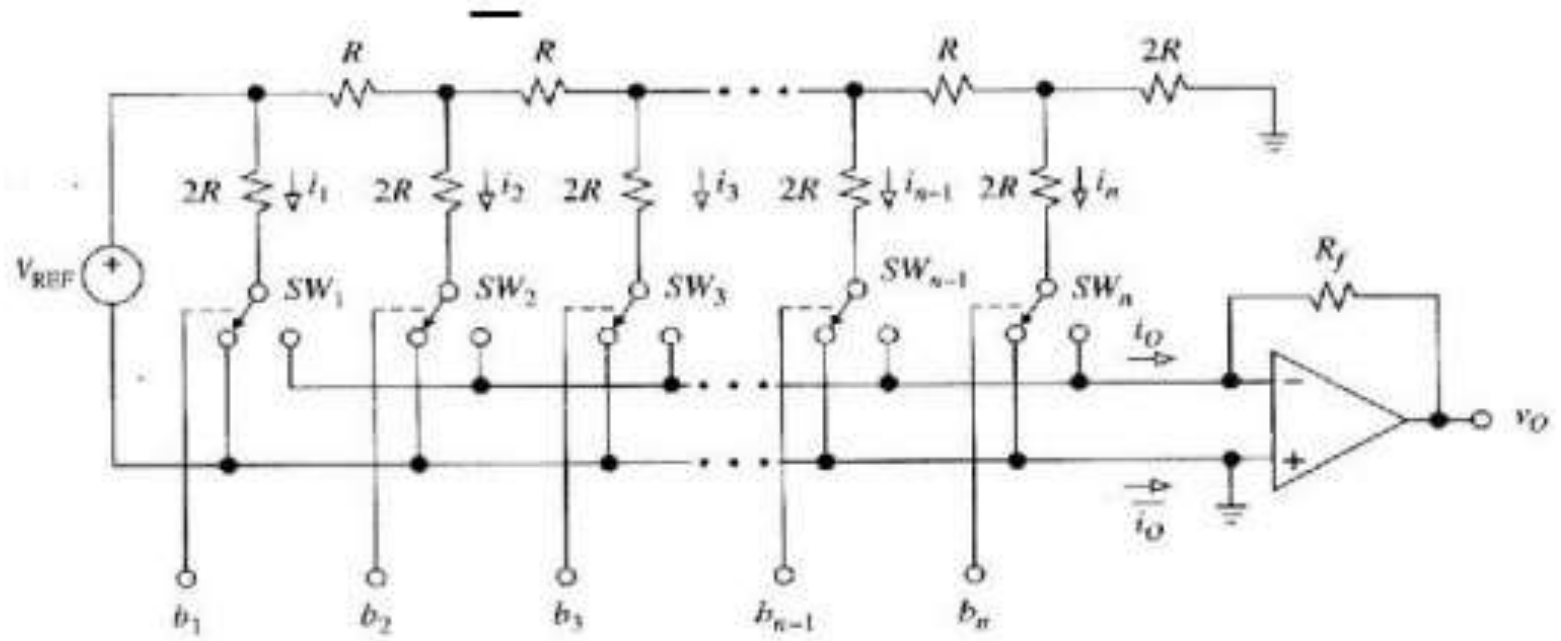
- Advantages
  - Only two resistor values (R and 2R)
  - Does not require high precision resistors
- Disadvantage
  - Lower conversion speed than binary weighted DAC

Inverted R-2R ladder DAC

1. Inverted or Current Mode DAC

- Current mode DACs operates based on the ladder currents. The ladder is formed by resistance R in the series path and resistance 2R in the shunt path. Thus the current is divided into i1 , i2, i3 ……in. in each arm. The currents are either diverted to the ground bus (io) or to the Virtual-ground bus (io).

Current mode R-2R ladder DAC



Current mode R-2R ladder DAC

- The currents are given as
- $i_1 = V_{REF}/2R = (V_{REF}/R)\ 2^{-1}$,
- $i_2 = (V_{REF})/2)/2R = (V_{REF}/R)\ 2^{-2}$ ……$i_n = (V_{REF}/R)\ 2^{-n}$.
- And the relationship between the currents are given as
- $i_2 = i_1/2$
- $i_3 = i_1/4$
- $i_4 = i_1/8$
- $i_n = i_1/2^{n-1}$
- Using the bits to identify the status of the switches, and letting V0 = -Rf *io* gives
- $V_0 = -(R_f/R)\ V_{REF}\ (b12^{-1} + b22^{-2} + \ldots\ldots\ldots + bn2^{-n})$

Current mode R-2R ladder DAC

- The two currents *io* and *io* are complementary to each other and the potential of *io* bus must be sufficiently close to that of the *io* bus. Otherwise, linearity errors will occur. The final op-amp is used as current to voltage converter.

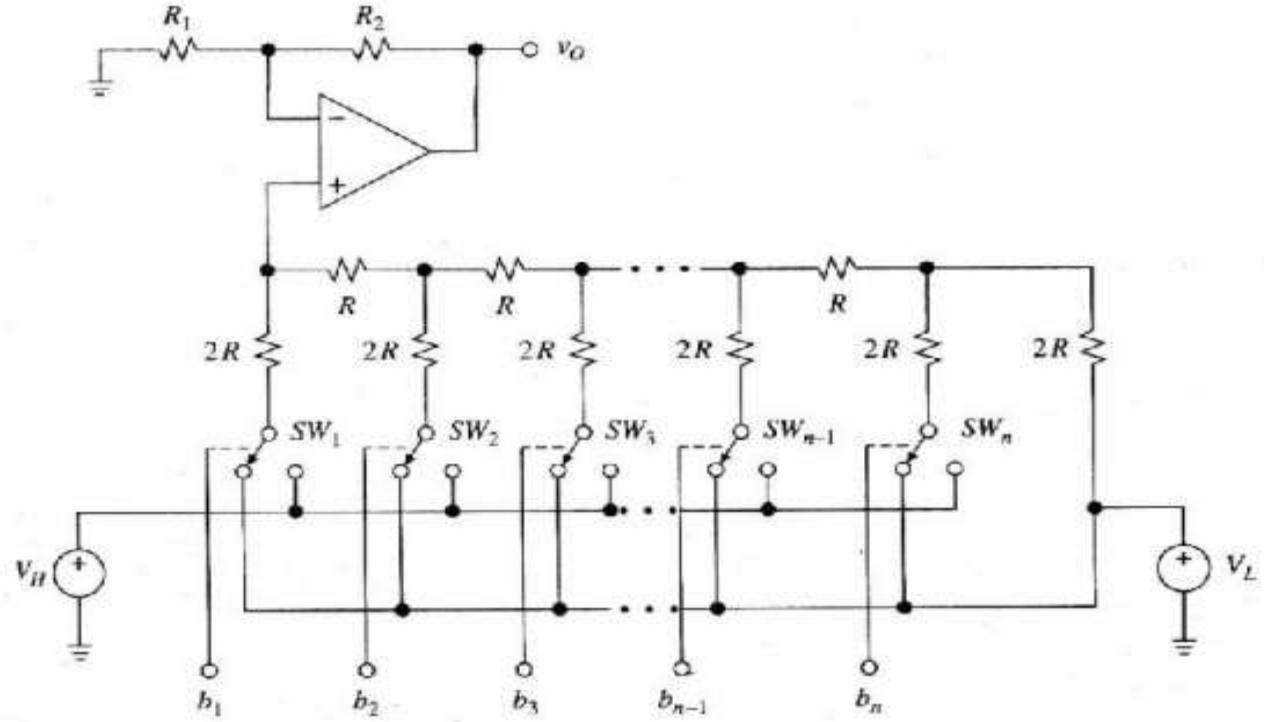
Advantages of Current mode D/A

1. The major advantage of current mode D/A converter is that the voltage change across each switch is minimal. So the charge injection is virtually eliminated and the switch driver design is made simpler.
2. In Current mode or inverted ladder type DACs, the stray capacitance do not affect the Speed of response of the circuit due to constant ladder node voltages. So improved speed performance.

Voltage Mode DAC

- This is the alternative mode of DAC and is called so because the 2R resistance in the shunt path is switched between two voltages named as V_L and V_H. The output of this DAC is obtained from the leftmost ladder node. As the input is sequenced through all the possible binary state starting from All 0s (0…..0) to all 1s (1…..1). The voltage of this node changes in steps of 2^{-n} (V_H - V_L) from the minimum voltage of Vo = V_L to the maximum of Vo = VH - 2^{-n} (V_H - V_L).

Voltage Mode DAC



Voltage Mode DAC

- The diagram also shows a non-inverting amplifier from which the final output is taken. Due to this buffering with a non- inverting amplifier, a scaling factor defined by $K = 1 + (R_2/R_1)$ results.

Advantages of Voltage Mode DAC

1. The major advantage of this technique is that it allows us to interpolate between any two voltages, neither of which need not be a zero.
2. More accurate selection and design of resistors R and 2R are possible and simple construction.
3. The binary word length can be easily increased by adding the required number or R-2R sections.

IC 1408 DAC

- **IC 1408 DAC Pin Diagram:**

  The IC 1408 DAC Pin Diagram is an 8 bit R/2R ladder type D/A converter compatible with TTL and CMOS logic. It is designed to use where the output current is linear product of an eight bit digital word. Fig. 14.108 shows the pin diagram and block diagram for IC 1408 DAC.

IC 1408 DAC

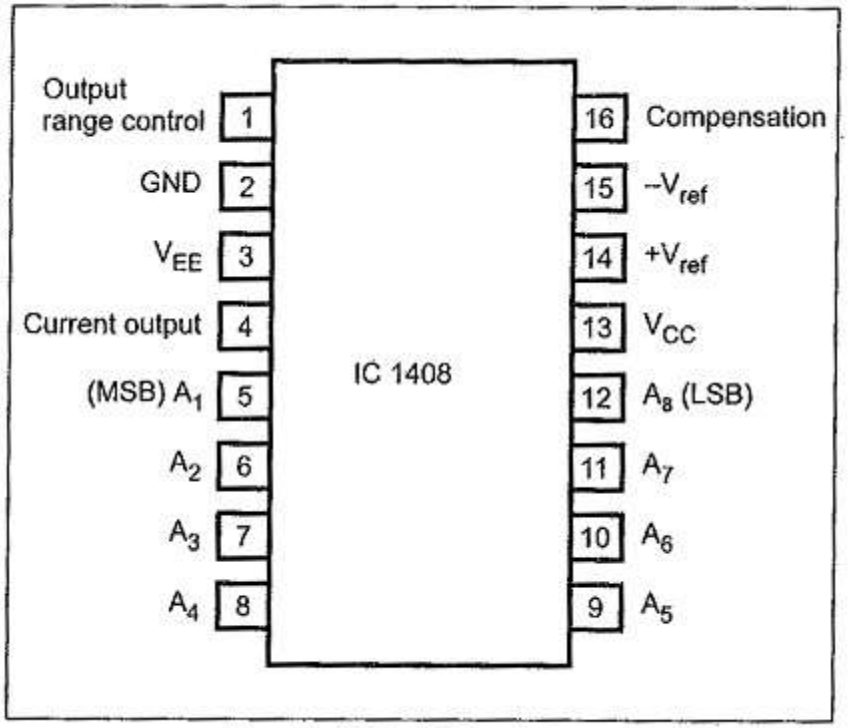


Fig. 14.108 (a) Pin diagram

IC 1408 DAC

- The IC 1408 DAC Pin Diagram consists of a reference current amplifier, an R/2R ladder and eight high speed current switches. It has eight input data lines A_1 (MSB) through A_8 (LSB) which control the positions of current switches.

IC 1408 DAC

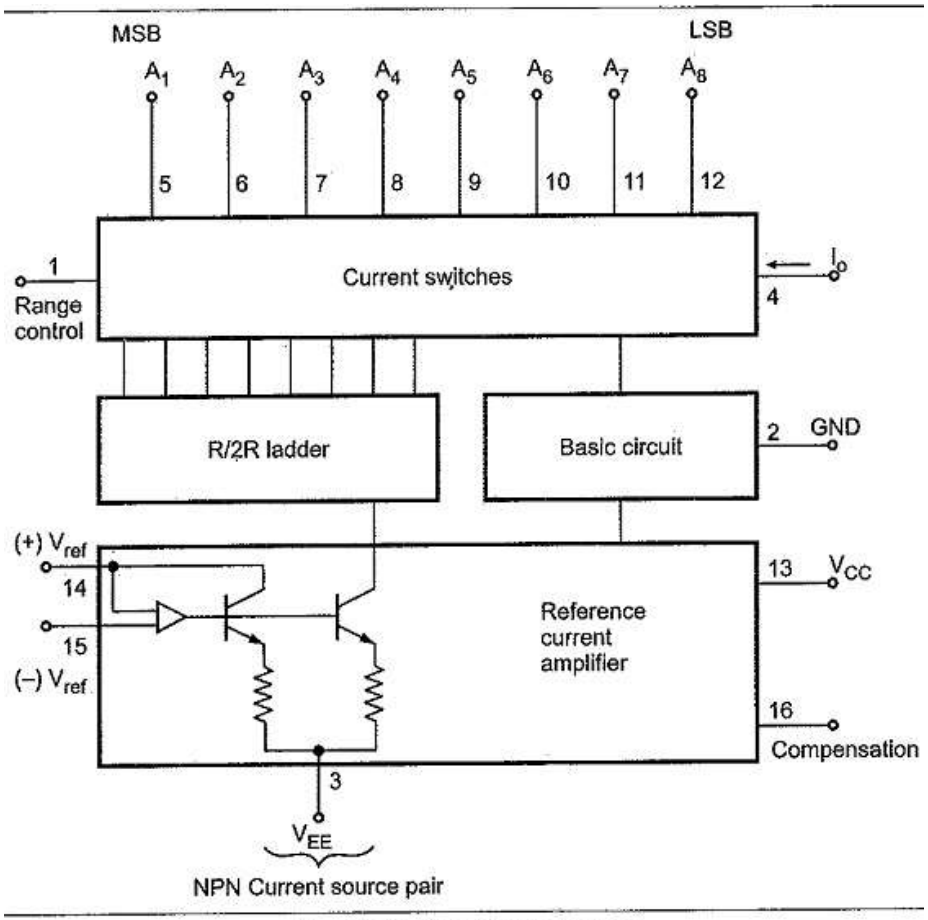


Fig. 14.108 (b) Block diagram

IC 1408 DAC

- It requires 2 mA reference current for full scale input and two power supplies V_{cc}= + 5 V and V_{EE} = – 15 V (V_{EE} can range from – 5 V to – 15 V).
- The voltage V_{ref} and resistor R_{14} determines the total reference current source and R_{15} is generally equal to R_{14} to match the input impedance of the reference current amplifier.
- Fig. 14.109 shows a typical circuit for IC 1408.
- The output current I_o can be given as

$$I_o = \frac{V_{ref}}{R_{14}}\left(\frac{A_1}{2}+\frac{A_2}{4}+\frac{A_3}{8}+\frac{A_4}{16}+\frac{A_5}{32}+\frac{A_6}{64}+\frac{A_7}{128}+\frac{A_8}{256}\right) \quad \ldots(1)$$

IC 1408 DAC

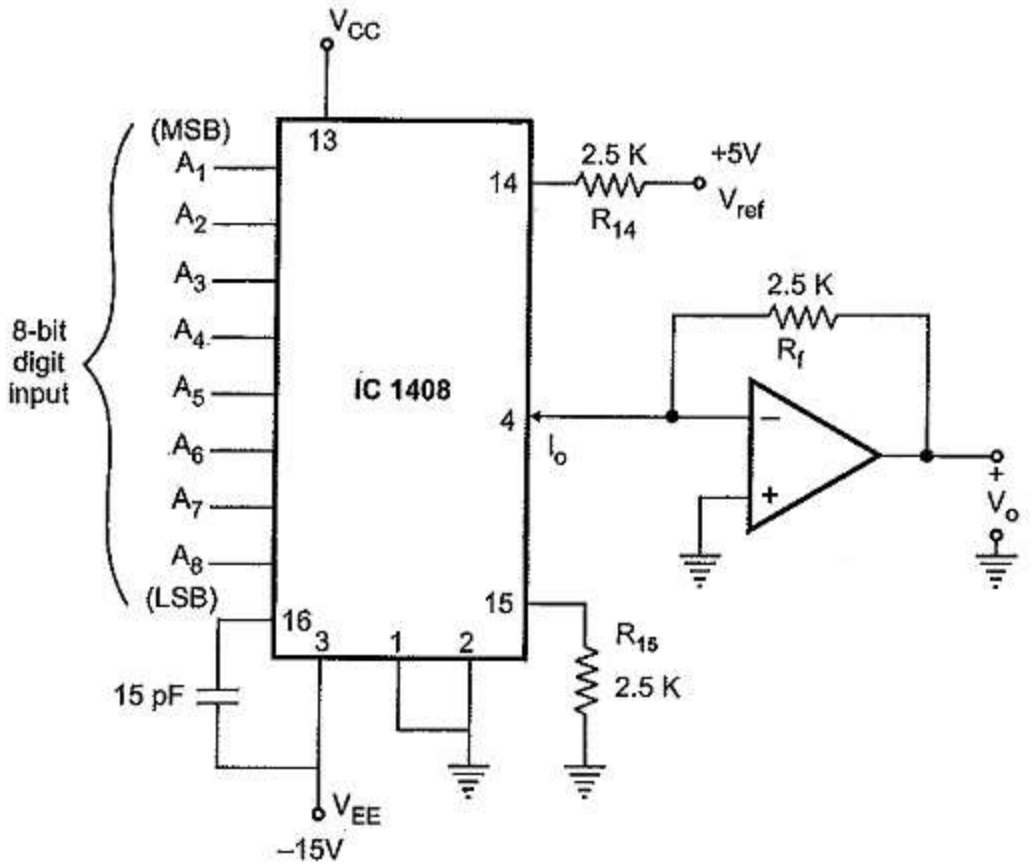


Fig. 14.109 Typical circuit for IC 1408

IC 1408 DAC

- **Note :** Input A_1 through A_8 can be either 0 or 1. Therefore, for typical circuit full scale current can be given as,
- $$I_o = \frac{5}{25\,K}\left(\frac{1}{2}+\frac{1}{4}+\frac{1}{8}+\frac{1}{16}+\frac{1}{32}+\frac{1}{64}+\frac{1}{128}+\frac{1}{256}\right)$$
$$= \frac{2\,mA \times 255}{256}$$
$$= 1.992\ mA$$

IC 1408 DAC

- It shows that the full scale output current is always 1 LSB less than the reference current source of 2 mA. This output current is converted into voltage by I to V converter. The output voltage for full scale input can be given as
- $$V_o = 1.992 \times 25\ K$$
$$= 4.98\ V$$

Specifications of DACs

- Resolution
- Speed
- Linearity
- Settling Time
- Reference Voltages
- Errors

Resolution

- Smallest analog increment corresponding to 1 LSB change
- An N-bit resolution can resolve 2^N distinct analog levels
- Common DAC has a 8-16 bit resolution

$$\text{Resolution} = V_{LSB} = \frac{V_{ref}}{2^N}$$

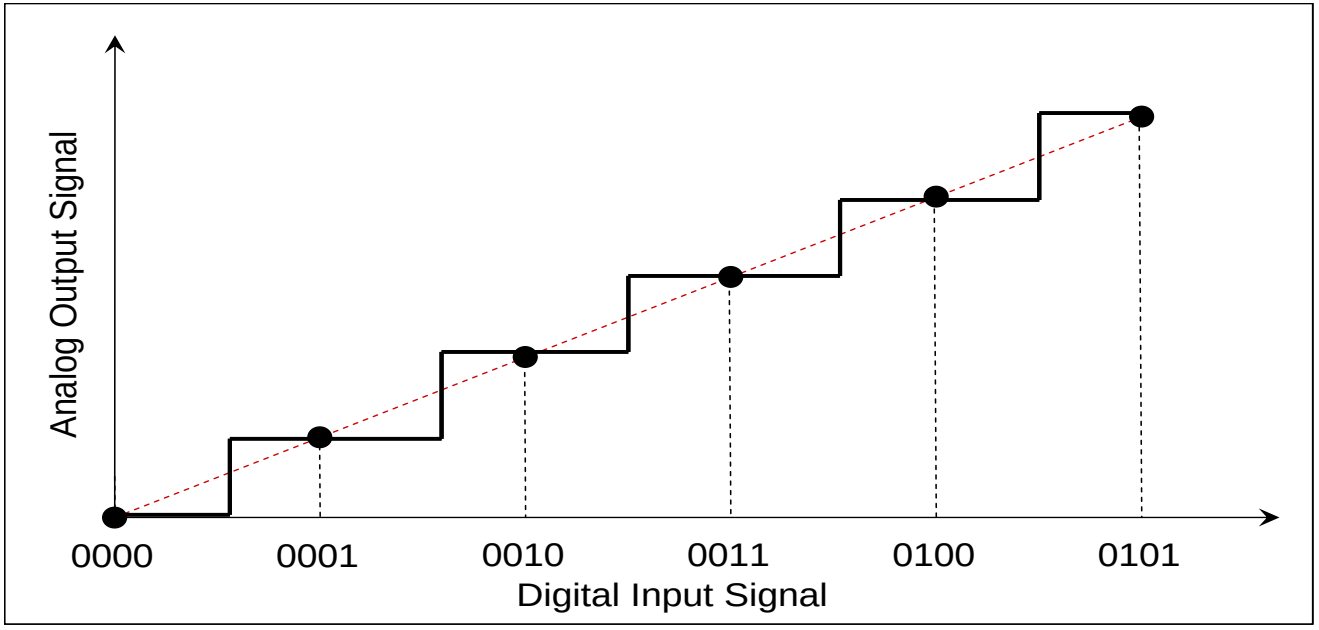
$$\text{where } N = number\ of\ bits$$

Speed

- Rate of conversion of a single digital input to its analog equivalent
- Conversion rate depends on
  - clock speed of input signal
  - settling time of converter
- When the input changes rapidly, the DAC conversion speed must be high.

Linearity

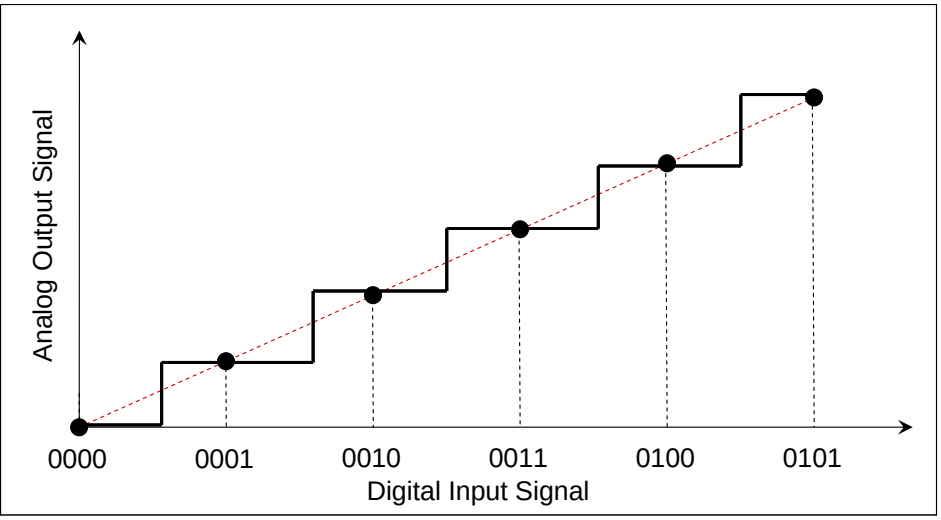
- The difference between the desired analog output and the actual output over the full range of expected values



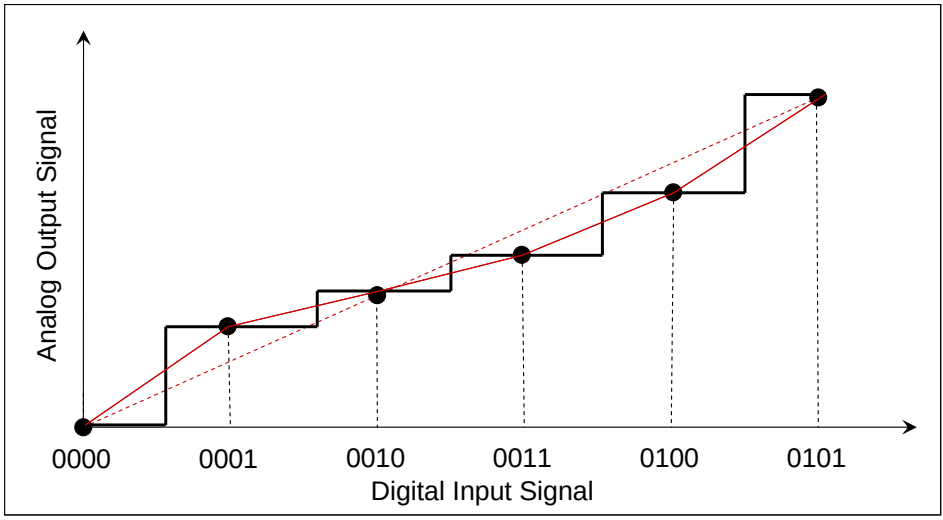
Linearity

- Ideally, a DAC should produce a linear relationship between the digital input and analog output

Linearity (Ideal)

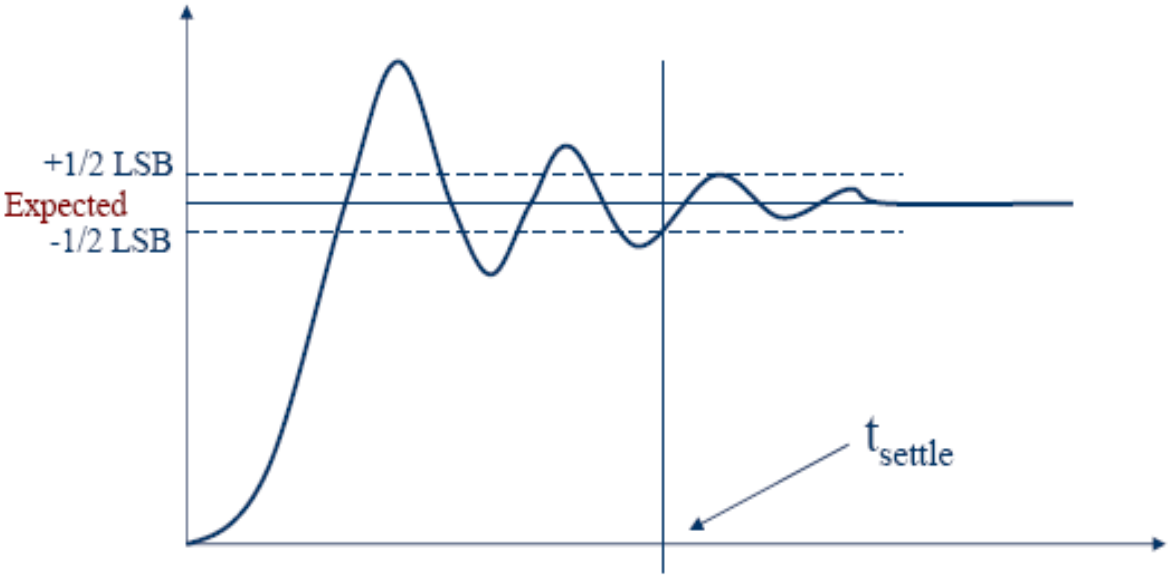


Non-Linearity



Settling Time

- Time required for the output signal to settle within +/- ½ LSB of its final value after a given change in input scale
- Limited by slew rate of output amplifier
- Ideally, an instantaneous change in analog voltage would occur when a new binary word enters into DAC



Reference Voltages

- Used to determine how each digital input will be assigned to each voltage division
- Types:
  - Non-multiplier DAC: Vref is fixed
  - Multiplier DAC: Vref provided by external source

Applications

- Digital Motor Control
- Computer Printers
- Sound Equipment (e.g. CD/MP3 Players, etc.)
- Electronic Cruise Control
- Digital Thermostat

Analog-to-Digital Converter (ADC)

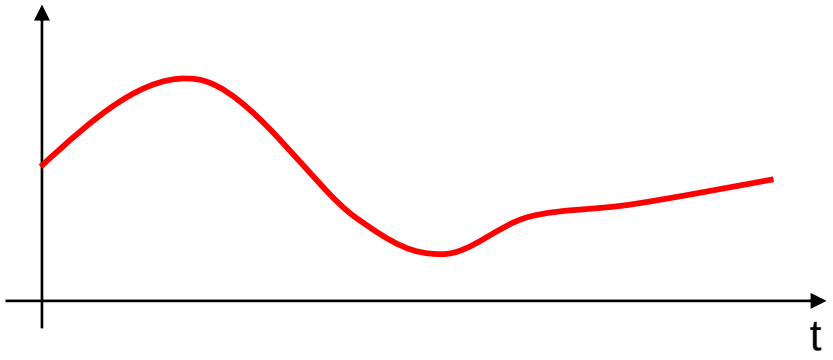
Background Information

- What is ADC?
- Conversion Process
- Accuracy
- Examples of ADC applications

Signal Types

Analog Signals

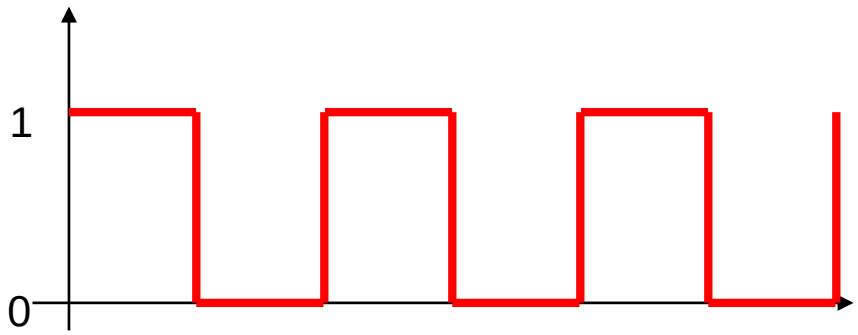
- Any continuous signal, that is a time varying variable of the signal, is a representation of some other time varying quantity
  - Measures one quantity in terms of some other quantity
  - Examples
    - Speedometer needle as function of speed
    - Radio volume as function of knob movement



Signal Types

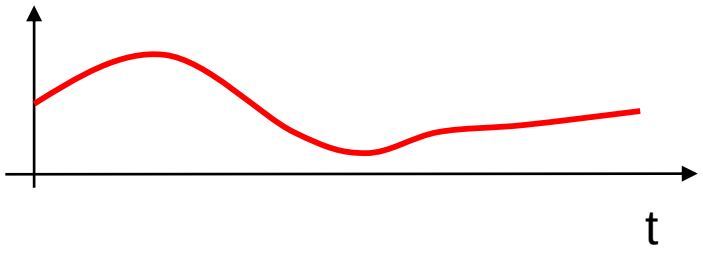
Digital Signals

- Consist of only two states
  - Binary States
  - On and off
- Computers can only perform processing on digitized signals



Analog-Digital Converter (ADC)

- An electronic integrated circuit which converts a signal from analog (**continuous**) to digital (discrete) form
- Provides a link between the analog world of transducers and the digital world of signal processing and data handling



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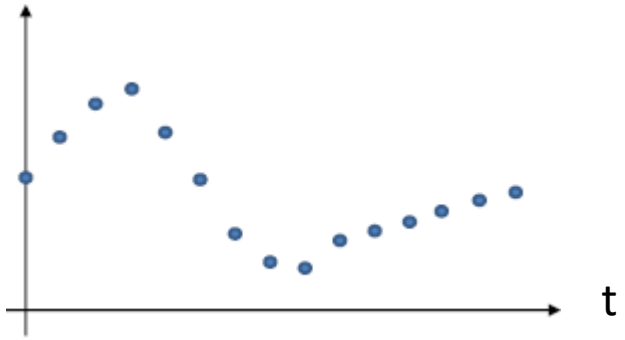
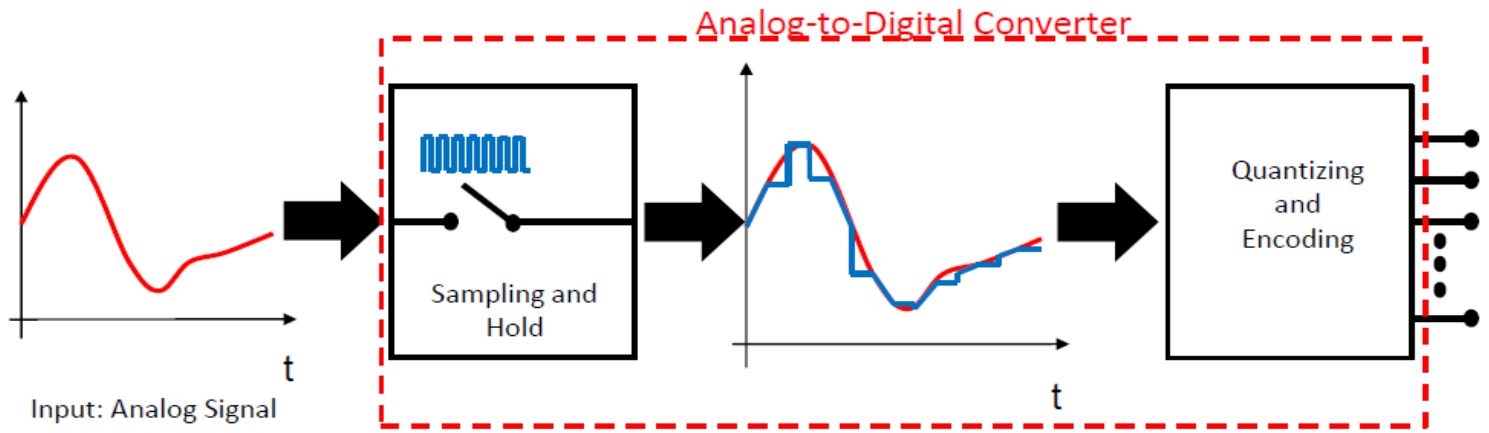


ADC Conversion Process

Two main steps of process

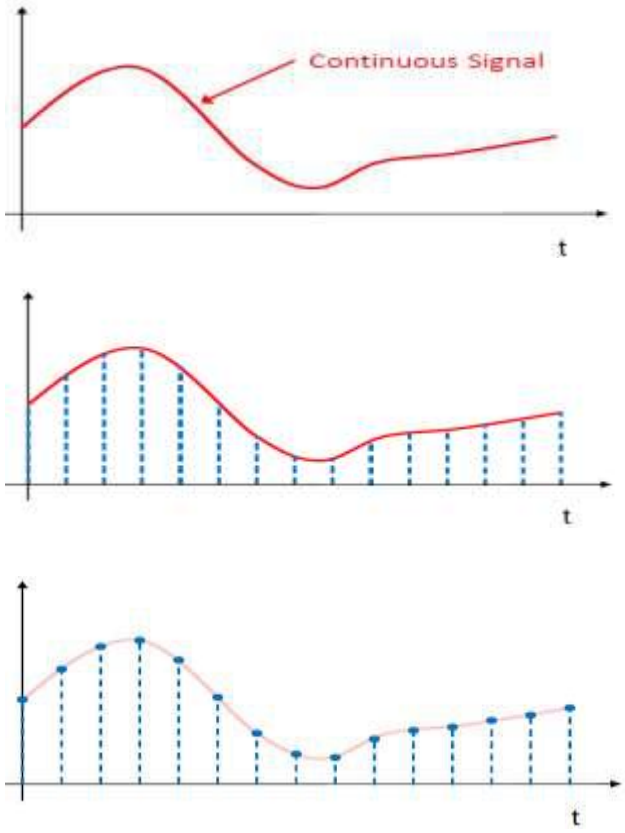
1. Sampling and Holding
2. Quantization and Encoding



ADC Process

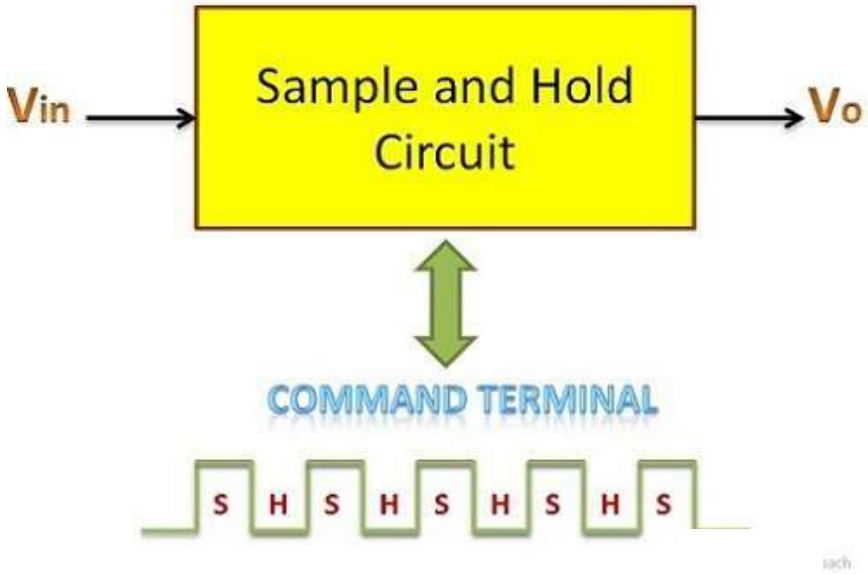
Sampling & Hold

- Measuring analog signals at uniform time intervals
  - Ideally twice as fast as what we are sampling
- Digital system works with discrete states
  - Taking samples from each location
- Reflects sampled and hold signal
  - Digital approximation

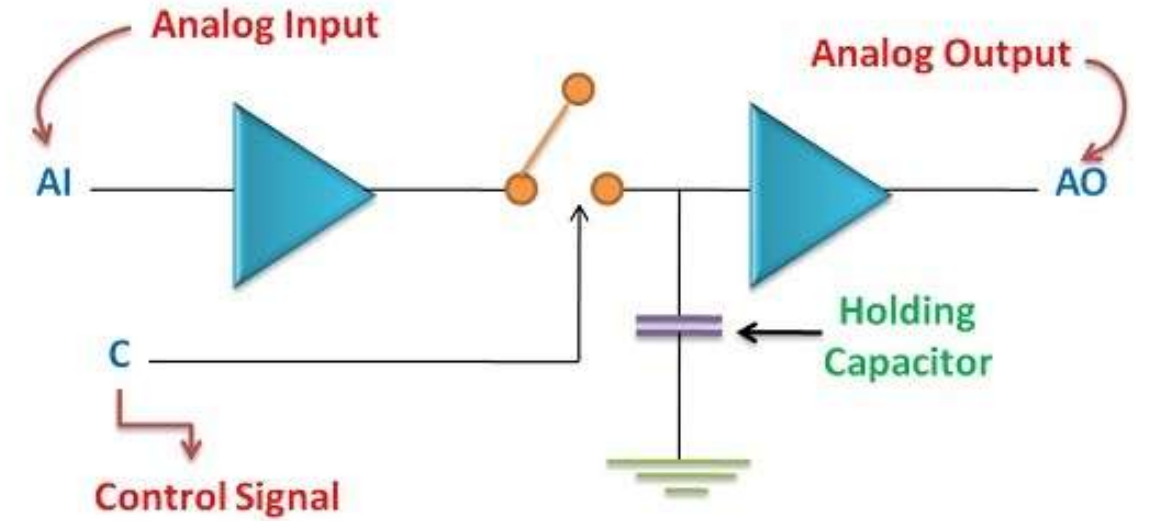


Sample and Hold Circuit

- The time during which sample and hold circuit generates the sample of the input signal is called **sampling time.**
- Similarly, the time duration of the circuit during which it holds the sampled value is called **holding time.**
- Sampling time is generally between **1µs to 14 µs** while the holding time can assume any value as required in the application.
- Capacitor is the heart of sample and hold circuit. The capacitor charges to its peak value when the switch is closed, i.e. during sampling and holds the sampled voltage when the switch is open.


Vin
Sample and Hold Circuit
Vo
COMMAND TERMINAL
S H S H S H S H S

Circuit Diagram



Circuit diagram of Sample and Hold Circuit

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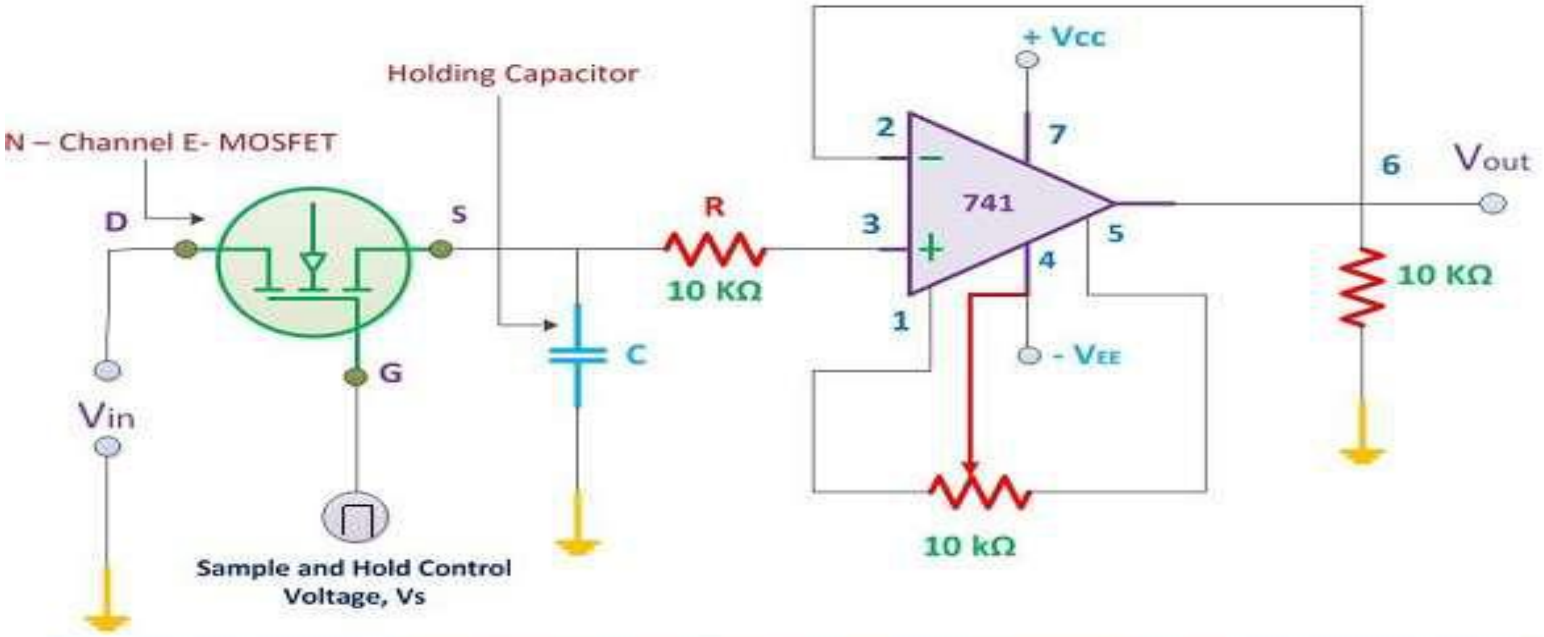
Circuit Diagram



Practical Circuit of Sample and Hold Circuit

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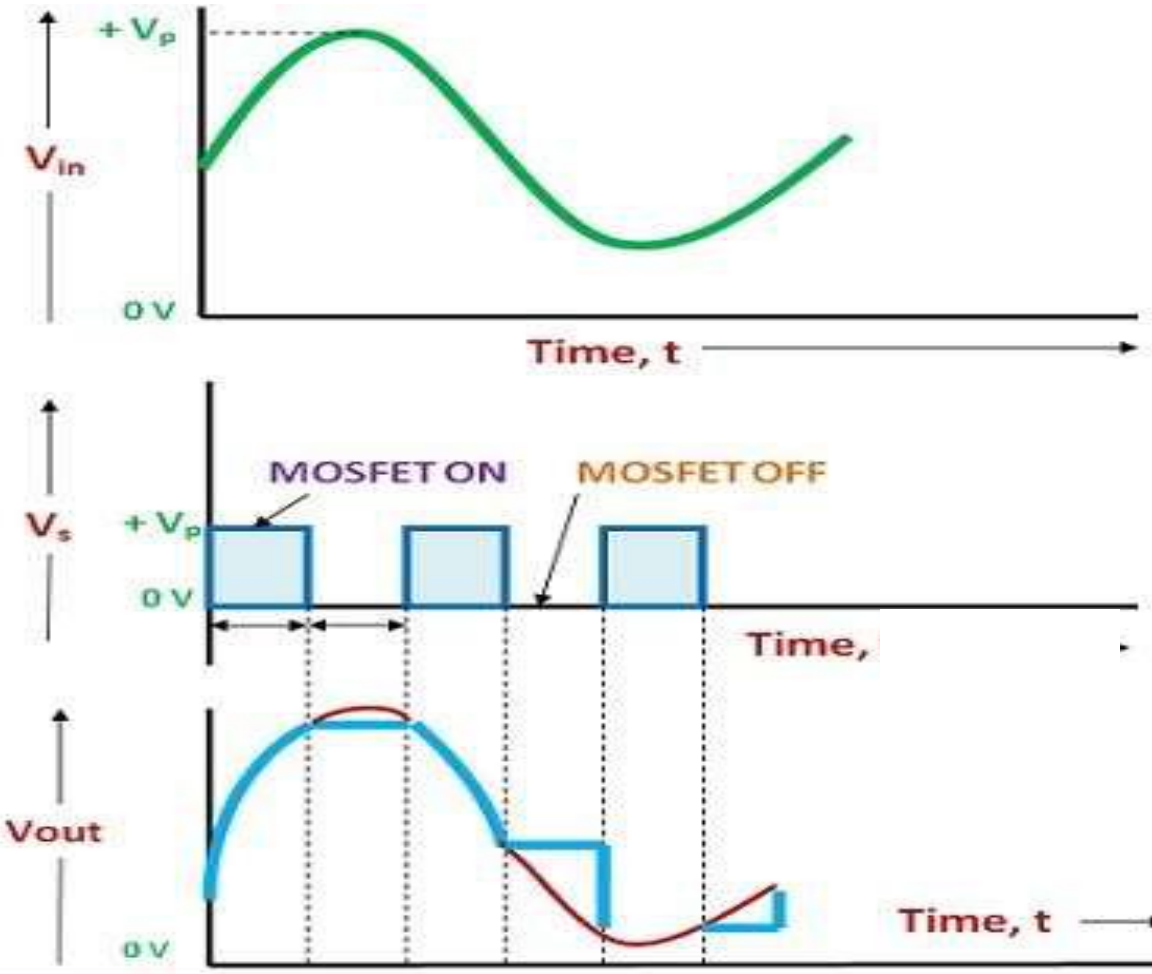
- The N-channel Enhancement MOSFET is used as the switching element.
- Input voltage is applied through its drain terminal and control voltage to its gate terminal.
- When the positive pulse of the control voltage is applied, the MOSFET will be switched to ON state - it acts as a closed switch.
- On the contrary, when the control voltage is zero then the MOSFET will be switched to OFF state - acts as an open switch.
- When the switch is closed, the analog signal applied to it through the drain terminal is fed to the capacitor.
- The capacitor charges to its peak value.
- When the MOSFET switch is opened, then the capacitor stops charging. Due to the high impedance operational amplifier connected at the end of the circuit, the capacitor experiences high impedance due to this it cannot get discharged.
- Charge is held by the capacitor for a definite amount of time - **holding period.**
- Time in which samples of the input voltage is generated - **sampling period.**

Input-Output Waveform



Input and Output Waveforms of Practical Sample and Hold Circuit

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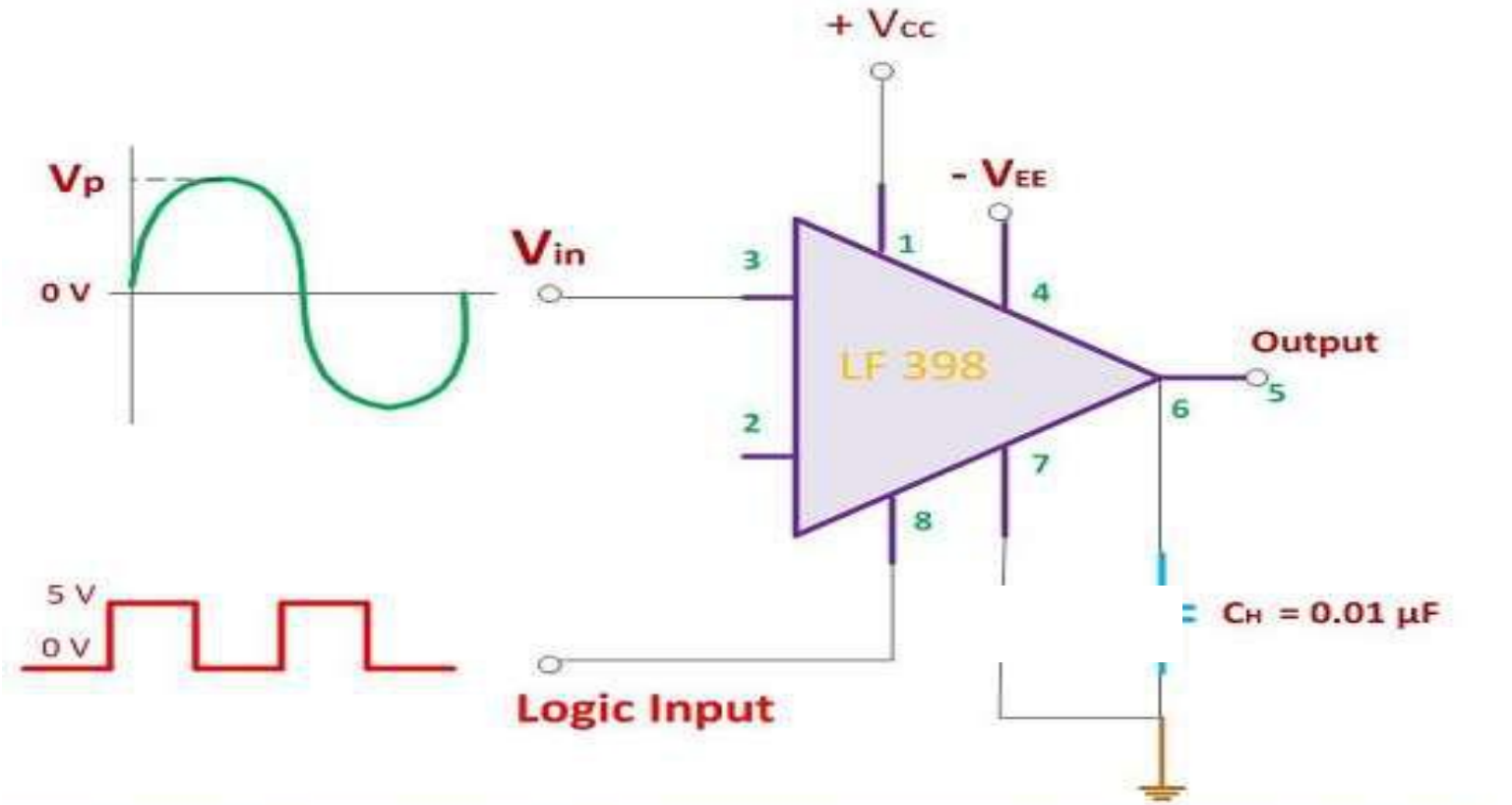

Typical Connection Diagram of Sample and Hold Circuit

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Applications of Sample and Hold Circuit

- Data Distribution System
- Sampling Oscilloscopes
- Data Conversion System
- Digital Voltmeters
- Analog Signal Processing
- Signal Constructional Filters

ADC Applications

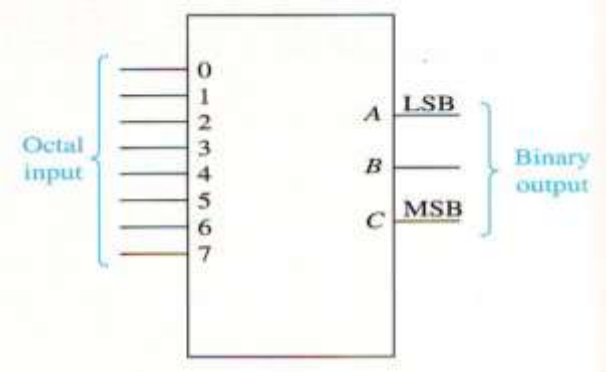
- ADC are used virtually everywhere where an analog signal has to be processed, stored, or transported in digital form
  - Microphones
  - Strain Gages
  - Thermocouple
  - Digital Multimeters

Types of ADC

- Parallel Comparator Type/ Flash A/D Converter
- Counter type A/D Converter
- Successive Approximation A/D Converter
- Dual Slope A/D Converter/Integrating Type

Flash ADC

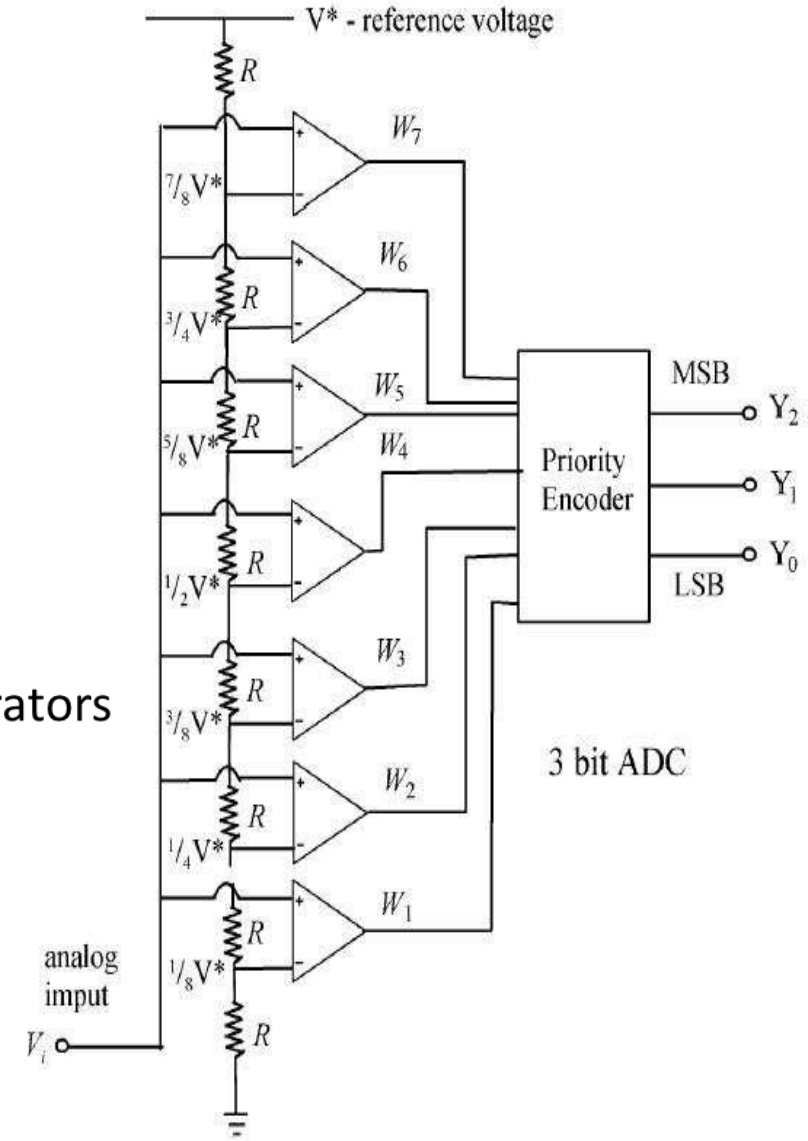
- Also known as parallel ADC
- Elements
  - Encoder – *Converts output of comparators to binary*
  - Comparators



$$V_{out} = \begin{cases} V_{S+} & V_1 > V_2 \\ V_{S-} & V_1 < V_2 \end{cases}$$

Flash ADC

- Algorithm
  - V_{in} value lies between two comparators
  - Resolution $\Delta V = \frac{V_{ref}}{2^N}$;
  - N= Encoder Output bits
  - Comparators => 2^N-1
  - Example: V_{ref} 8V, Encoder 3-bit
    - Resolution $\Delta V = \frac{8}{2^3}$ = 1.0V
    - Comparators 2^3-1=7
  - 1 additional encoder bit -> 2 x # Comparators



Flash ADC Example

V_{in} = 5.5V, V_{ref}= 8V

V_{in} lies in between V_{comp5} & V_{comp6}

$V_{comp5} = V_{ref}*5/8 = 5V$

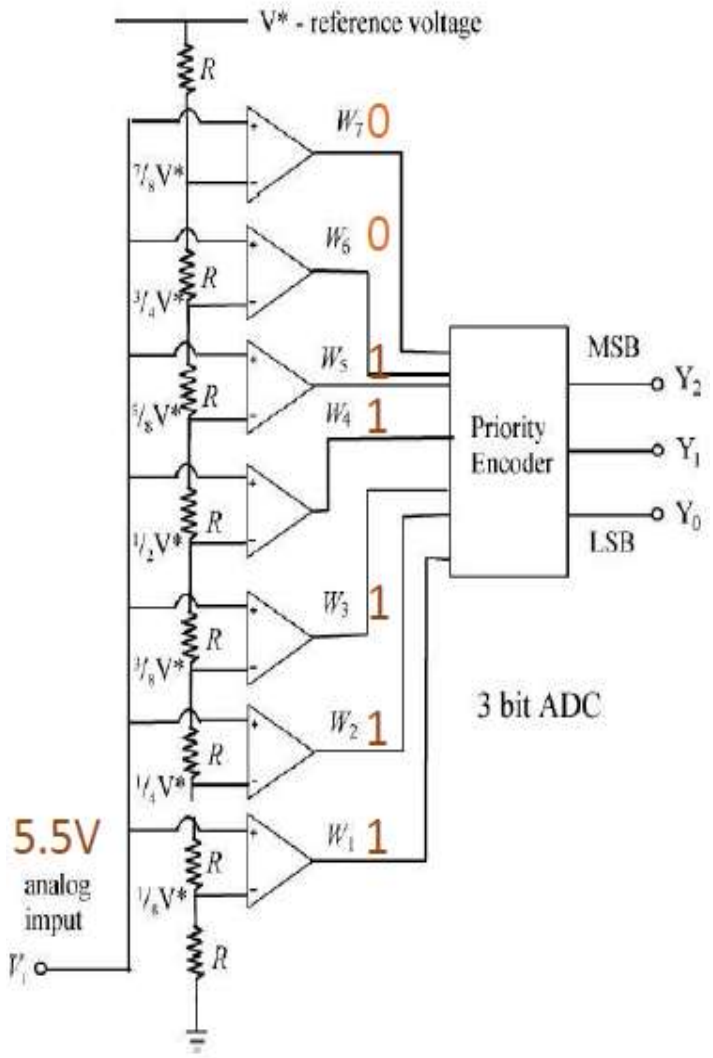
$V_{comp6} = V_{ref}*6/8 = 6V$

Comparator 1 - 5 => output **1**

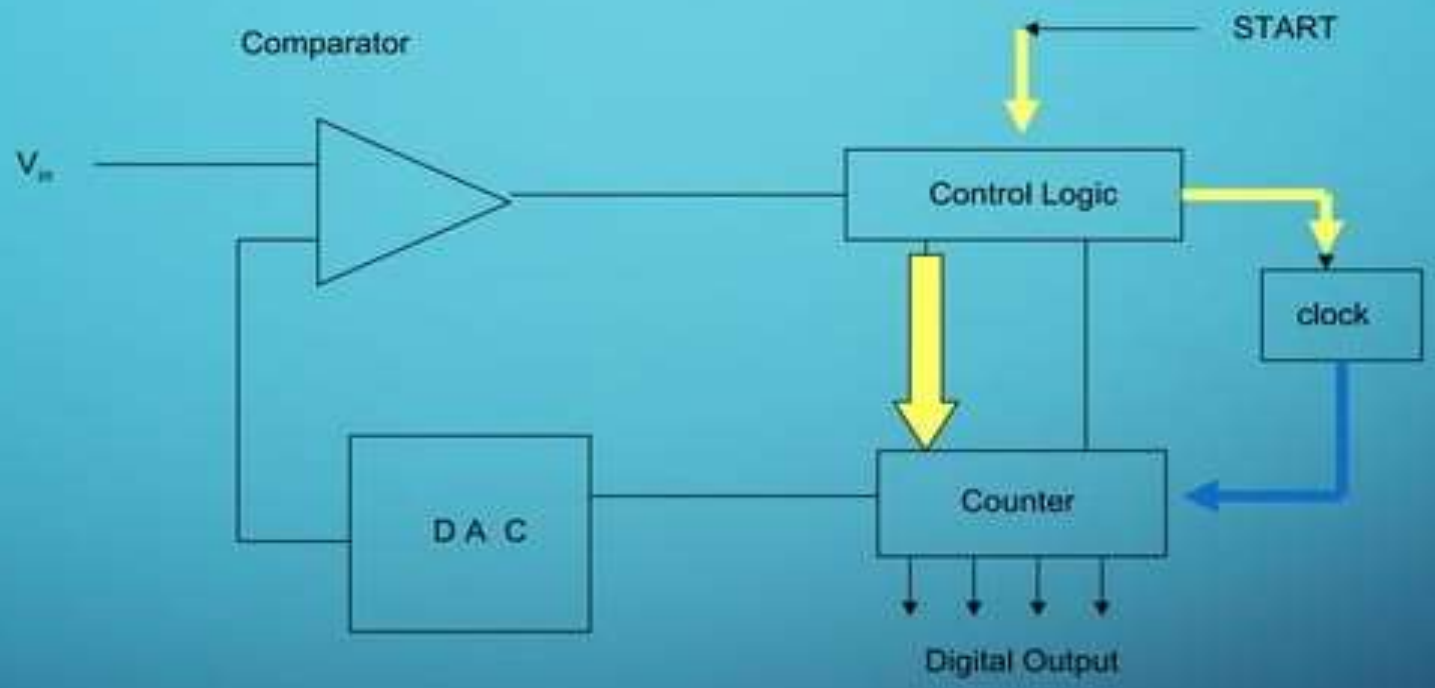
Comparator 6 - 7 => output **0**

Encoder Octal Input = sum(0011111) = 5

Encoder Binary Output = 1 0 1



COUNTER TYPE



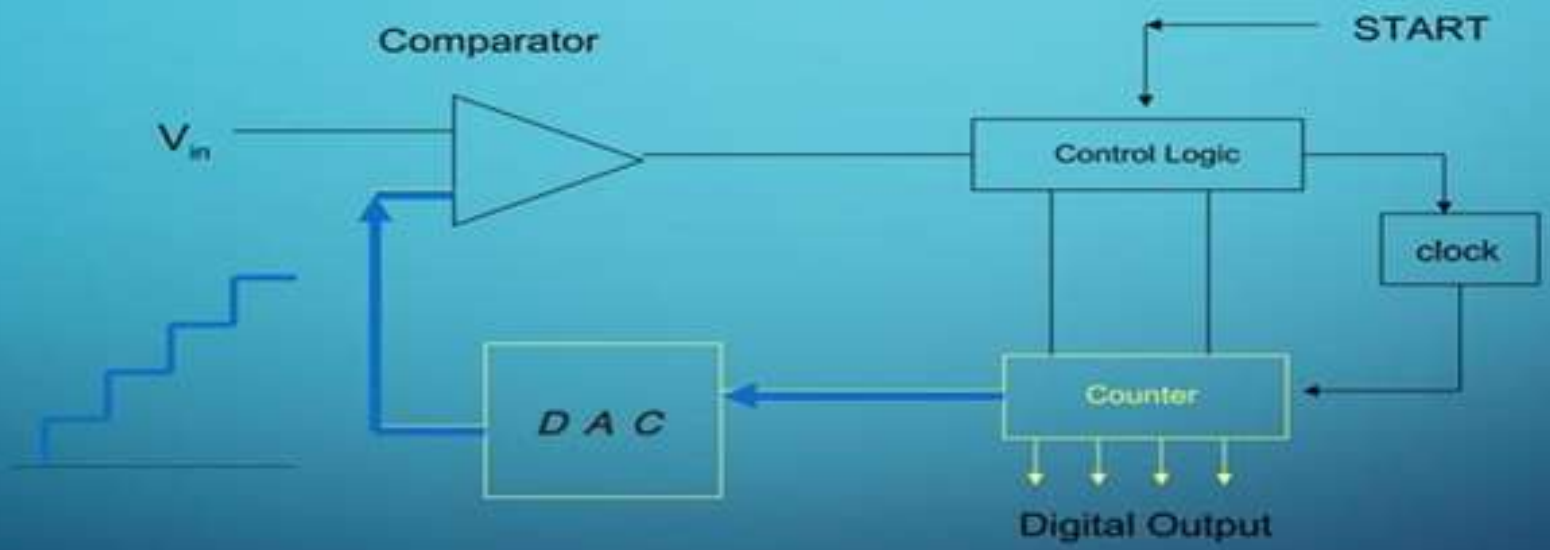
•When START is received,

•control logic initializes the system, (sets counter to 0), and

•turns on Clock sending regular pulses to the counter.

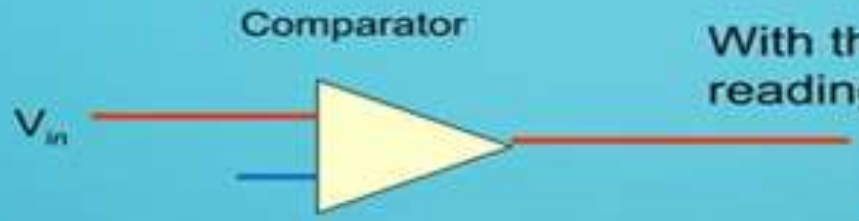
As the Clock sends regular pulses to the counter, the counter outputs a digital signal to the Digital-to-Analog converter

As the counter counts, its output to the D A C generates a staircase waveform ramp also increases to the comparator.



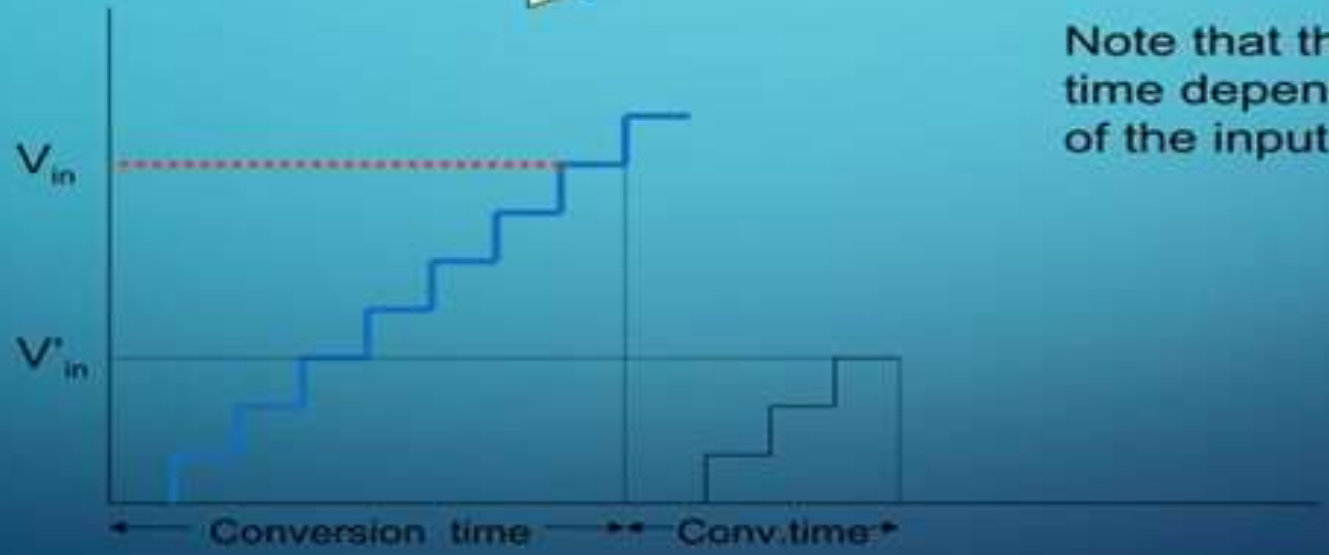
As the ramp voltage increases to the comparator, it rises closer and closer to V_{in} at which point the comparator shifts states

When the ramp voltage exceeds V_{in} , the comparator output shifts which signals the control logic to turn off the clock



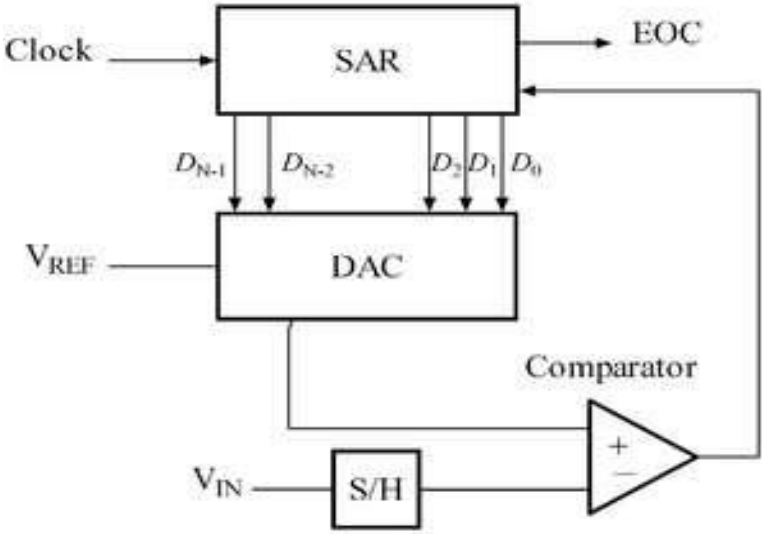
With the clock off, the counter reading is proportional to V_{in}

Note that the conversion time depends on the size of the input signal



Successive Approximation ADC

- Elements
- DAC = Digital to Analog Converter
- EOC = End of Conversion
- SAR = Successive Approximation Register
- S/H = Sample and Hold Circuit
- V_{in} = Input Voltage
- Comparator
- V_{ref} = Reference Voltage



Successive Approximation ADC

- Algorithm
- Uses an N-bit DAC and original analog results
- Performs a binary comparison of V_{DAC} and V_{in}
- MSB is initialized at 1 for DAC
- If $V_{in} < V_{DAC}$ ($V_{REF} / 2^{\wedge(N=1)}$) then MSB is reset to 0
- If $V_{in} > V_{DAC}$ ($V_{REF} / 2^{\wedge(N+1)}$) successive bit is set to 1
- Algorithm is repeated up to LSB
- At end DAC in = ADC out
- N-bit conversion requires N comparison cycles

Successive Approximation ADC - Example

- 5-bit ADC, V_{in}=0.6V, V_{ref}=1V
- Cycle 1 => MSB=1

SAR = **1** 0 0 0 0

$V_{DAC} = V_{ref}/2^{\wedge 1} = .5$ $V_{in} > V_{DAC}$ SAR unchanged = 1 0 0 0 0

DAC bit/voltage

Bit	4	3	2	1	0
Voltage	.5	.25	.125	.0625	.03125

- Cycle 2

SAR = 1 **1** 0 0 0

$V_{DAC} = .5 + .25 = .75$ $V_{in} < V_{DAC}$ SAR bit3 reset to 0 = 1 0 0 0 0

- Cycle 3

SAR = 1 0 **1** 0 0

$V_{DAC} = .5 + .125 = .625$ $V_{in} < V_{DAC}$ SAR bit2 reset to 0 = 1 0 0 0 0

- Cycle 4

SAR = 1 0 0 **1** 0

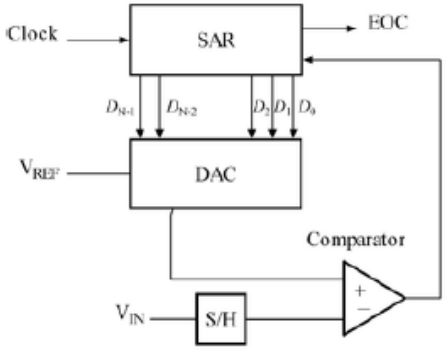
$V_{DAC} = .5+.0625=.5625$ $V_{in} > V_{DAC}$ SAR unchanged = 1 0 0 1 0

- Cycle 5

SAR = 1 0 0 1 **1**

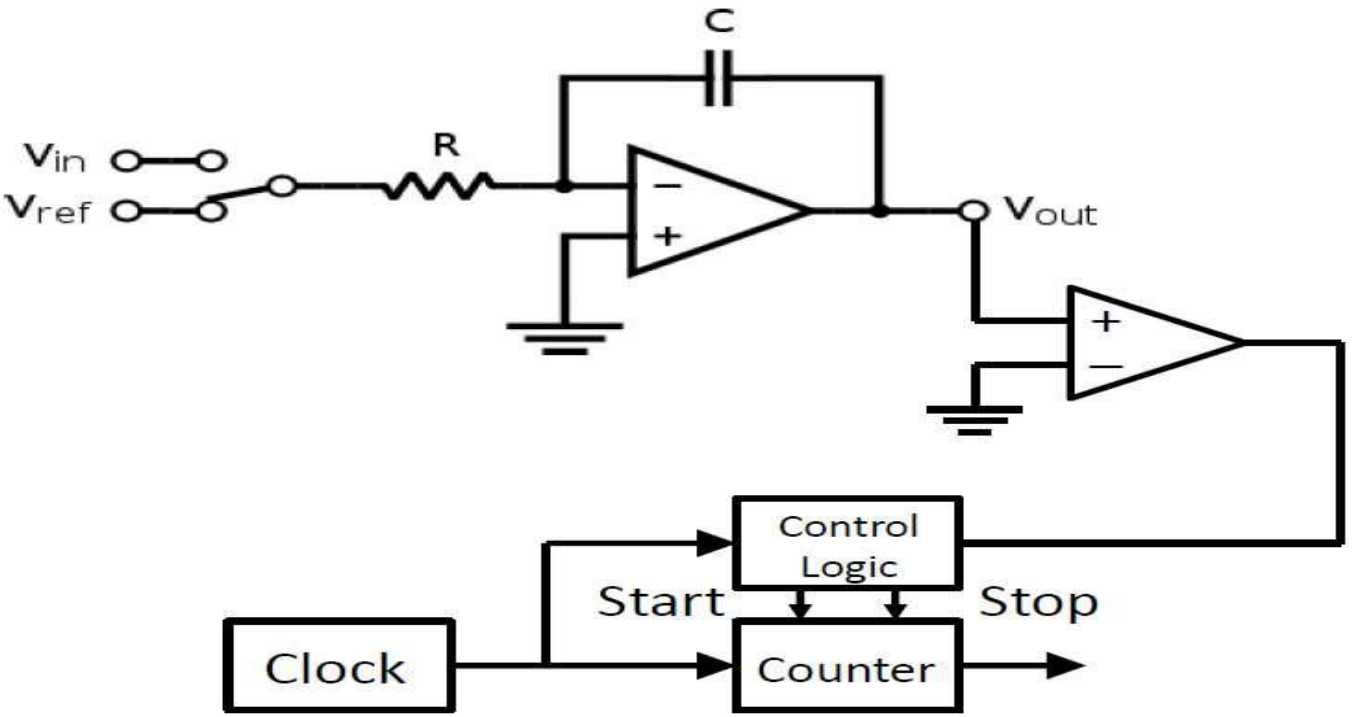
$V_{DAC} = .5+.0625+.03125=$ **.59375**

$V_{in} > V_{DAC}$ SAR unchanged = **1 0 0 1 1**



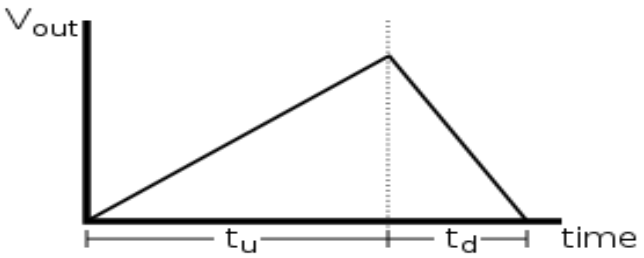
Dual Slope A/D Converter

- Also known as an Integrating ADC



Dual-Slope ADC – How It Works

- An unknown input voltage is applied to the input of the integrator and allowed to ramp for a fixed time period (t_u)
- Then, a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (t_d)
- The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measured run-down time period
- The run-down time measurement is usually made in units of the converter's clock, so longer integration times allow for higher resolutions
- The speed of the converter can be improved by sacrificing resolution



$$V_{in} = -V_{ref} \frac{t_d}{t_u}$$

UNIT – III
ACTIVE FILTERS & OSCILLATORS

ACTIVE FILTERS

- An electric filter is often a frequency selective circuit that passes a specified band of frequencies and block or attenuates signals of frequencies outside this band.
- Classified of filters

1. Analog or digital
2. Passive or active
3. Audio and radio frequency

Some commonly used active filters

1. Low pass filter
2. High pass filter
3. Band pass filter
4. Band reject filter
5. All Pass filter

Active filters: As their name implies, **Active Filters** contain active components such as operational amplifiers transistors or FET's within their circuit design. They draw their power from an external power source and use it to boost or amplify the output signal. These are generally used in communication and signal processing i.e. radio, television etc.

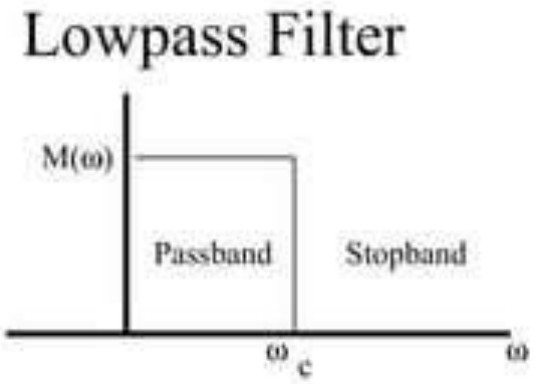
- Advantage of Active filters over Passive filters

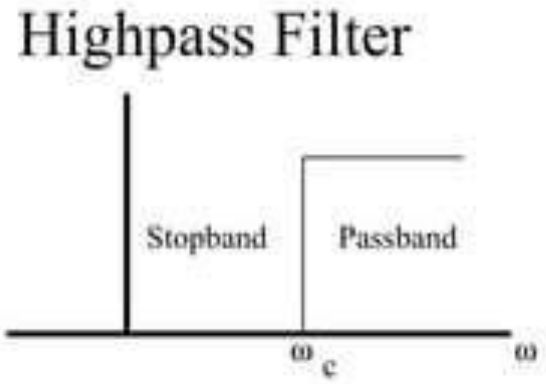
1. Gain and frequency adjustment flexibility
2. No loading problem (because of high i/p and low o/p resistance of op-amp)
3. Active filters are cheaper than passive filters

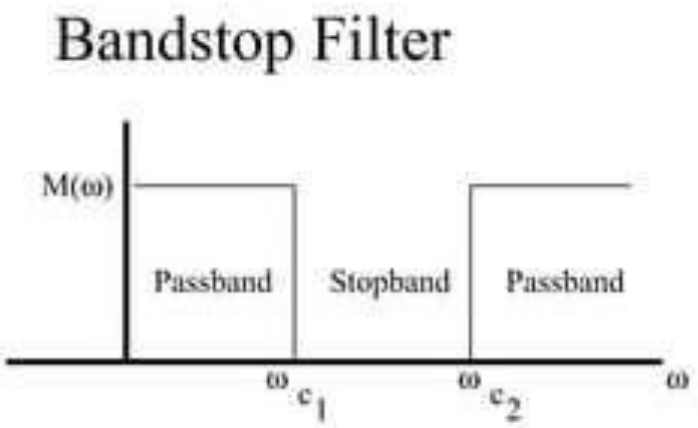
ACTIVE FILTERS

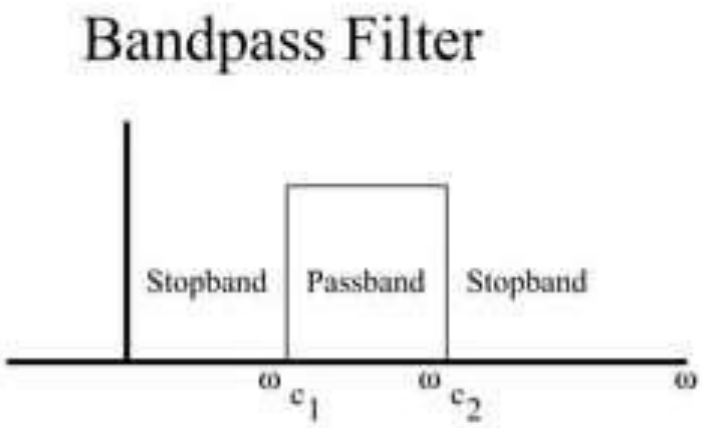
- No inductors
- Made up of op-amps, resistors and capacitors
- Provides arbitrary gain
- Generally easier to design
- High input impedance prevents excessive loading of the driving source
- Low output impedance prevents the filter from being affected by the load
- Easy to adjust over a wide frequency range without altering the desired response

FREQUENCY RESPONSE IDEAL FILTERS

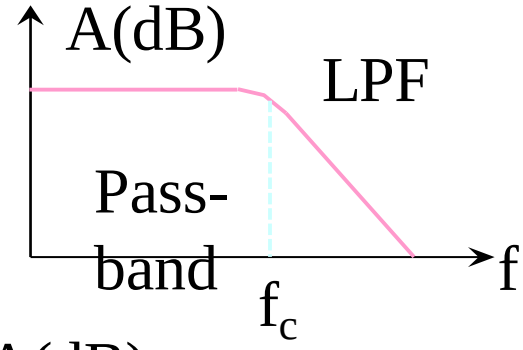


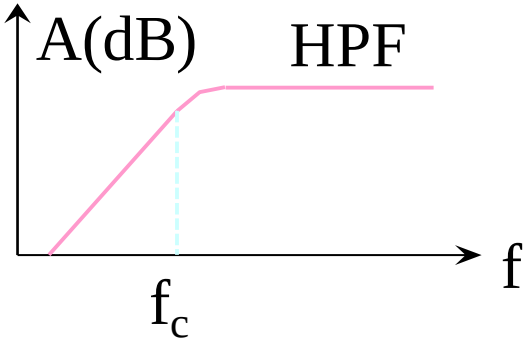


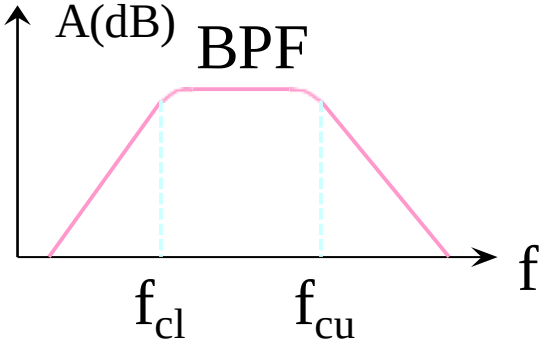


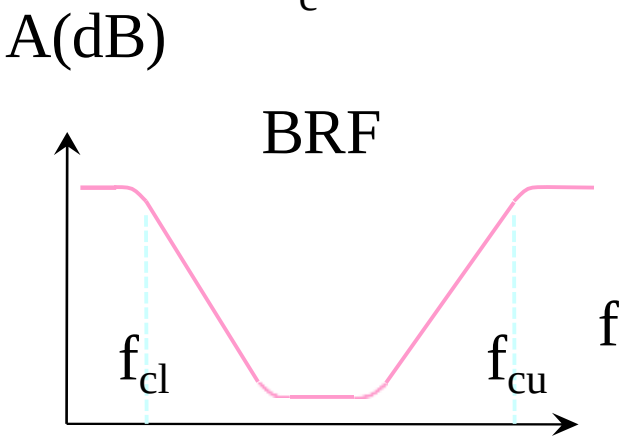


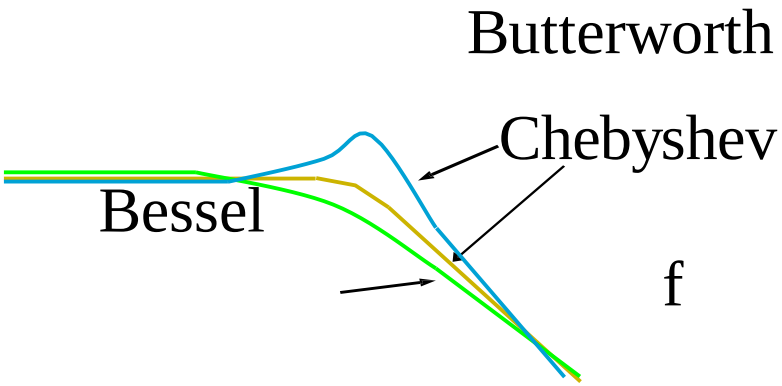
FREQUENCY RESPONSE OF PRACTICAL FILTERS











FIRST ORDER LOW PASS FILTER

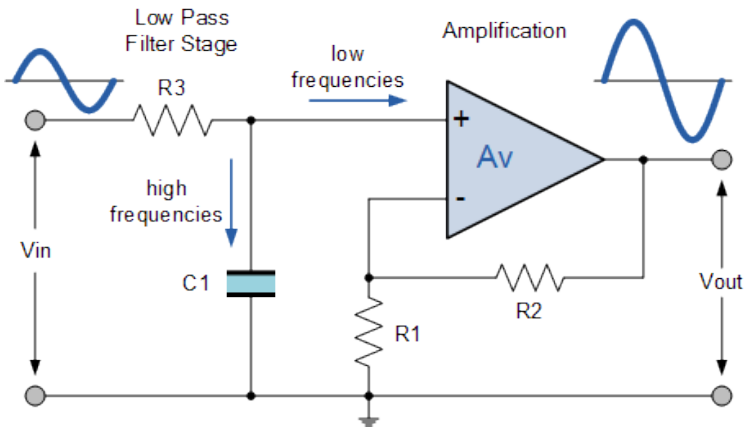


Fig.1 circuit diagram

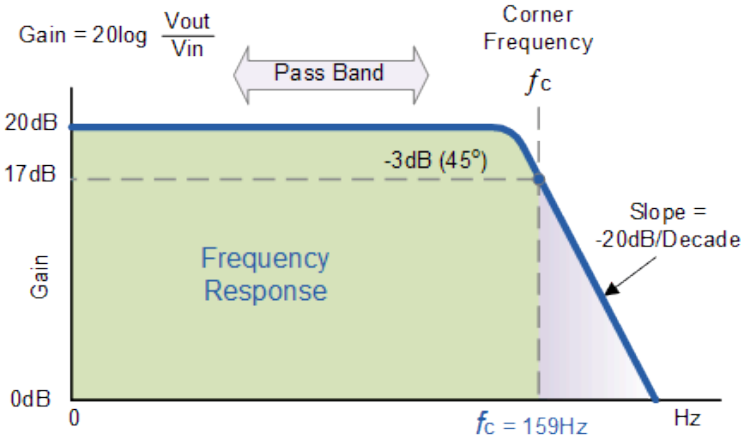


Fig.2 Frequency response

Note : The op-Amp is used in the non- inverting configuration ; hence it does not load down the RC Network.

Gain of a first-order low pass filter

$$Voltage\ Gain,\ (Av) = \frac{Vout}{Vin} = \frac{A_F}{\sqrt{1+\left(\frac{f}{fc}\right)^2}}$$

•Where:

- A_F = the pass band gain of the filter, (1 + R2/R1)
- f = the frequency of the input signal in Hertz, (Hz)
- fc = the cut-off frequency in Hertz, (Hz)

Thus, the operation of a low pass active filter can be verified from the frequency gain equation above as:

•1. At very low frequencies, $f < fc$ $\quad \frac{Vout}{Vin} \cong A_F$

•2. At the cut-off frequency, $f = fc$ $\quad \frac{Vout}{Vin} = \frac{A_F}{\sqrt{2}} = 0.707\,A_F$

•3. At very high frequencies, $f > fc$ $\quad \frac{Vout}{Vin} < A_F$

Designing Low pass filter

1. Choose a value of high cut off Frequency f_c
2. Select a value of C less than or equal to 1μF. Mylar or tantalum capacitor are recommended for better performance.
3. Calculate $R = 1/(2\pi f_c C)$
4. Select R1 and R2

   A_F = the pass band gain of the filter, (1 + R2/R1)

FIRST ORDER HIGH PASS FILTER

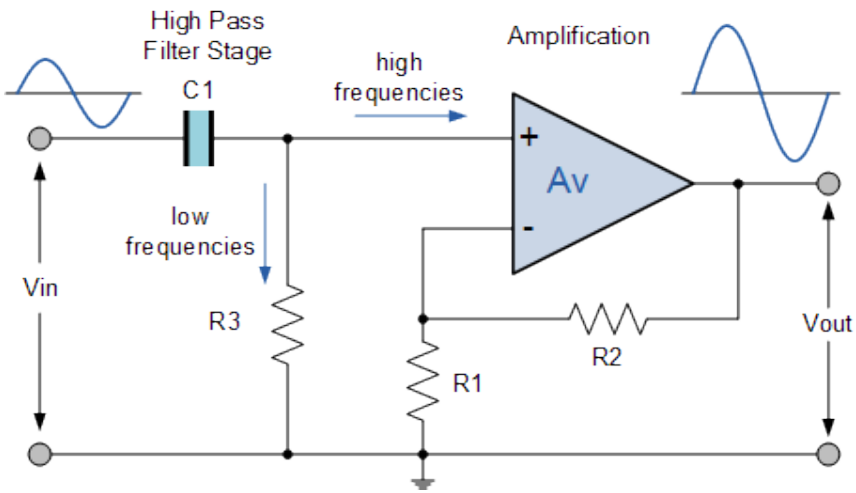


Fig circuit diagram

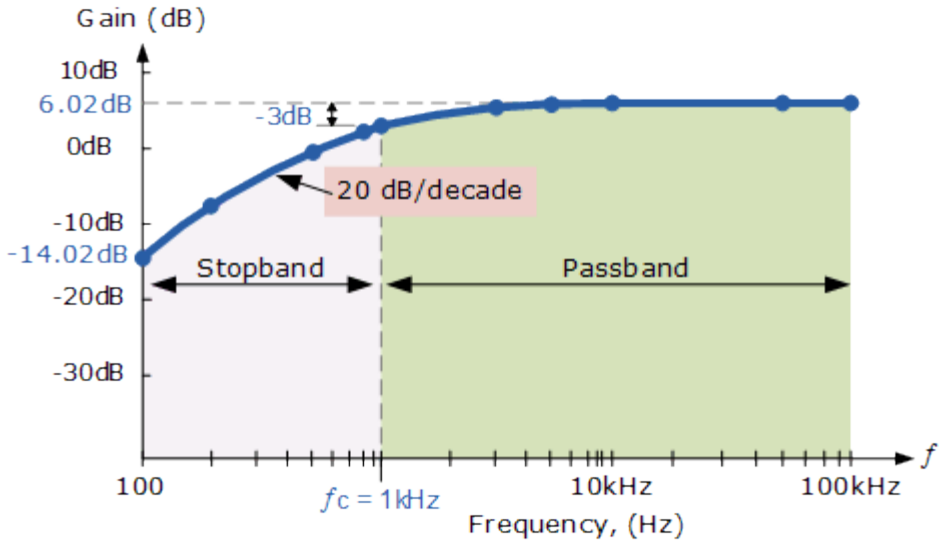


Fig . Frequency response

Gain of a first-order Active High pass filter

$$\text{Voltage Gain, (Av)} = \frac{\text{Vout}}{\text{Vin}} = \frac{A_F\left(\frac{f}{fc}\right)}{\sqrt{1+\left(\frac{f}{fc}\right)^2}}$$

•Where:

- A_F = the pass band gain of the filter, (1 + R2/R1)
- f = the frequency of the input signal in Hertz, (Hz)
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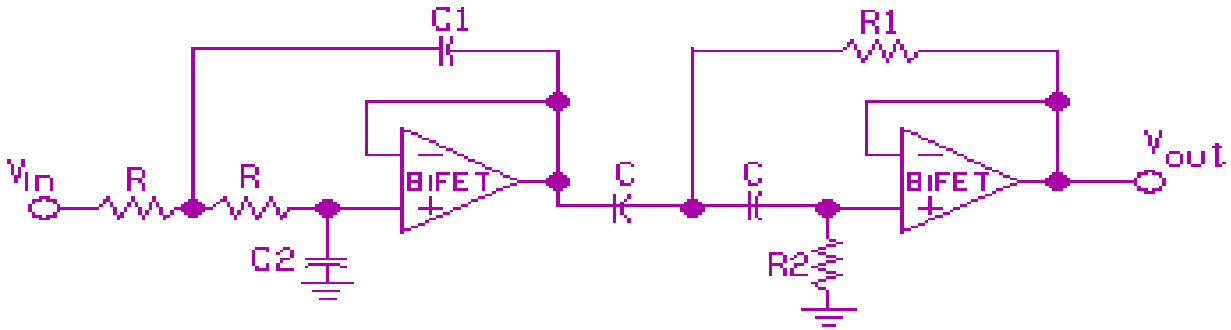
•3. At very high frequencies, $f > fc$ $\quad \frac{\text{Vout}}{\text{Vin}} \cong A_F$

BROAD BAND PASS FILTER

If BW and f_{centre} are given, then:

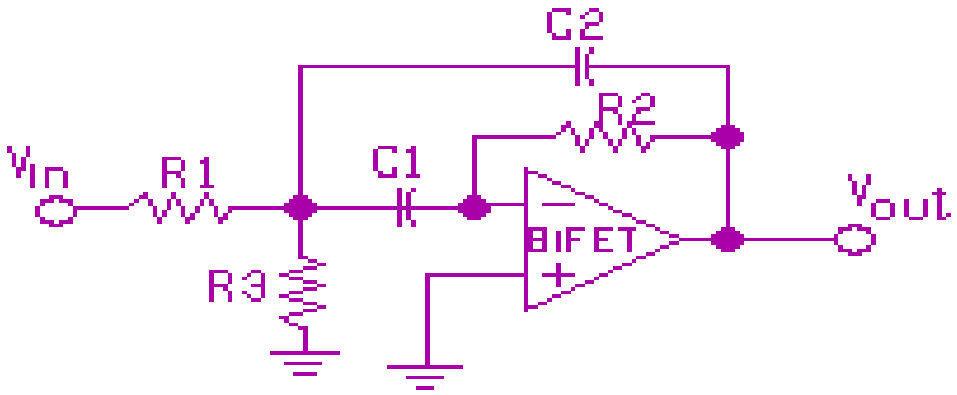
$$f_{cl} = \sqrt{\frac{BW^2}{4} + f_{ctr}^2} - \frac{BW}{2}\,;\; f_{cu} = \sqrt{\frac{BW^2}{4} + f_{ctr}^2} + \frac{BW}{2}$$

A *broadband* BPF can be obtained by combining a LPF and a HPF:



The Q of this filter is usually > 1.

NARROW BAND PASS FILTER



$$BW = \frac{f_{ctr}}{Q} = \frac{1}{2\pi R_1 C}$$

$C1 = C2 = C$

$R_2 = 2\,R_1$

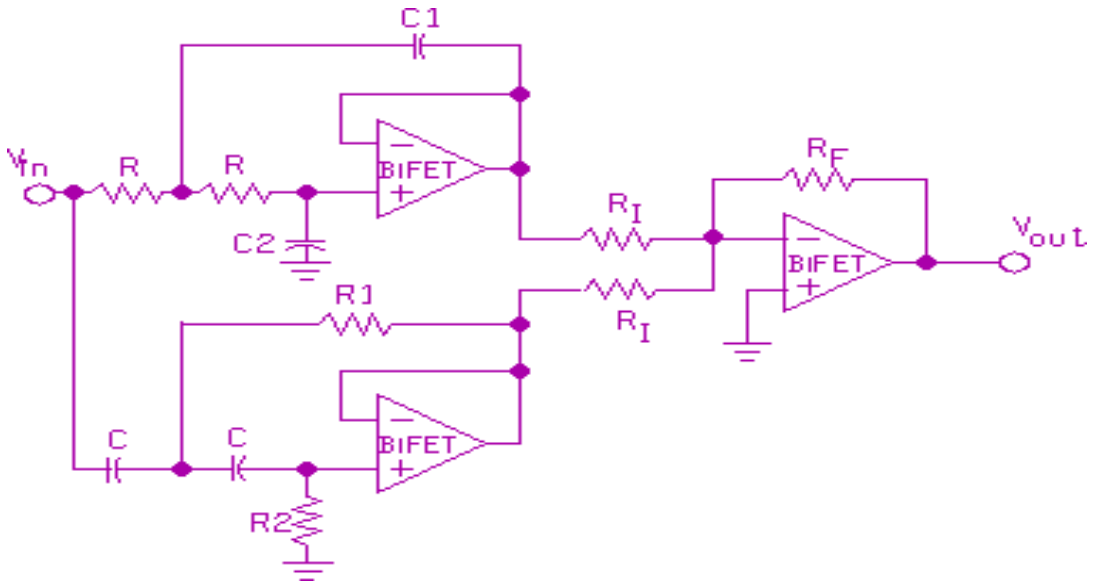
$$R_3 = \frac{R_1}{2Q^2 - 1}$$

$$f_{ctr} = \frac{1}{2\sqrt{2}\pi R_1 C}\sqrt{1 + \frac{R_1}{R_3}}$$

R_3 can be adjusted or trimmed to change f_{ctr} without affecting the BW. Note that $Q < 1$.

BROAD BAND REJECT FILTER

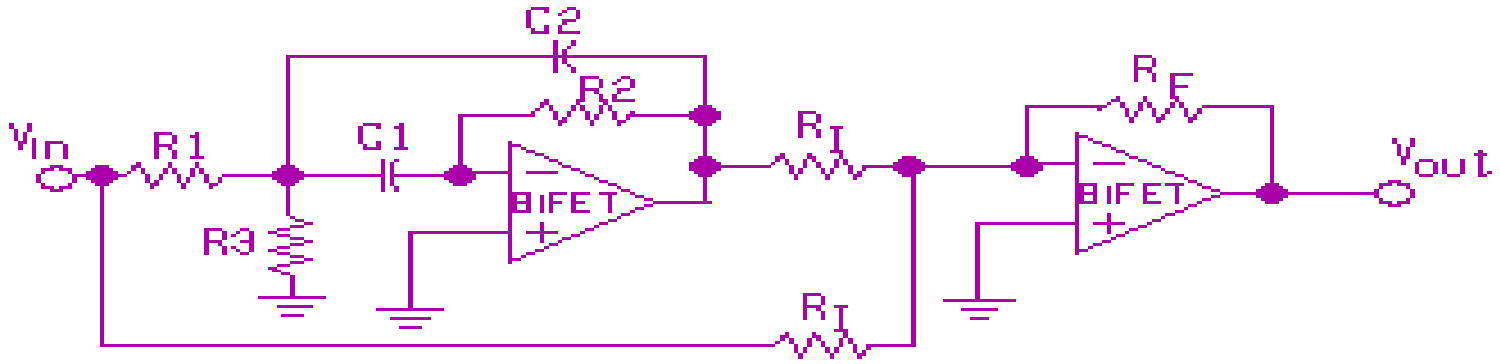
A LPF and a HPF can also be combined to give a broadband BRF:



1 2-pole band-reject filter

NARROW BAND REJECT FILTER

Easily obtained by combining the inverting output of a narrow-band BRF and the original signal:



The equations for R1, R2, R3, C1, and C2 are the same as before.$R_I = R_F$ for unity gain and is often chosen to be >> R1.

ALL PASS FILTER

- The All Pass Filter Design is one that passes all frequency components of the input signal without attenuation. Any ordinary wire can be used to perform this characteristic but the most important factor in an all pass filter is that it provides predictable phase shifts for different frequencies of the input signal.

$$V_o = V_{in}\left(\frac{1+j2\pi f\,CR}{1+j2\pi f\,CR}\right)$$

ALL PASS FILTER

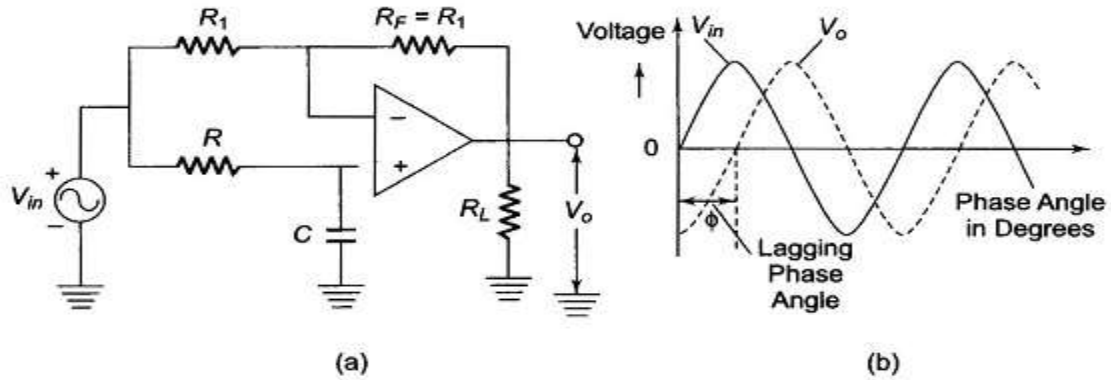


Fig. 15.22 (a) All Pass Filter Circuit (b) Input-Output Waveform Relation of an All Pass Filter (lagging)

$$V_o = V_{in}\left(\frac{1-j2\pi f\,CR}{1+j2\pi f\,CR}\right)$$

AUDIO OSCILLATORS

- An audio oscillator is useful for testing equipment that operates in the audio-frequency range. Such instruments always produce a sine-wave signal, variable in both amplitude and frequency, and usually provide a square-wave output as well. The maximum amplitude of the output waveform is typically on the order of 25 V_{rms}. whereas the range of frequencies covers at least the audio-frequency range from 20 Hz to 20 kHz. The most common output impedances for audio oscillators are 75 Ω and 600 Ω.

- The two most common audio-oscillator circuits are the Wien bridge oscillator and the phase-shift oscillator, both of which employ RC feedback networks. The Wien bridge offers some very attractive features, including a straightforward design, a relatively pure sine-wave output, and a very stable frequency.

RC PHASE SHIFT OSCILLATOR

- The second audio-oscillator circuit of interest is the phase-shift oscillator.
- The phase-shift network for the phase-shift oscillator, is an RC network made up of equal-value capacitors and resistors connected in cascade. Each of the three *RC* stages shown provides a 60^{o} phase shift. with the total phase shift equal to the required 180^{o}.

Cont’d

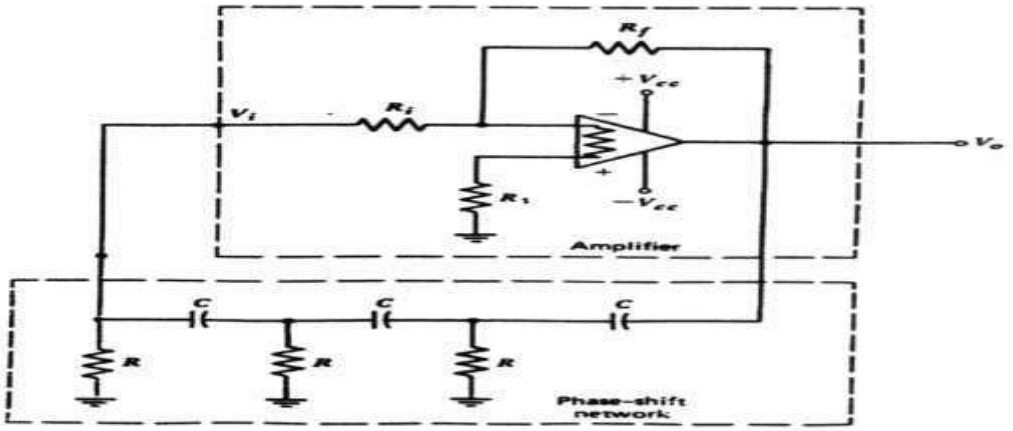


Fig.1-4 Basic phase-shift oscillator circuit.

Cont'd

- If the phase shift of the feedback network satisfies the 180^o phase-shift requirements, the imaginary components of Eq. 1-9 must be equal to zero or

$$\frac{1}{(\omega RC)^3} - \frac{6}{\omega RC} = 0$$

Cont'd

- The frequency of oscillation for the circuit can be determined by substituting $2\pi f_o$ for ω_o in Eq. 1-10 and solving for the frequency. The result is

$$f_o = \frac{1}{2\pi(\sqrt{6})CR}$$

Cont'd

$$\beta = \frac{V_i}{V_o} = \frac{1}{1 - 5\ x\ 6} = \frac{1}{29}$$

$$V_o = -29V_i$$

which means that the gain of the amplifier must be at least 29 if the circuit is to sustain oscillation.

Problem

Determine the frequency of oscillation of a phase-shift oscillator with a three-section feedback network consisting of 13-Ω resistors and 100-μF capacitors.

Solution

we can compute the frequency Of oscillation as

$$f = \frac{1}{2\pi\sqrt{6}RC}$$

$$= \frac{1}{(2\pi\sqrt{6})(13\Omega)(100\mu F)} = 50Hz$$

WIEN BRIDGE OSCILLATOR

- The Wien bridge oscillator is essentially a feedback amplifier in which the Wien bridge serves as the phase-shift network. The Wien bridge is an ac bridge, the balance of which is achieved at one particular frequency.

Cont'd

- The basic Wien bridge oscillator is shown in Fig. 1-2. as can be seen. the Wien bridge oscillator consists of a Wien bridge and an operational amplifier represented by the triangular symbol. Operational amplifiers are integrated circuit amplifiers and have high-voltage gain, high input impedance, and low output impedance. The condition for bala

$$Z_1 Z_4 = Z_2 Z_3 \quad \textbf{(1-2)}$$

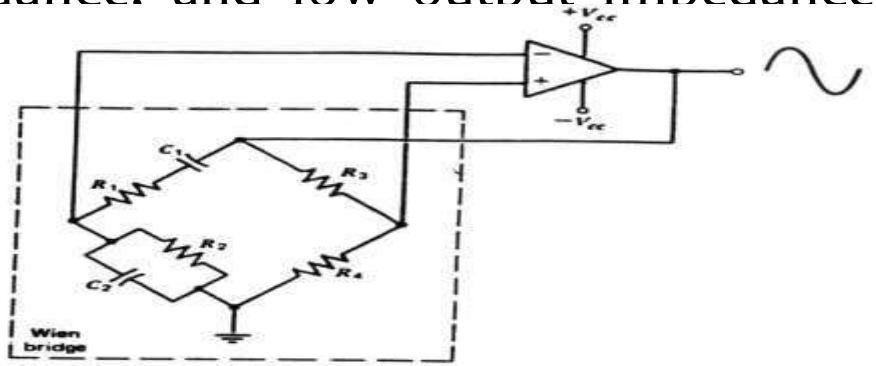


Fig. 1-2 Wien bridge oscillator.

Cont'd

Where

$$Z_1 = R_1 - j/\omega C_1$$

$$Z_2 = \frac{R_2(-j/\omega C_2)}{R_2 - j/\omega C_2} = \frac{-jR_2}{-j + R_2\omega C_2}$$

$$Z_3 = R_3$$

$$Z_4 = R_4$$

Substituting the appropriate expressions into Eq. 1-2 yields

$$\left(R_1 - \frac{j}{\omega C_1}\right)\left|R_4 = \right|\left(\frac{-jR_2}{-j + R_2\omega C_2}\right)\left|R_3\right. \quad (1\text{-}3)$$

Cont'd

- if the bridge is balanced both the magnitude and phase angle of the impedances must be equal. These conditions are best satisfied by equating real terms and imaginary terms. Separating and equating the real terms in Eq. 1-3 yields.

$$\frac{R_3}{R_4} = \frac{R_1}{R_2} + \frac{C_2}{C_1} \qquad (1\text{-}4)$$

Separating and equating imaginary terms in Eq. 1-3 yields

$$\omega C_1 R_2 = \frac{1}{\omega C_2 R_1} \qquad (1\text{-}5)$$

Cont'd

- Where $\omega = 2\pi f$ Substituting for to in Eq. 1-5, we can obtain an expression for frequency which is

$$f = \frac{1}{2\pi\,(C_1 R_1 C_2 R_2)^{1/2}} \qquad (1\text{-}6)$$

- If $C_1 = C_2 = C$ and $R_1 = R_2 = R$ then Eq. 1-4 simplifies yield

$$\frac{R_3}{R_4} = 2 \qquad (1\text{-}7)$$

Cont'd

- and from Eq. 1-6 we obtain

$$f = \frac{1}{2\pi RC} \qquad (1\text{-}8)$$

Where

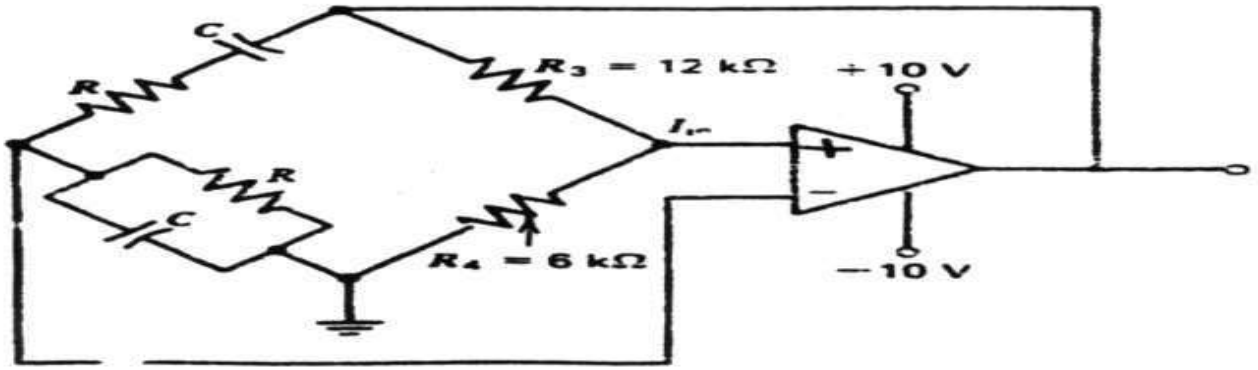
f = frequency of oscillation of the circuit in Hertz

C = capacitance in farads

R = resistance in ohms

Problem

Determine the frequency of oscillation of the Wien bridge oscillator shown in Fig. 1-3 if $R = 6\Omega$ and C = 0.003 F.



Solution

we compute the frequency as

$$f = \frac{1}{2\pi RC}$$

$$= \frac{1}{(2\pi)(6k\Omega)(0.003\mu F)}$$

$$= 8.885\,kHz$$

3. Quadrature Oscillator :-

Signals that are of same frequency but have a phase shift of 90° w.r.t each other are called Quadrature signals. An example of quadrature signals is sine and cosine waves shown in fig ②. The ckt of a quadrature oscillator that generates both sine and cosine wave is shown in fig ①.

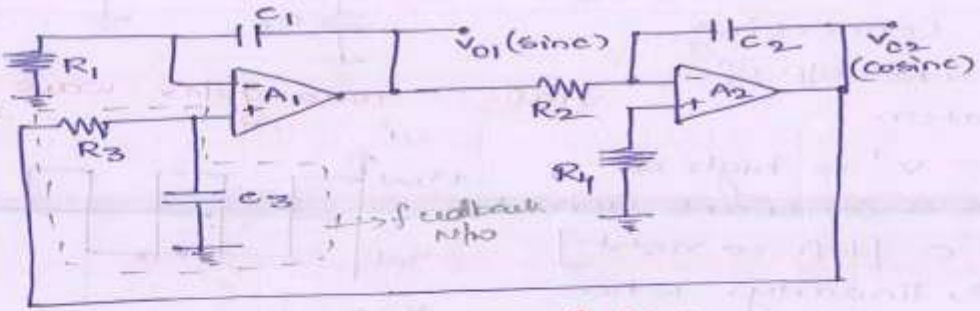


fig ①: Quadrature Oscillator

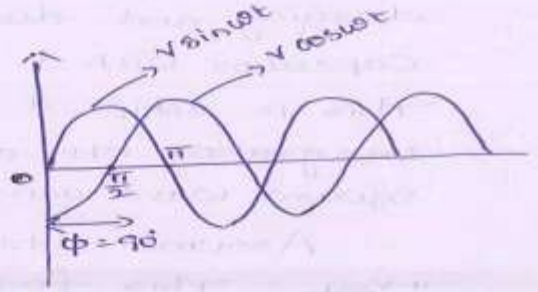


fig ②:

The ckt consists of two op-Amps A_1 and A_2. The op-Amp A_2 is inverting integrator. Due to inverting nature it adds −180° phase and due to integrating nature it adds −90° phase. So total phase shift due to A_2 is −270°. while potential divider $R_3 - C_3$ along with A_1 contributes remaining −90° and hence total phase shift around a loop is −360° i.e, 0°. This ensures positive feedback satisfying Barkhausen condition. This is possible only at frequency 'f_0' at which oscillator produces sine and cosine waveforms. This 'f_0' is frequency of oscillation and is given by,

$$f_0 = \frac{1}{2\pi RC}, \text{ where, } R_1C_1 = R_2C_2 = R_3C_3 = RC \quad \text{——— ①}$$

TRIANGULAR WAVE GENERATOR

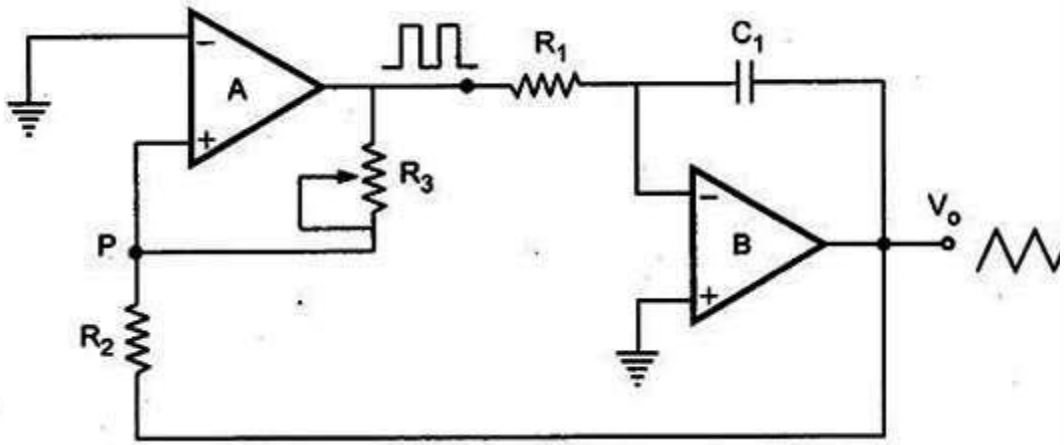


Fig: Schematic of Triangular wave generator

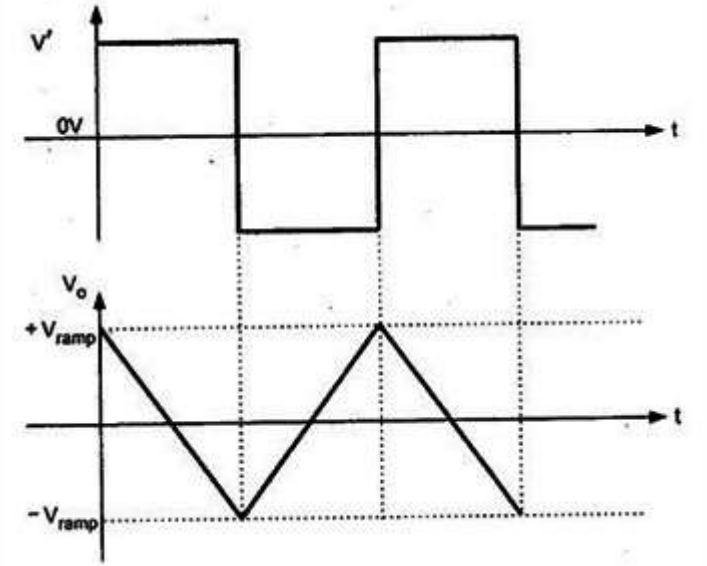


Figure 1.2: Output of comparator and integrator

Cont’d

- It consists of a comparator (A) and an integrator (B) as shown in figure 1.1. The output of comparator A is
- a square wave of amplitude $\pm Vsat$ and is applied to the inverting (-) input terminal of the integrator B. The output of integrator is a triangular wave and it is feedback as input to the comparator A through a voltage divider $R2R3$.

- To understand circuit operation, assume that the output of comparator A is at $+Vsat$. This forces a constant current through C to give a negative going ramp at the output of the integrator, as shown in the Fig.
- Therefore, one end of voltage divider is at a voltage $+Vsat$ and the other at the negative going ramp. When the negative going ramp reaches a certain value $-Vramp$, the output of comparator A switches from positive
- saturation to negative saturation ($-Vsat$). This forces a reverse constant current (right to left) through C to give a positive going ramp at the output of the integrator, as shown in the figure. When positive going ramp reaches $+Vramp$, the effective voltage at point p becomes slightly above O V. As a result, the output of comparator A switches from negative saturation to positive saturation ($+Vsat$). The sequence then repeats to give triangular wave at the output of integrator B.

SAWTOOTH WAVE GENERATOR

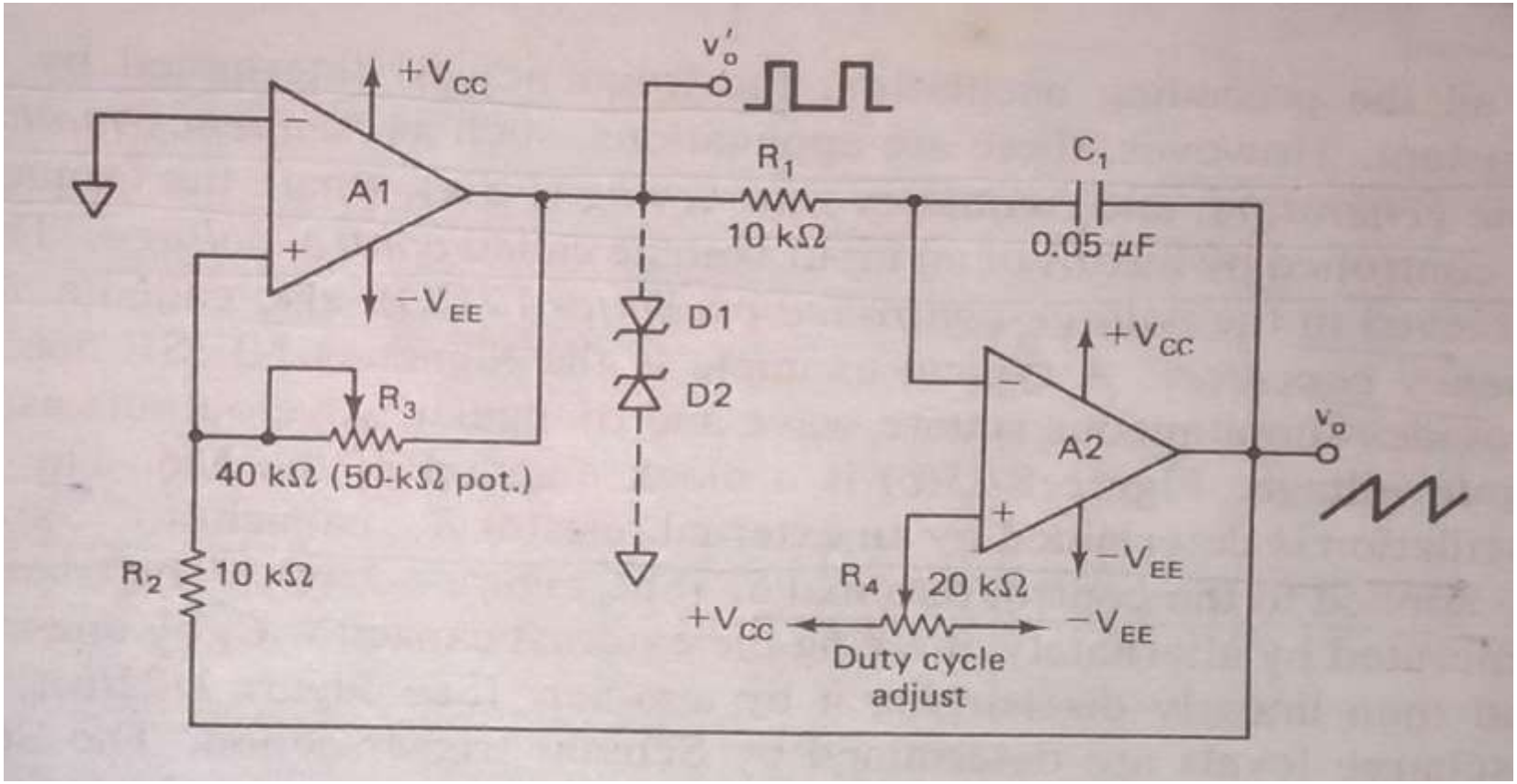


Fig: Schematic of Sawtooth wave generator

Cont'd

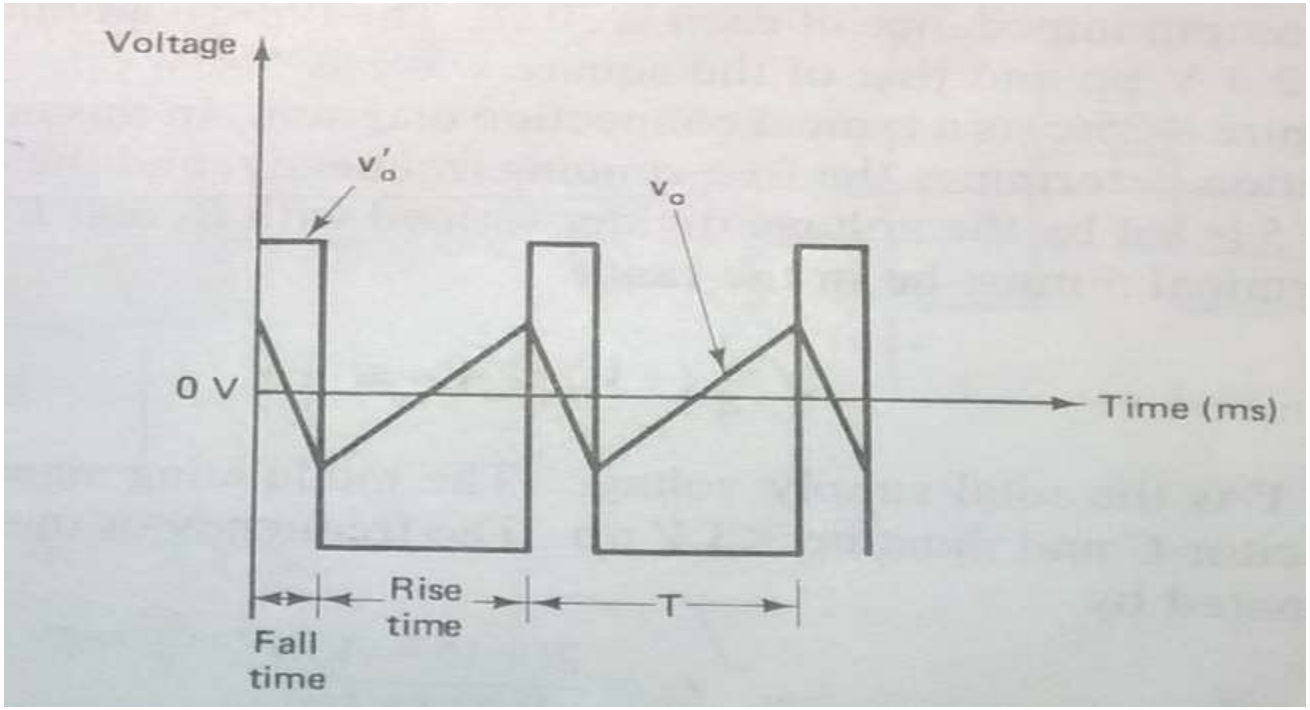


Fig: Output of sawtooth wave generator

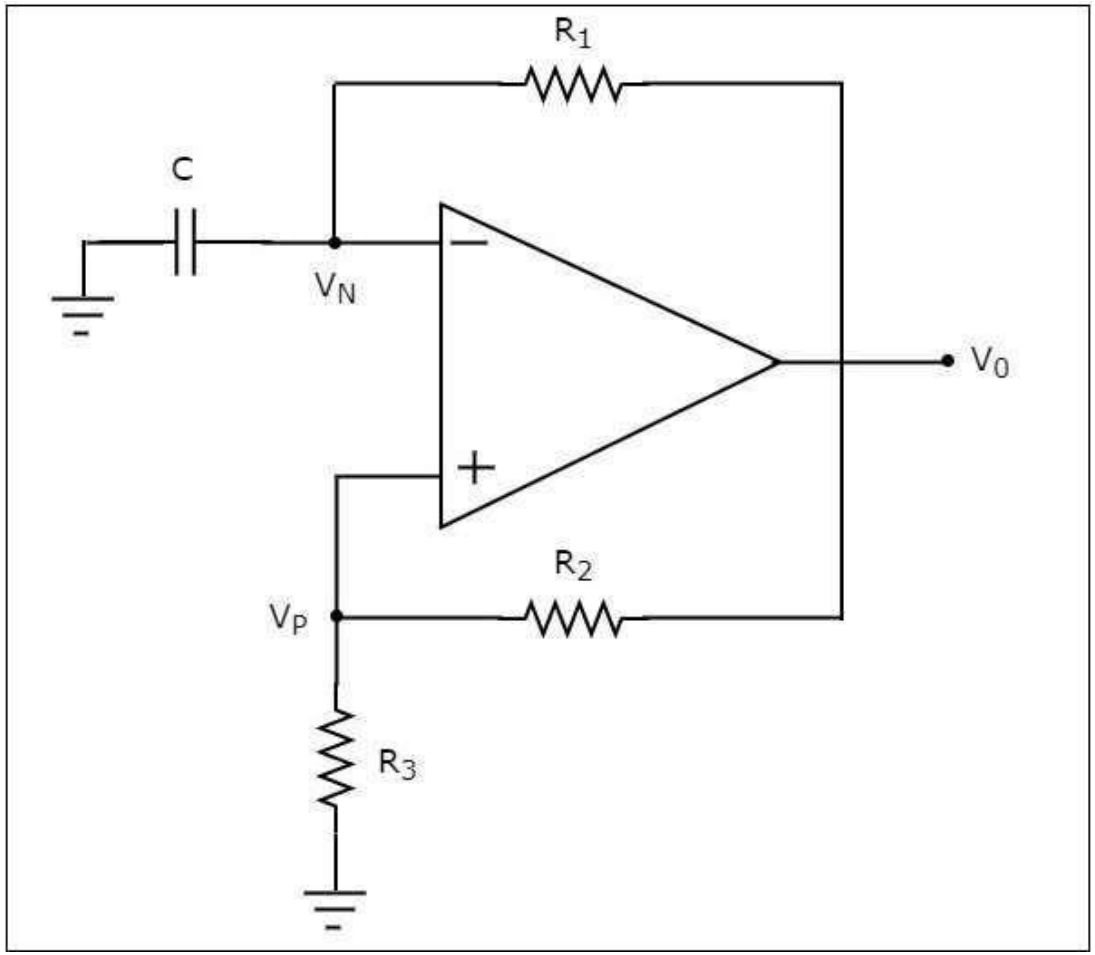
Cont'd

- Sawtooth waveform can be also generated by an asymmetrical astable multivibrator followed by an integrator as shown in figure 1.3. The sawtooth wave generators have wide application in time-base generators and pulse width modulation circuits. The difference between the triangular wave and sawtooth waveform is that the rise time of triangular wave is always equal to its fall of time while in saw tooth generator, rise time may be much higher than its fall of time , vice versa. The triangular wave generator can be converted in to a sawtooth wave generator by injecting a variable dc voltage into the non-inverting terminal of the integrator.

Cont'd

- In this circuit a potentiometer is used. Now the output of integrator is a triangular wave riding on some dc level that is a function of *R*4 setting. The duty cycle of square wave will be determined by the polarity and amplitude of dc level. A duty cycle less than 50% will cause output of integrator be a sawtooth.
- With the wiper at the centre of *R*4, the output of integrator is square wave. Use of the potentiometer is when the wiper moves towards $-VEE$,the rise time of the sawtooth become longer than the fall time. If the wiper moves towards $+VCC$, the fall time becomes more than the rise time.

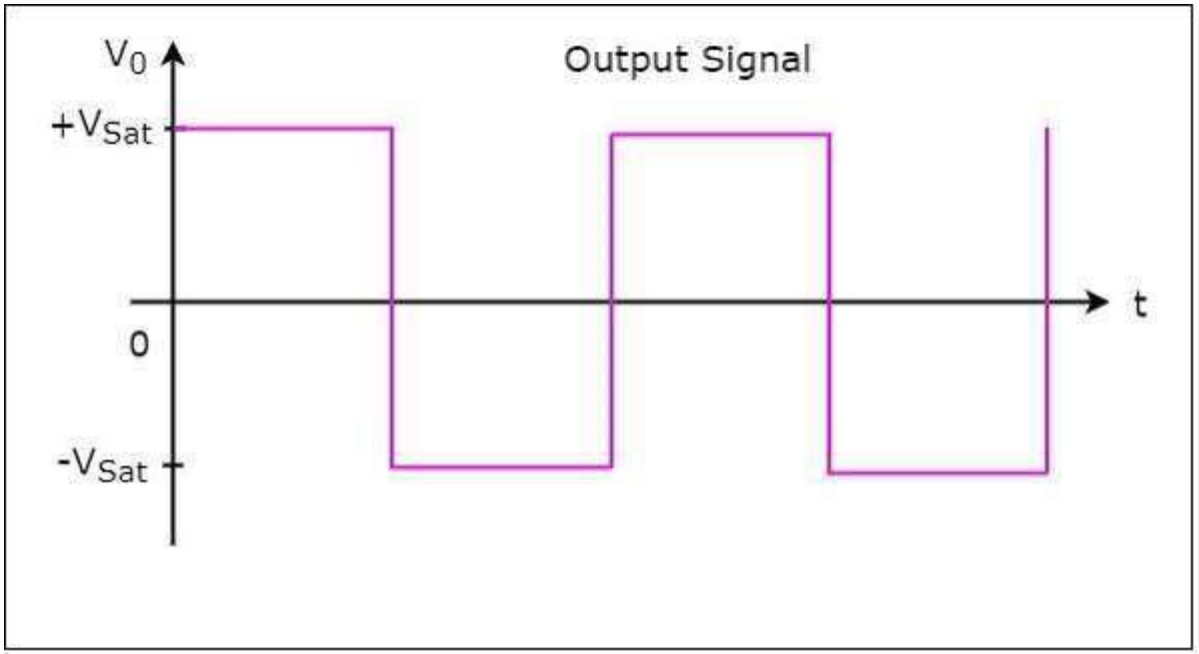
SQUARE WAVE GENERATOR



Cont’d

- A **square wave generator** is an electronic circuit which generates square wave. This section discusses about op-amp based square wave generators.
- The **circuit diagram** of a op-amp based square wave generator is shown in the following figure

Output waveform of square wave generator



Voltage Controlled Oscillator (VCO) :-

A VCO is an oscillator in which the frequency of oscillations can be controlled by an externally applied voltage. The VCO provides the linear relationship b/w the applied voltage and the oscillation frequency. The Applied voltage is called "control voltage (V_c)". The control of frequency with the help of control voltage is also called "voltage to frequency conversion". Hence, VCO is also called "voltage to frequency converter". Practically VCO is used to produce square and Triangular waveforms whose frequency is controlled by control voltage.

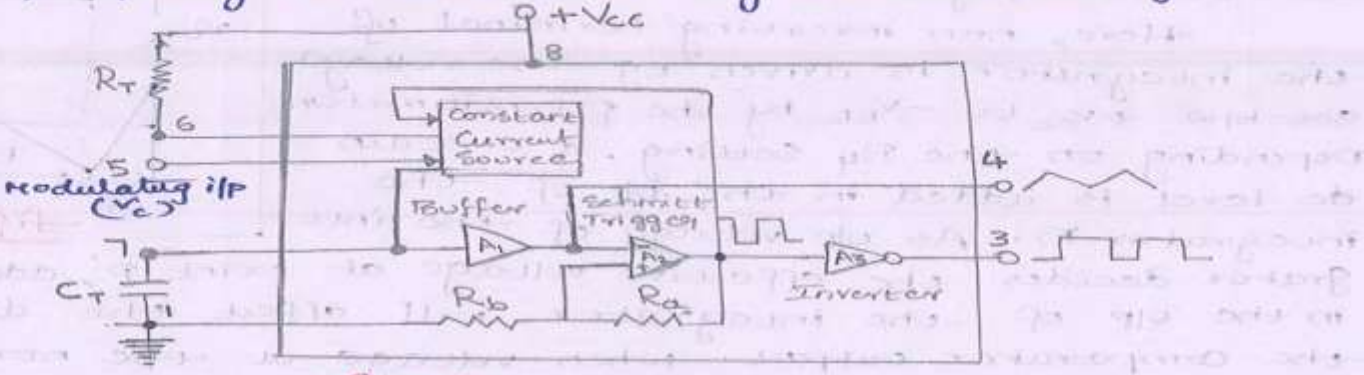


fig (b)

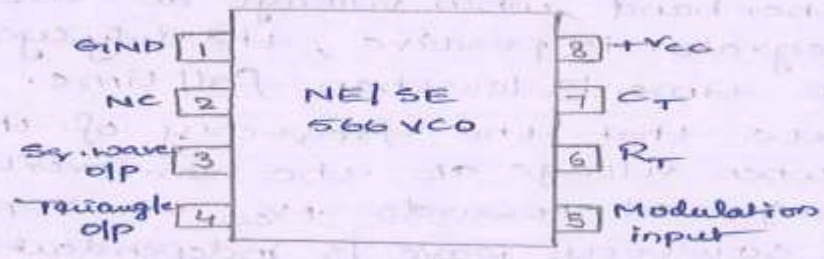


fig (a) pin diagram

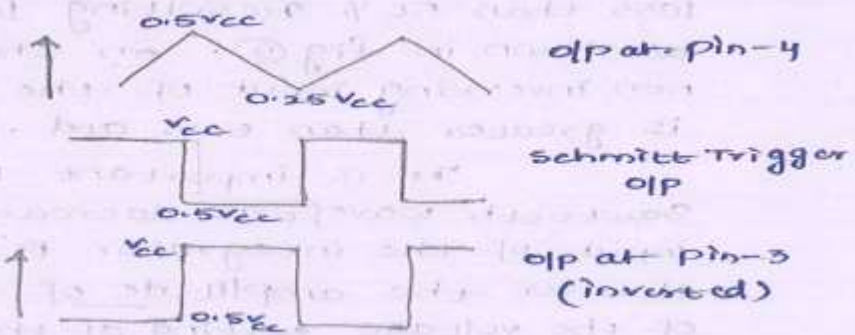


fig (c) :- output waveform

A common type of VCO available in IC form is Signetics NE/SE 566. The pin configuration and basic block diagram of 566 VCO are shown in fig 1(a), (b). From fig (b), a timing capacitor C_T is linearly charged or discharged by a constant current source. The amount of current can be controlled by changing the voltage 'V_c' applied at the modulating input (pin-5) or by changing the timing resistor 'R_T' external to IC chip. The voltage at pin-6 is held at the same voltage as pin-5. Thus, if the modulating voltage at pin-5 is increased, the voltage at pin 6 also increases, resulting in less voltage across R_T and thereby decreasing the charging current.

Operation :-

The voltage across the capacitor C_T is applied to the inverting input terminal of Schmitt Trigger A_2 via buffer Amplifier A_1. The o/p voltage swing of the Schmitt Trigger is designed to V_{cc} and $0.5V_{cc}$. If $R_a = R_b$ in the positive feedback loop, the voltage at the non-inverting input terminal of A_2 swings from $0.5V_{cc}$ to $0.25V_{cc}$. In fig (c), when the voltage on the capacitor C_T exceeds $0.5V_{cc}$ during charging, the o/p of the Schmitt Trigger goes LOW ($0.5V_{cc}$). The capacitor now discharges and when it is at $0.25V_{cc}$, the o/p of Schmitt Trigger goes HIGH (V_{cc}). Here, capacitor charges and discharges for the same amount of time. This gives a Triangular voltage waveform across 'C_T' which is also available at pin-4. The o/p ~~waveform~~ sq. wave of the Schmitt Trigger is inverted by inverter A_3 and is available at pin-3. The o/p waveforms are shown in fig (c).

→ The frequency of the VCO is,

$$f_o = \frac{2(V_{cc} - V_c)}{C_T R_T V_{cc}} \quad \text{——— (1)}$$

The o/p freq. can be changed either by (i) R_T, (ii) C_T or (iii) the voltage 'V_c' at the modulating input terminal pin-5.

The voltage to frequency conversion factor is,

$$K_v = \frac{8 f_o}{V_{cc}} \quad \text{——— (2)}$$