UNIT-1

JUNCTION DIODE CHARACTERISTICS

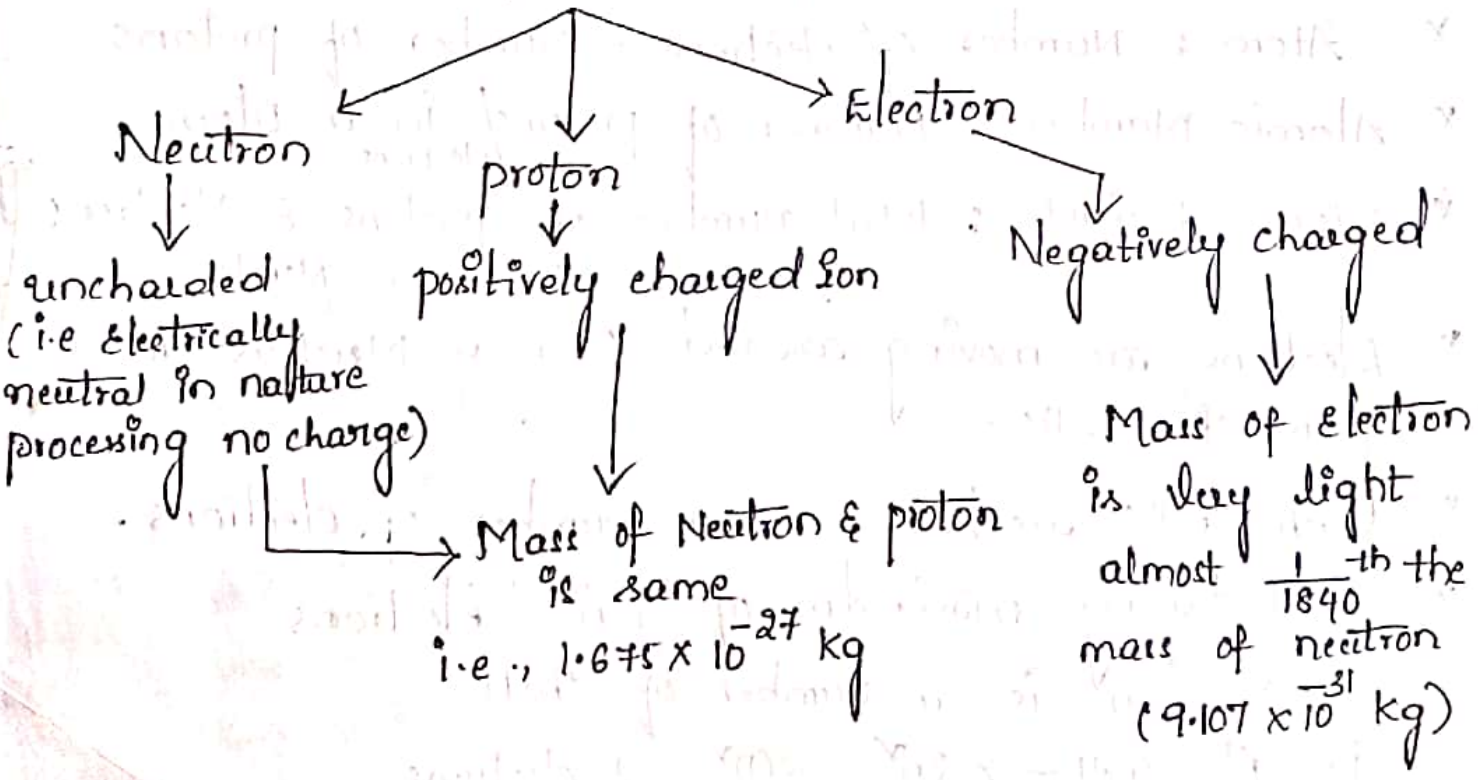
To understand the working of p-n junction diode it is necessary to know the basics of materials (P-type & N-type) and also to understand the how diodes, Transistors, Thyristors and Integrated circuits work, it is necessary to know the basic physics behind the behaviour of Semi-conductor material (Semi-conductor is one of type of Material).

Introduction :-

∝ The Matter which occupies the space may be 3 types are Solid, Liquid (or) gaseous.

∝ Infact, according to the modern Electron theory, matter is composed of the three fundamental particles, which are invisible to bare eyes.

These are : particles



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ATOM :-

* The atoms have a planetary type of structure according to Bohr model.
* All protons and neutrons are bound together at the centre of an atom - which called "Nucleus", while all the Electrons are moving round the Nucleus.

So, Nucleus can thought of as a Central sun, about which electrons revolve in a particular fashion like the planets.

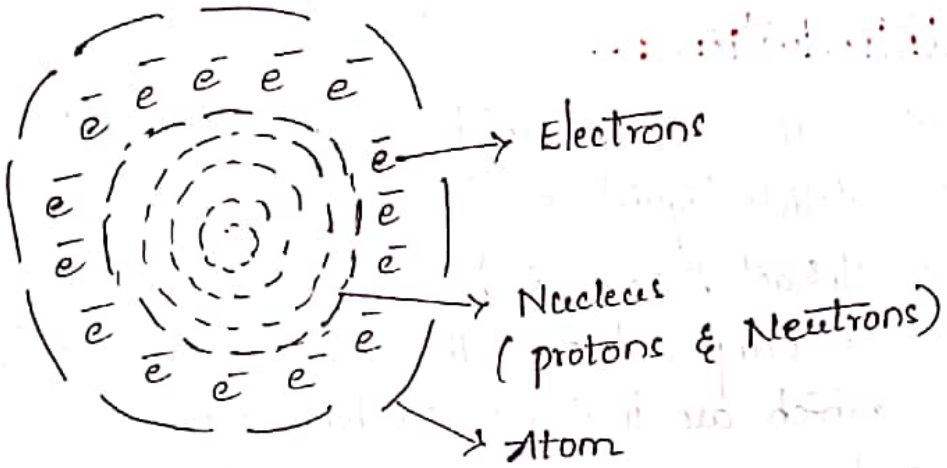

Fig: Structure of an "Atom"

* Atom : Number of electrons = Number of protons
* Atomic Number : Number of protons/electrons in a atom
* Atomic Weight : Total number of protons & Neutrons in Nucleus
* Electrons are moving around over a Nucleus in the form of shells.
* Each shells are having some number of electrons.
* Shell having maximum of "$2n^2$" electrons where, 'n' is a number of shell.

  i.e 1st shell → $2n^2 = 2(1)^2 = 2$ electrons
  2nd shell → $2n^2 = 2(2)^2 = 8$ electrons etc.

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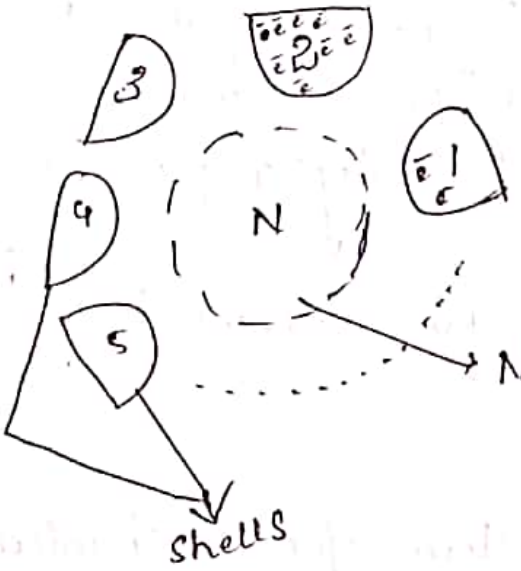

Here 1, 2 1 3 . . . . are shells around nucleus which are having group of electrons

* Each shell has an Energy level associated with it.

Valence shell & Valence electron :-

The closer of an electron is to the Nucleus, stronger force of attraction, because of closest to the nucleus, while the shell which is farthest (far) from the nucleus is having week force of attraction and the electrons nucleus are very loosely bound to the Nucleus. Such electron in the outermost shell are responsible for the electrical & chemical characteristics of an atom.

"The outermost shell is called "Valence shell" and the electrons in the shell are called as "Valence electrons".

* Valence electrons in Outermost shell are having "highest Energy level".

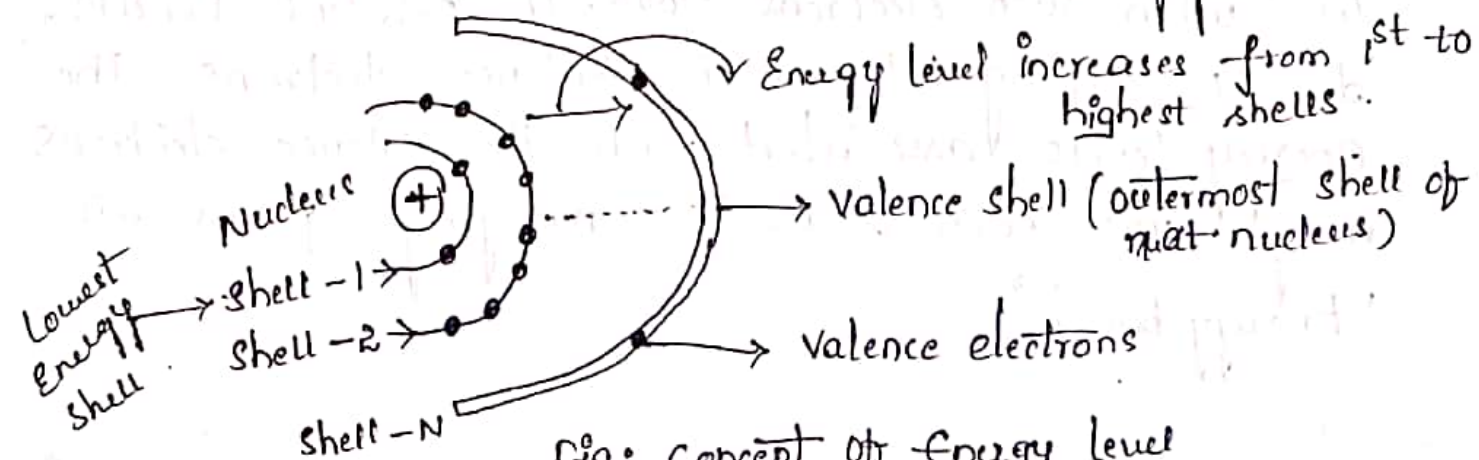

fig: concept of Energy level

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Free electron :-

The electron which is not subjected to the "force" of attraction of the nucleus is called "free electron". Such free electrons are basically responsible to the "flow of current".

"More the number of free electrons better is the conductivity of the metal".

Materials :-

Material is a broad term for a chemical substance (or) mixture of substances that constitute a thing.

** Energy band Theory :-

Nucleus

Shell nearer to nucleus → having low energy level

Shell farthest (far) to nucleus → highest energy level

* Due to high energy levels of electrons in outermost shell, electrons can be easily extracted from outermost shell to another orbit of an atom.

* The valence electrons are shared by forming a bond with the valence electrons of an adjacent atom. Such bonds are called "Covalent bond"

* Now, the valence electrons posses highest energy level when such electrons forms the covalent bonds, due to coupling between the valence electrons, the energy levels associated with the valence electrons merge into each other, this merging forms an "Energy band".

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Energy band :- It describes the ranges of Energy level bands. The electrons in same orbit exhibits different energy levels The grouping of this different Energy levels is called "Energy band.

Types of Energy bands :-

1. Valence band
2. Conduction band
3. forbidden band or gap.

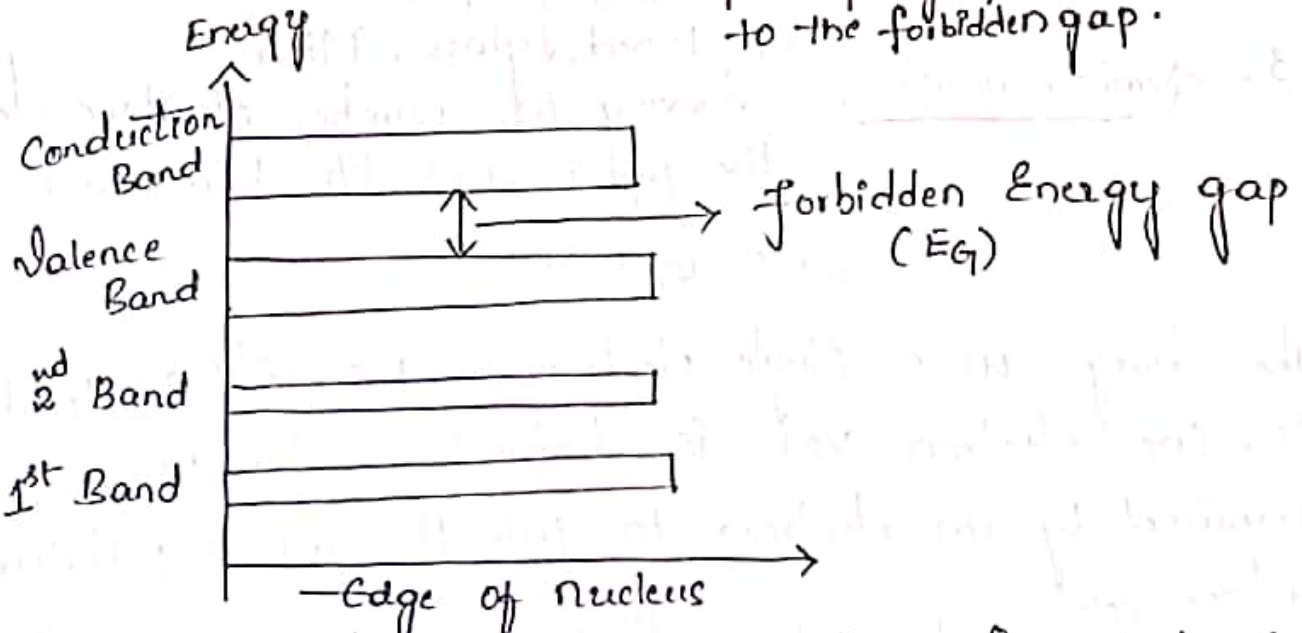
Valence band : Energy band formed due to merging of Energy levels associated with the Valence electrons is "Valence band".

Conduction band : Energy band formed due to merging of Energy levels associated with the free-electrons is called "Conduction-band".

forbidden band : Energy band which is separating the Conduction band and Valence band is called "forbidden band".

→ In order to push an electron from Valence band to Conduction band the applied external energy in the form of light/heat must be equal to the forbidden gap.

Energy band diagram :-



* Energy associated with forbidden band is called as "Energy gap (E_G) it is measured in the unit electron volt

$1eV = 1.6 \times 10^{-19} J$

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The Graphical representation of the energy band in a solid is called "Energy band diagram".

* For any given type of material the forbidden Energy gap may be large, small (or) Non-exisistent.
* Based on width of forbidden energy gap, the materials are classified into 3-types.

Classification of Materials :-

1. Conductors
2. Insulators
3. Semiconductors

1. **Conductors** :- These are having Large no. of free electrons Exist at room temparature. So E_G (forbidden engy gap) does not Exist. Conduction and Valence bands are Overlapped.

   Ex: Copper, Aluminium, Silver

2. **Insulators** :- No free electrons. The gap of energy is Very high b/w conduction & Valence band nearly 7ev.

   Ex: Wood, glass, Mica

3. **Semiconductors** :- having felw number of free electrons the gap is 1ev b/w both bands.

   Ex :- Ge, Si

The charge on a Single electron is 1.6×10^{-19} Coulomb So, One electron volt is defined as the energy required by an electron to fall through a potential of one volt.

$$1ev = 1.6 \times 10^{-19} (C) \times 1(V)$$

$$(1ev = 1.6 \times 10^{-19} J)$$

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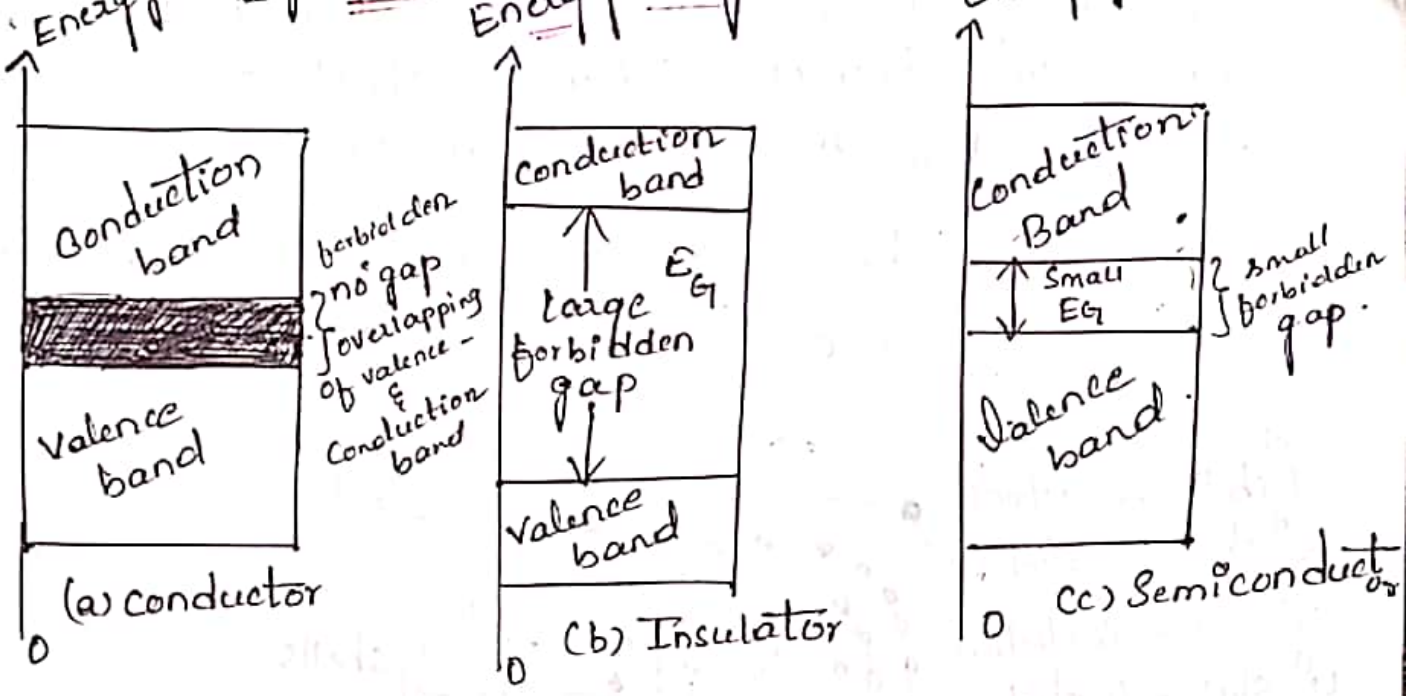
Fig Energy-Band Diagram for material



- In our Syllabus, having Semiconductor material we need to know in depth of Semiconductors.)!

** Semiconductors :-

* It is an important category of materials, which are neither insulators nor conductors.
* The forbidden gap in such material is very Narrow as shown in above figure, really gap is "1 ev".
* In such materials (Semiconductors), the energy provided by the heat at room temparature is sufficient to lift the electrons from the Valence band to conduction band. so at room temparature Semiconductors are capable of conduction. but at 0°K or absolute zero(-273°C), all the Semiconductors are acts as Insulators. Here forbiddden gap is dep nds on temparature.

for Si & Ge $E_G = 1.21 - 3.6 \times 10^{-4} \times T$ ev (Si°) approx. 1.12 ev at room temp 300°K

$E_G = 0.785 - 2.23 \times 10^{-4} \times T$ ev (Ge) at room temp 0.72 ev

$\therefore$ 'T' is Absolute temperature in °K.

* Si, Ge are widely used Semiconductor materials in electronic devices.

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* Among Silicon & Germanium, Silicon is most widely used why because, Silicon is stable while depends of temparature than Germanium i.e

The Germanium has a Nucleus with 32 protons and 32 electrons in the electrons are distributed as follows:

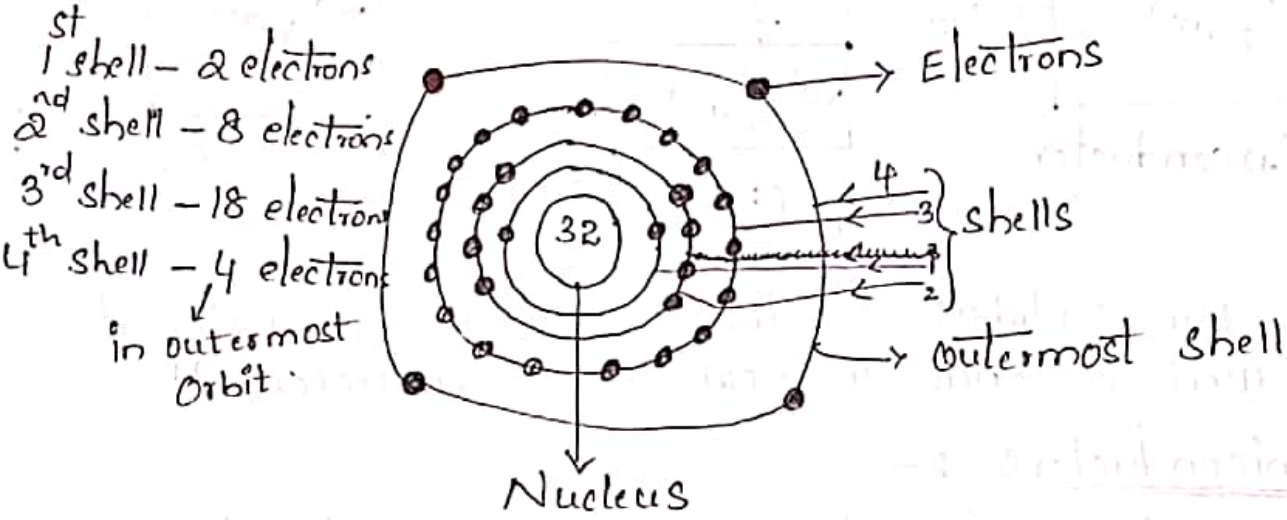

fig: Germanium atom

* The Silicon has Nucleus with 14 protons and 14 Electrons.

2 electrons – 1st shell/orbit.
8 electrons – 2nd shell/orbit.
4 electrons – outer most orbit.

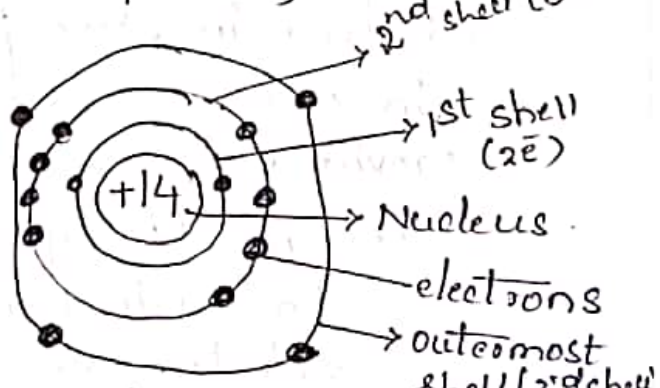

fig: Silicon atom (4 electrons).

* Looking at the structure of Silicon & Ge atom it can be seen that Valence shell (outer most shell) of silicon is 3rd shell, while Valence shell of "germanium" is 4th shell. Hence Valence electrons of Ge are at larger distance from Nucleus than Valence electrons of Silicon.

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hence Valence electrons ē of Ge are more loosely bound to the Nucleus than those of Silicon. Thus Valence electrons of Ge can easily escape from the atom, due to Very small additional Energy imparted to them. So at high temparature, Ge becomes unstable than Silicon. So, we mostly prefer "Si" than "Ge" Semiconductor material.

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Classification of Semi-conductors :-

2 types 1. Intrinsic Semiconductors
2. Extrinsic Semiconductors

1. Intrinsic Semiconductors :-

* A Sample of Semiconductor in its purest form is called an "Intrinsic Semiconductor".
* Impurity content is Very Very small
* for understanding the conduction in an Intrinsic Semi-conductor let us study the Crystalline structure of an Intrinsic Semiconductor.

Crystal structure of Intrinsic Semiconductor :-

Consider an atomic structure of an intrinsic Semi-Conductor like Silicon. An outermost shell of an intrinsic Semiconductor of Silicon has 4 electrons. each of these 4 electrons form a bond with another Valence electron of the neighbouring atoms. This is nothing but sharing of electrons. Such bonds are called "Covalent bonds" The atoms align themselves to form a 3Dimensional uniform pattern called a "Crystal".

But 3D structure is very difficult to represent pictorially. Hence the symbolic 2D structure is used to represent a 3D form as shown figure below.

Crystal

* The Covalent bonds are represented by a pair of dotted lines encircling the two electrons forming the Covalent bond.

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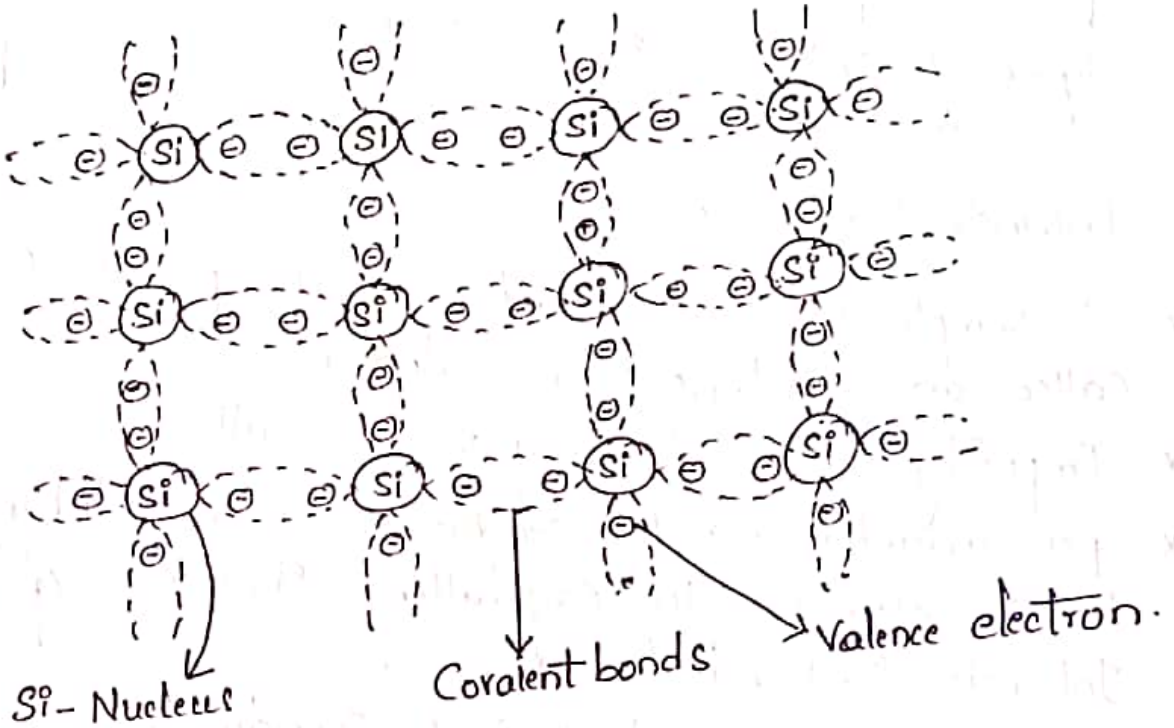

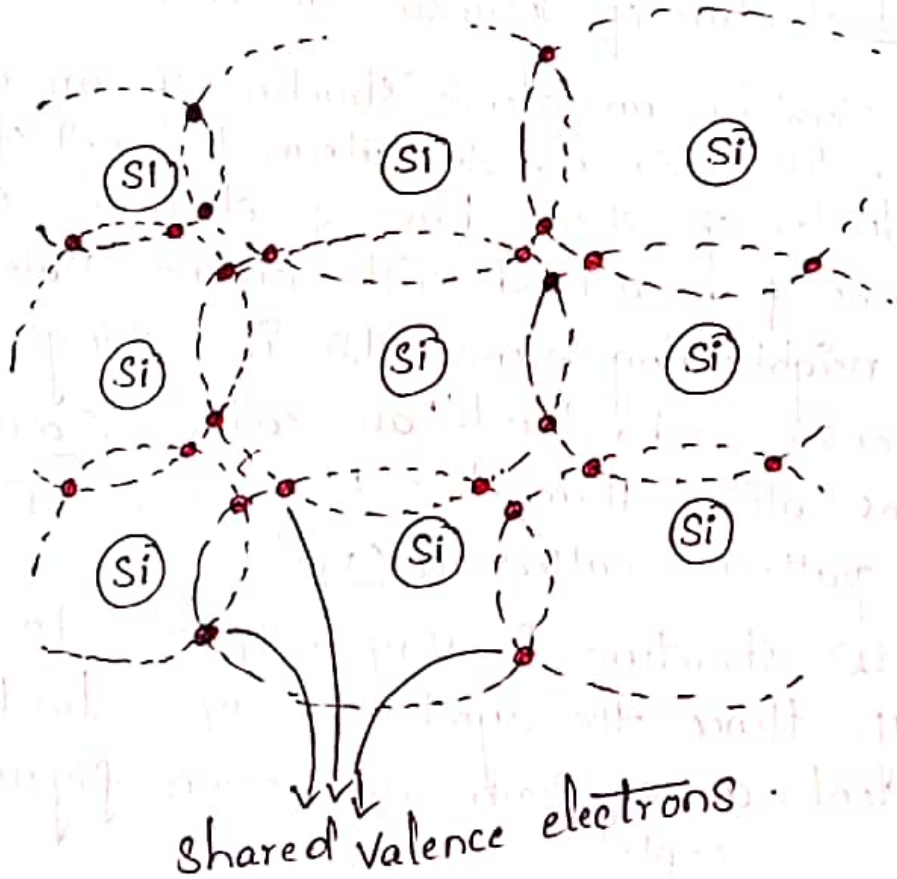

fig (a) & (b) : Two Dimensional representation of Silicon crystal.

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sharing of valence electrons and

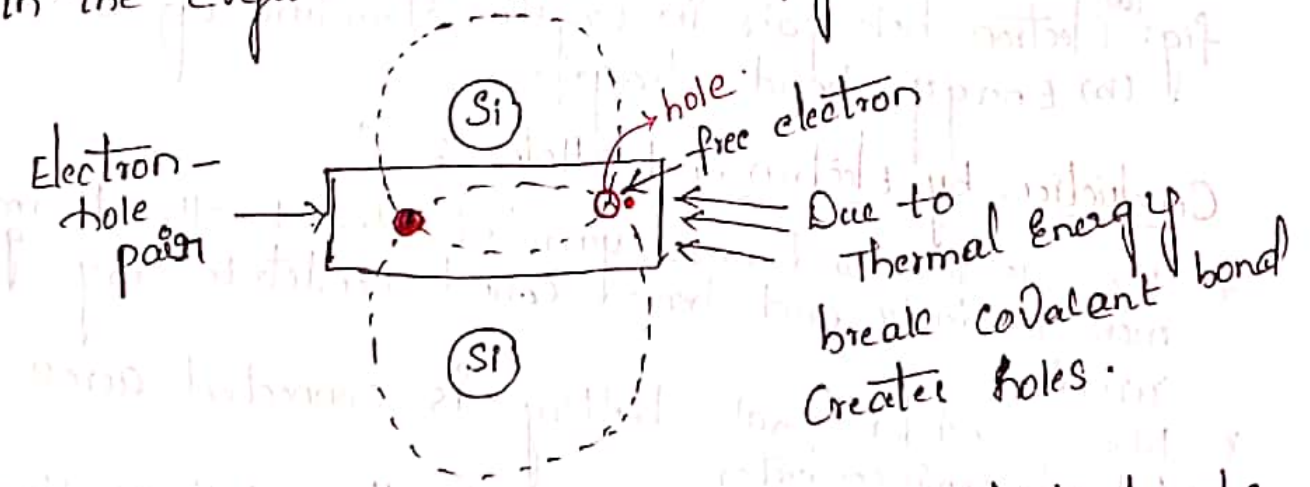
* In figure (b), we observe that both the electrons are shared by the two atoms. Hence the outermost shell of valence electrons of all the atoms is completely filled, and valence electrons are tightly bound to the parent atom. "No-free electrons are available at absolute zero temperature.

* Hence such an Intrinsic Semiconductor behaves as a "perfect insulator" at "zero temperature."

At room temperature, behaviour of Intrinsic Semiconductor :-

* Intrinsic Semiconductors behaves as a perfect insulator at absolute zero temperature.

* At room temperature, Number of valence electrons absorb the thermal energy, due to which they break the covalent bond and drift (moves) to the Conduction band. Such electrons become free to move in the Crystal as shown in fig below.



* Energy required to break the Covalent bonds is 0.72 eV for germanium, 1.1 eV for Silicon } at room temperature

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* Once the electrons are dislodged from the covalent bonds, Then they become free, such free electrons wander in a random fashion in a crystal.
* When a valence electron drift from valence to conduction band breaking a covalent bond, a vacancy is created in the broken covalent bond. such vacancy is called a hole. Whenever electron becomes free, the corresponding holes gets generated.
* So free-electrons and holes (positively charged) get generated in pairs. Such generation of electron-hole pair due to thermal Energy is called "Thermal generation".

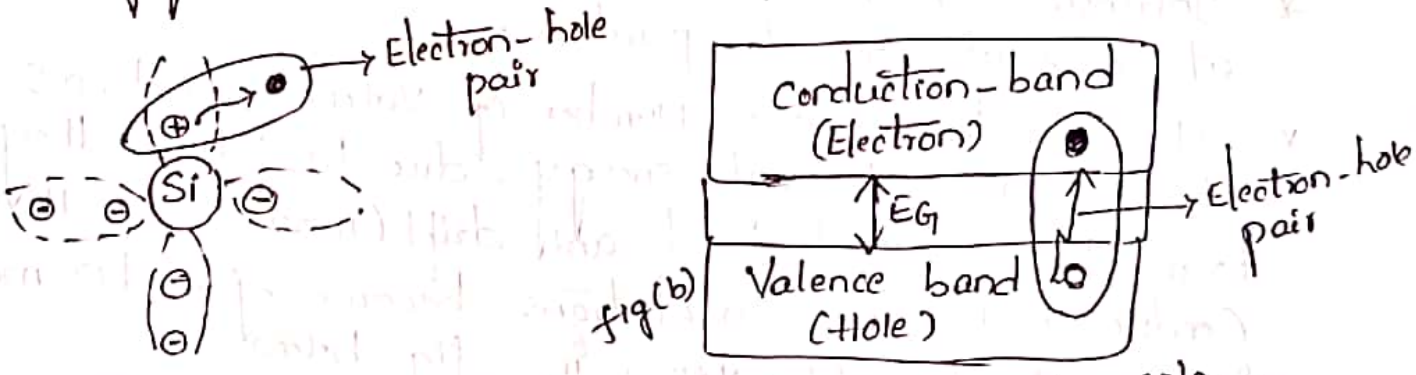

fig: (a) Electron-hole pair in Crystal Structure of Silicon
(b) Energy-band diagram

Conduction by Electron and Holes :-

* The electrons and holes generated due to the thermal generation move randomly and hence cannot constitute any current.
* Now Consider that battery is connected across the Intrinsic Semi-conductor.
* Under the influence of applied voltage (battery) there is electron as well as hole motion in particular direction Causing the "flow of current".

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* The free electrons are moved under the influence of applied voltage. These electrons are negatively charged get repelled from the -ve terminal of battery and attracted towards the +ve terminal. Thus there is an electric current due to the movement of electrons in Conduction band. This is called "Electron current".

* IIly, The holes are moved under the influence of applied voltage. These holes are +vely charged get repelled from the +ve terminal of battery and attracted towards the -ve terminal. Thus there is an electric current due to the movement of holes in Valence band. This is called "Hole current".

* Hole current is, the direction of motion of holes is the opposite direction to that of electrons.

** Note :- * Current due to movement of free electrons in the conduction band is "Electron-current".
* Current due to movement of holes in the Valence band is "Hole current".
* The Electron as well as hole current together Constitutes current in an intrinsic Semiconductor.

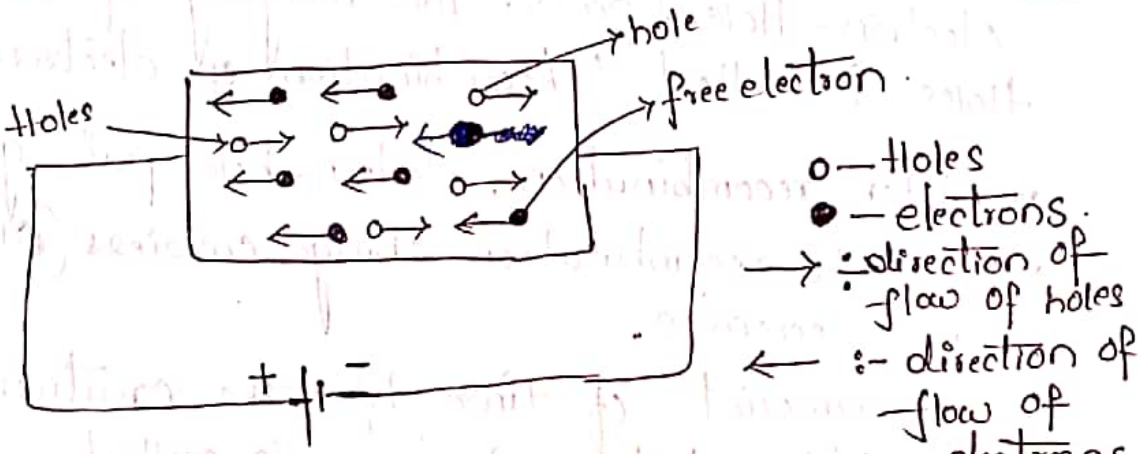

fig: Conduction in Intrinsic Semiconductor.

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Conductivity : The property called Conductivity indicates the ease with which a material can carry the current. Thus more conductivity means that material can carry high current, very easily.

* The conductivity of a good conductor is high while that of an insulator is low.

Note :- In Intrinsic Semiconductor, very few electron-hole pairs get generated at room temperature. Hence very small current can be constituted, due to the application of voltage to an Intrinsic Semiconductor. Thus the conductivity of an Intrinsic Semiconductor at room temperature is very low. Such a low conductivity has very little practical significance. i.e Intrinsic Semiconductor are not used in practice for manufacturing of electronic devices.

* Recombination of electrons and Holes :-

electrons movement in conduction band is always random
Holes movement in valence band is always random
This Thermal agitation continues to produce new Electron-Hole pairs. This merging of electrons and Holes is called "Recombination of electrons & holes".

* After recombination, electron-hole pair gets disappeared
* Due to recombination, charge carriers (electrons & holes) are decreases.
* The amount of time b/w the creation and disappearance of a free electrons or holes is called "Mean life time of the charge carrier".

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Intrinsic concentration :-

At any temperature, at any instant, the free electrons and holes the two types of charge carriers are present in equal number. This concentration is called "Intrinsic Concentration" Mathematically, indicated as,

$$n = p = n_i$$

Where n = Number of free electrons per unit volume

p = Number of holes " " "

n_i = Intrinsic concentration ** (units : number per m^3 (or) number per cm^3)

Derivation of Conductivity of an Intrinsic-Semiconductor :-

For the Semiconductor :-

n = Concentration of free-electrons $/m^3$

p = Concentration of holes $/m^3$

μ_n = Mobility of electrons in $m^2/V\text{-}s$

μ_p = Mobility of holes in $m^2/V\text{-}s$

The current density is given by,

$$J = (n\mu_n + p\mu_p)\, q\, E \ A/m^2$$

Where q = charge on one electron = 1.6×10^{-19} C

E = Electric field in V/m

According to ohm's law $J = \sigma E$

where σ = conductivity in $(\Omega\text{-}m)^{-1}$

Comparing (1) & (2) eqs

$$\sigma E = (n\mu_n + p\mu_p) q \ (\Omega\text{-}m)^{-1}$$

Conductivity is $\sigma = (n\mu_n + p\mu_p) q \ (\Omega\text{-}m)^{-1}$

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for intrinsic semiconductor :

$$\sigma_i = n_i (\mu_n + \mu_p) q \ (\Omega\text{-}m)^{-1}$$

EXTRINSIC SEMICONDUCTORS :-

In order to change the properties of intrinsic Semiconductor a small amount of some other material is added to it.

* The process of adding other material to the crystal of intrinsic semiconductors to improve its conductivity is called "Doping".
* Doped Semiconductor material is called "Extrinsic Semiconductor"
* The Doping increases the Conductivity of the basic intrinsic Semiconductors hence the extrinsic Semiconductors are used in practice for manufacturing of various electronic devices such as diodes, transistors etc.

Extrinsic Semiconductors :

Types of Impurities :-

Depending upon the type of Impurities, the two types of Extrinsic Semiconductors are

1. n-type
2. P-type

Types of Impurities :-

1. Donar Impurity
2. Acceptor Impurity

Donar Impurity :- The Impurity material having 5 Valence electrons is called "pentavalent atom" when it is added to an intrinsic Semiconductor it is called "Donor doping"

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* Each impurity atom donates one free electron to an intrinsic material. Such an impurity is called "Donar impurity"

Ex:- Arsenic, Bismuth, phosphorous etc.

This creates an Extrinsic semiconductor with large number of free electrons, called n-type Semiconductor.

Acceptor Impurity :- another type of Impurity is trivalent atom which has only 3 valence electrons. Such an impurity is called "Acceptor impurity". When this is added to an intrinsic Semiconductor, it creates more holes and ready to accept an electron hence the doping is "acceptor doing".

Ex:- Gallium, Indium, Boron etc.

The resulting extrinsic Semiconductor with large number of holes is called p-type Semiconductor.

N-Type Semi-conductor :-

Definition :- When a small amount of pentavalent impurity is added to a pure semiconductor, it is called as "n-type Semi-conductor."

pentavalent impurity : has 5 valence electrons.

Ex: Arsenic, Bismuth, Antimony, phosphorous

P A A B

* These Impurities are called as "Donar impurity".

formation :- Consider the formation of n-type material by adding Arsenic (As) into Silicon (Si). The arsenic atom has five valence electrons. Silicon atom has 4 Valence electrons. These forms covalent bonds with four adjacent silicon atoms. but 5th electron has no charge to formation a covalent bond.

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This spare electron enters the conduction band as a "free electron". This means that each arsenic atom added into silicon atom gives one free electron. The number of free electrons are controlled by the amount of impurity added to the silicon.

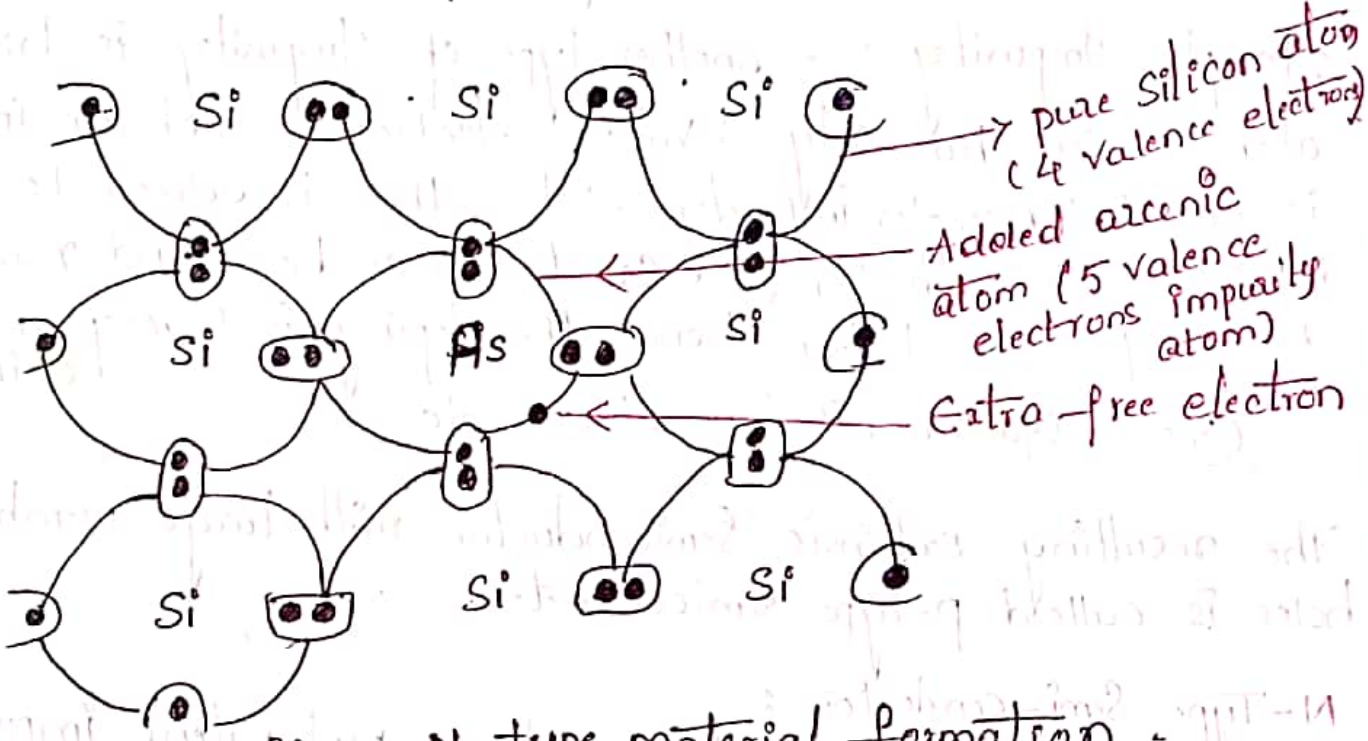

fig:- N-type material formation.

Conduction in N-type Semi-conductor :-

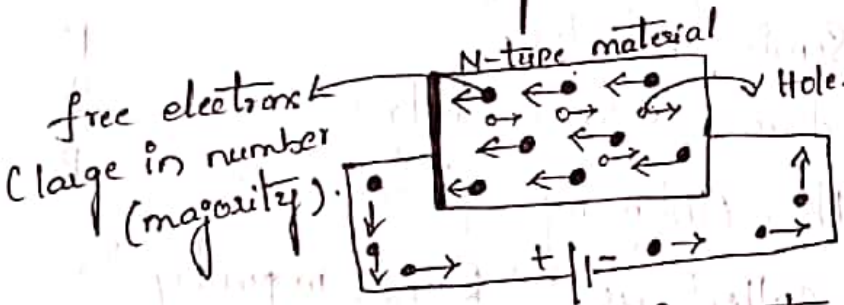

fig: Conduction in n-type material

When the vtg (voltage) is applied to the n-type Semiconductor, the free electrons which are readily available due to added impurity, move in a direction of positive terminal of voltage applied. Holes are less in number hence electrons are dominated here.

Hence In N-type, free electrons are majority Carriers while the holes which are small in number are called "Minority Carriers".

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Conductivity of n-type material :

It is known that in n-type semiconductor material, the free electrons are majority carriers while the holes are minority carriers.

n_n = Concentration of free electrons in n-type
p_n = Concentration of holes in n-type
N_D = Concentration of donor atoms.

Here, n indicates concentration of type of charge carrier electron or hole while the suffix indicates the type of material i.e., n type or p-type.

From basic equation of conductivity,
the conductivity of n-type material can be expressed as,

$$\sigma_n = (n_n \mu_n + p_n \mu_p) e$$

but $p_n << n_n$ as holes are in minority hence,

$$\sigma_n = n_n \mu_n e$$

The number of free electrons is dominantly controlled by donor atoms added than the thermal generation at room temperature.

Hence, concentration of donor atoms N_D added can be approximately assumed to be equal to concentration of free electrons n_n in 'n' type materials.

Thus as $N_D >> n_i$ we can write

$$n_n \simeq N_D$$

$$\sigma_n \approx N_D \mu_n e$$

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2. P-Type Semiconductor :- (BME)

When a small amount of trivalent impurity is added to a pure semiconductor, it is called "p-type Semiconductor".

* Tri-valent impurity has 3-Valence electrons. These elements are Galium (Ga), Boron (B), Indium (In) etc. such an impurity is called "Acceptor Impurity". (BAGI)

P-Type Material formation :-

Consider the formation of p-type material by adding Gallium (Ga) into Silicon (Si). Galium atom has 3 valence electrons Si has 4 Valence electron. So galium atom fits in the silicon Crystal in such a way that its 3 valence electron form covalent bonds with the 3 adjacent atom of silicon Being Shot of one electron, the fourth Covalent bond in the Valence shell is incomplete. The resulting vacancy is called a hole. Such a p-type material formation is represented as follows.

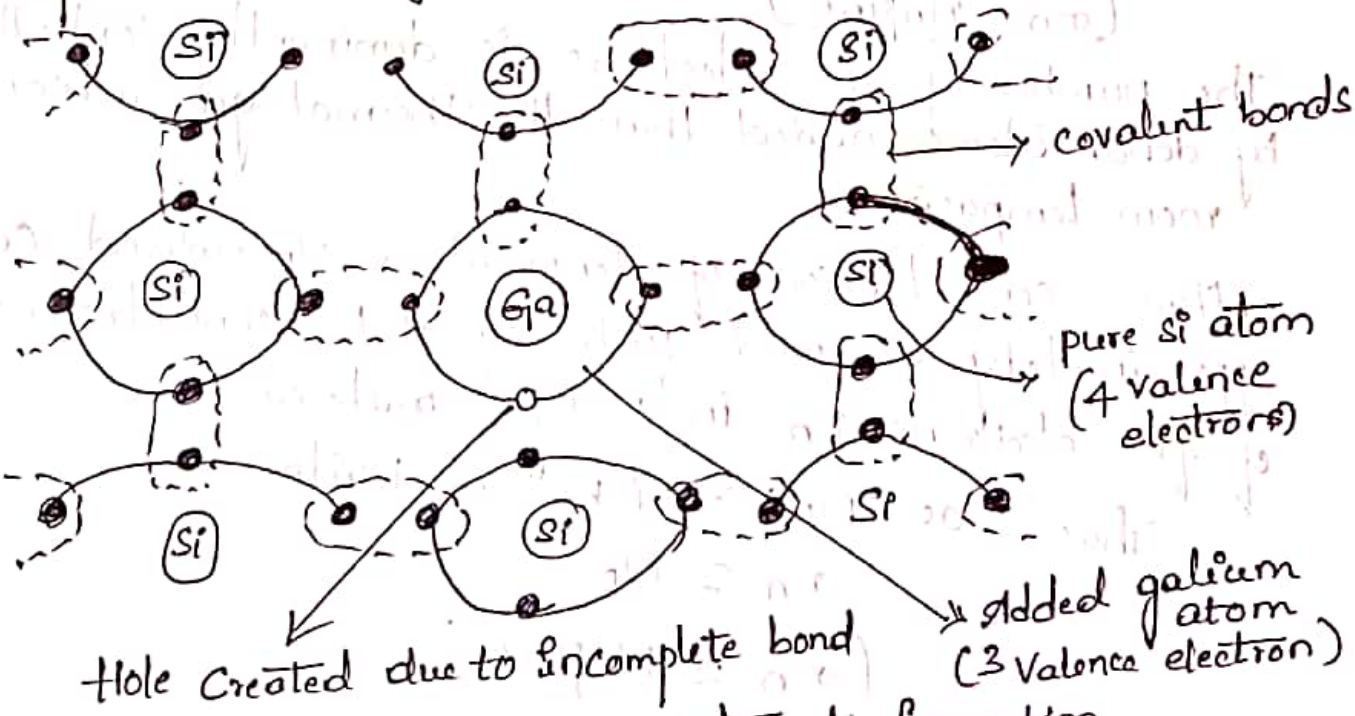

fig: p-Type material formation.

* Note: In this structure galium atom (trivalent impurity) is added to Si-atom (semi-conductor material) it give one hole. This process repeated for more no. of times gives more holes

Hence, p type material has majority number of holes and minority number of electrons.

Conduction in p-type Semi-conductor :-

Now, p-type material is subjected to an electric field by applying a voltage then the holes move in a valence band and are mainly responsible for the conduction. So the current conduction in p-type material is predominantly due to the holes. The free electrons are also present in Conduction band but are very less in number. Hence holes are majority carriers while electrons are minority carriers in p-type material.

The conduction of p-type material is as shown below

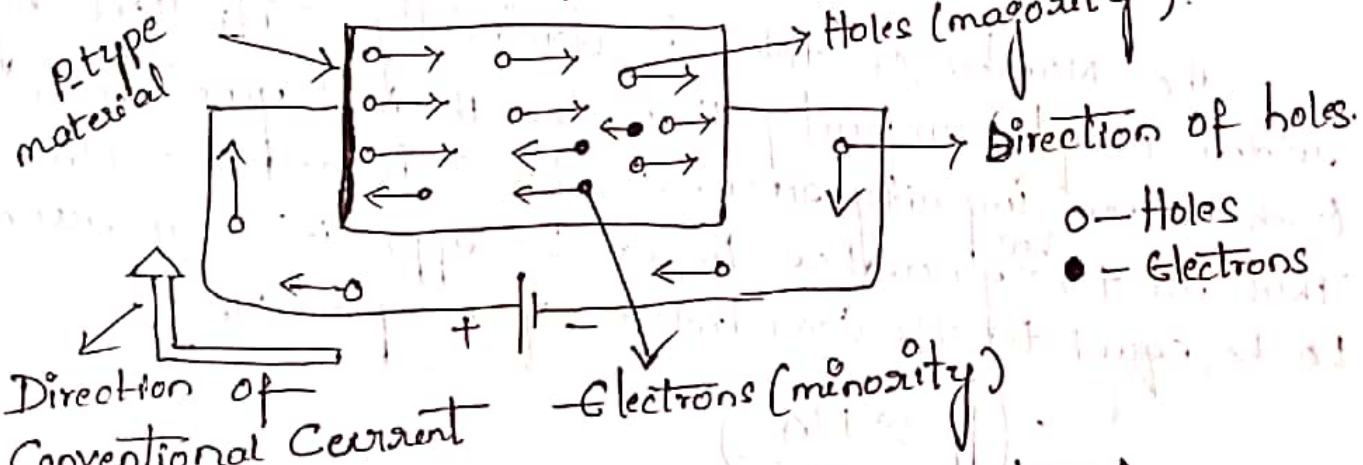

Fig: Conduction in p-type material.

When applying '+' positive terminal to one side of p type material and negative terminal is connected to another side of p-type. holes are positively charged so these are repell to positive terminal move away from positive terminal & towards to negative terminal because of dislike move polarities are attracted to each other. Hence current conduction take place through negative to positive terminal direction.

Conductivity of p-type material :-

For p-type holes are majority carriers, electrons are minority.

n_p = Concentration of free electrons in p-type

p_p = Concentration of Holes in p-type

N_A = Concentration of Acceptor atoms

Thus, the conductivity of p-type material can be Expressed as,

$$\sigma_p = (n_p \mu_n + p_p \mu_p) q \longrightarrow (1)$$

But $n_p << p_p$ as free electrons are in minority here

Hence from (1) $\Rightarrow$ $\sigma_p = (p_p \mu_p q) \longrightarrow (2)$ (n_p - Neglected. so $n_p \mu_n = 0$).

The Number of Holes is dominantly controlled by added acceptor impurity than the Thermal generation. Each added impurity atom creates a hole. hence $N_A >> n_i$.

Thus all the holes generated p_p can be approximately assumed to be equal to the Concentration of acceptor N_A.

$$\therefore p_p \approx N_A$$

$$\therefore \sigma_p = N_A \mu_p q \longrightarrow \text{from (2)}$$

(n_i = intrinsic concentration of the basic semiconductor used.)

Law of Mass-Action for Extrinsic-Semiconductor :—

Mathematically, the law is Expressed as,

St:- The product of electron & hole Concentration is equal to Square of the Intrinsic Carrier Concentration.

$$n \cdot p = n_i^2$$

Where n_i is Intrinsic concentration

Important observations :—

1. The Law can be applied to both intrinsic and extrinsic semiconductors.
2. In case of Extrinsic Semiconductors, n_i is the intrinsic Concentration of the basic semiconductor material used.
3. For n-type material, $n = n_n$ while $p = p_n$

   Hence Law can be stated as ....

$$n_n p_n = n_i^2$$

4. for p-type $n = n_p$ while $p = p_p$ hence law can be stated as $n_p p_p = n_i^2$
5. The law is applicable irrespective of amount of doping.
6. As n_i depends on temparature, the law applicable at a fixed temperature.
7. The law can be used to find both majority and minority Carrier Concentrations in an Extrinsic Semiconductor.

Proof:- Generation of charge Carrier = Recombination of charge Carriers.

$$R = G$$

Generation of charge Carrier's $G = n = p = n_i$

$\therefore$ Recombination of charge Carrier $\propto n \cdot p$

$R \propto n \cdot p$

$G = R = \gamma \cdot n \cdot p \rightarrow (1)$

$G = \gamma \cdot n \cdot p = \gamma \cdot n_i^2 \rightarrow (2)$

$(1) = (2)$

$\gamma \cdot n_i^2 = \gamma \cdot n \cdot p$

$n_i^2 = n \cdot p$

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Carrier Concentration in Extrinsic Semi-Conductors :—

Let us obtain the Concentration of minority and majority carriers in n type and p-type materials using Law of mass action.

N-type material :—

for n-type, $n_n = N_D$

At any fixed temperature, according to "Law of mass action"

$$n_n \times p_n = n_i^2$$

where n_n = majority (electrons) carrier Concentration.

p_n = minority (holes) carrier Concentration.

Using $n_n = N_D$, we can write minority carrier concentration as

$$N_D p_n = n_i^2$$

$$\boxed{p_n = \frac{n_i^2}{N_D}} \quad //$$

P-type material :—

for p-type $p_p = N_A$

According to law of mass action,

$$n_p \times p_p = n_i^2$$

where n_p = (electron) i.e minority carrier Concentration

p_p = (hole) i.e majority carrier Concentration

Using $p_p = N_A$ we can write

$$n_p N_A = n_i^2$$

$$\boxed{n_p = \frac{n_i^2}{N_A}} \quad //$$

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Concept of Depletion region and Barrier potential :

Extrinsic Semiconductors are classified as 2-types those are n-type and p-type. In n-type, the electrons are majority charge Carriers, while holes are minority charge carriers. In p-type, the holes are majority charge carriers and electrons are minority charge carriers. These two types of materials namely p-type and n-type are chemically combined with a special fabrication technique to form a p-n junction. ~~diode~~ Such a Semiconductor p-n junction forms a popular electronic device called "Diode".

The Diode is a basic element of number of electronic Circuits. Thus, the study of behaviour and characteristics of Semiconductor p-n junction is very important in understanding the operation of number of electronic circuits and applications.

* Before Enter into the operation of p-n junction diode, first we need to know some simple basic concepts regarding to the p-n junction operation.

Those are

* formation of Depletion region
* Barrier potential

Formation of Depletion Region :—

{Depletion region also called as "Transition region" and also space charge region}

* Normally, In p-type and n-type materials while we are Combine, junction is form. Concentration gradient Exist near to the junction. There are large number of holes on p-side while very small number of holes on n-side, near the junction. Thus holes starts moving from p side to n-side i.e from high Concentration area towards low Concentration area.

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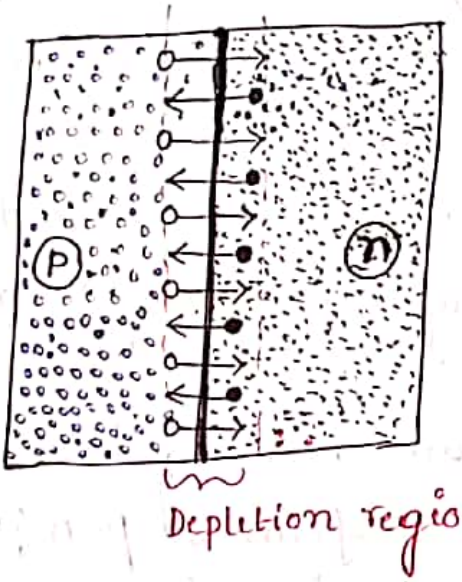
This is nothing but "Diffusion" of holes from p side to n side.



o ⟹ Hole diffusion

⟸ • Electron diffusion

As holes enter the n-region, they find number of donor atoms. The holes recombine with the donor atoms. As donor atoms accept additional holes, they become positively charged immobile ions. This happens immediately when holes cross the junction hence number of positively charged immobile ions get formed near the junction on n-side.

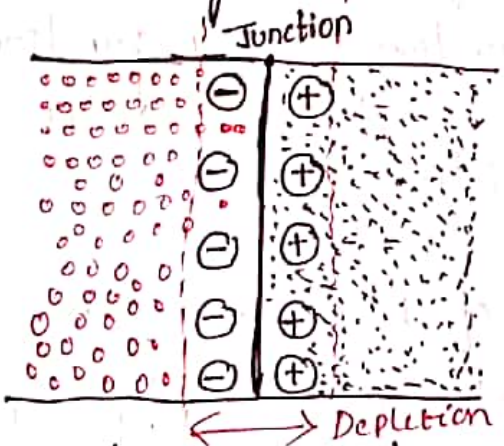


Fig (2): Formation of immobile ions

Atoms on p-side are acceptor atoms. The electrons diffusing from n-side to p side recombine with the acceptor atoms on p-side. As acceptor atoms accept additional electrons, they become negatively charged immobile ions. Such large number of negatively charged immobile ions get formed near the junction on p-side The formation of immobile ions near the junction is shown in above fig (2).

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Thus in thermal Equilibrium, in the region near the junction there Exists a wall of negative immobile charges on p-side and a wall of positive immobile charges on n-side. In this region, there are no mobile charge Carriers. Such a region is depleted of the free mobile charge carriers and hence called "Depletion region" or "Depletion layer".

Note :- The Depletion region gets formed in open Circuited p-n junction very quickly.

* The Depletion region is also called "Space-charge region.
* In Equilibrium Condition, the depletion region gets widened upto a point where no further electrons or holes can Cross the junction. Thus depletion region acts as the "Barrier".

Barrier potential :- (also called as - Junction potential / Built-in-potential)

Near the junction, on one side there are many positive charges and on other side there are many negative charges. According to Coulomb's law, there Exists a force between these opposite charges. And this force produces an Electric field between the charges. The Direction of an Electric field is from positive charge towards negative charge.

The opposite charges existing near the junction Creates a potential difference (voltage) across the junction The Electric field between the charges is responsible to produce potential difference across the junction. This potential difference has a fixed polarity and it acts as a barrier to flow of electrons and holes, across the junction. Hence this potential is called Barrier potential, junction potential or built-in potential barrier of a p-n junction.

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* Barrier potential is Expressed in volts. Its value is called "Height of the barrier of a p-n denoted as V_j (or) V_{bi}

* Barrier potential also indicates the amount of voltage with proper polarity, to be applied across the p-n junction, to restart the flow of electrons and holes across the junction.

* The Barrier potential is expressed in volts, it is approximately 0.7V for Silicon and 0.3V for germanium, at 25 °C.

* Barrier potential of p-n junction mainly depends on the following factors:

1. The Type of Semiconductor used.
2. The Concentration of donor impurity on n-side
3. The Concentration of Acceptor impurity on p-side
4. The intrinsic Concentration of basic semiconductor
5. The Temparature.

The Expression for the Barrier potential / is junction potential

$$V_j = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Where V_T = voltage equivalent of temperature

N_D = Doping Concentration of n-side / amount of doping of n-side.

N_A = Doping Concentration of p-side / amount of doping of p-side.

Note: V_j (junction potential / Barrier potential) is depends on V_T.

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CONCEPT OF DRIFT CURRENT AND DIFFUSION CURRENT

DRIFT CURRENT :—

* When a voltage is applied to a Semiconductor, the free electrons try to move in a straight line towards the positive terminal of the battery.
* The electrons moving towards positive terminal Colloide with the atoms of semiconductor and Connecting wires along its way.
* Each time electron strikes an atom, it rebounds in a random direction.
* But still the applied voltage make the electrons drift towards the positive terminal. This drift Causes Current produced due to drifting of free electrons is called "Drift Current", and the velocity with which electrons drift is called "Drift Velocity".

Definition :— Drift current means, the flow of current due to Bouncing of electrons from one atom to another, travelling from negative terminal to positive terminal of the applied voltage.

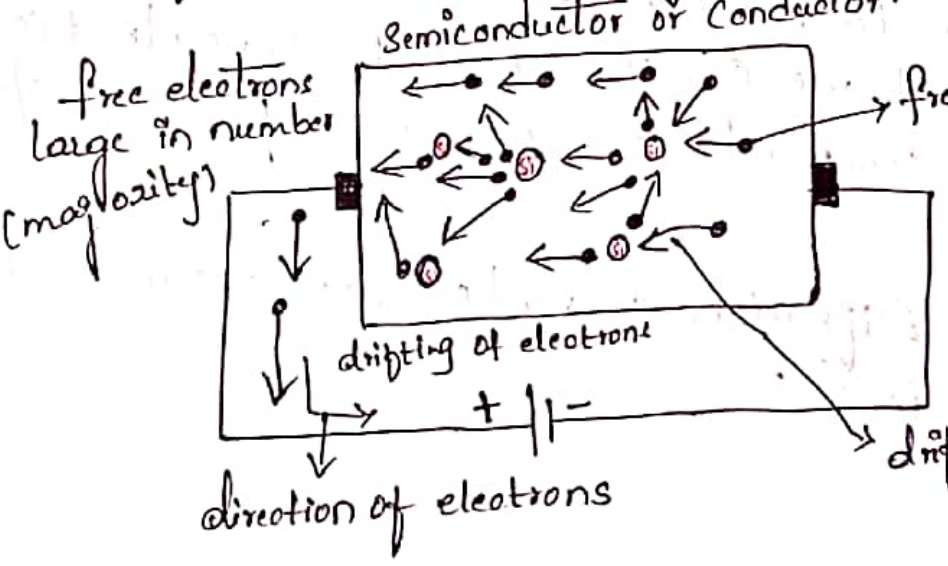

fig :- Drift mechanism Causing Drift current.

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DIFFUSION CURRENT :-

* Due to drifting of free electrons under the externally applied voltage, produces Drift-current.
* In addition to drift current, there may exist an additional current due to the transport of charges in a Semiconductor. Such an additional current is due to the phenomenon called "Diffusion".
* The current due to diffusion is called "Diffusion current" Basically it is due to "Non-uniform Concentration of charged particles" in a Semiconductor
* Let us know what is Diffusion and Nom-uniform Concentration of charged particles".

Consider a p-type Semiconductor bar which is Non-uniformly doped as shown in fig. Due to non-uniform doping the holes are large in number on one side while less in number on other side. Due to this there is High Carrier Concentration area with one side and lower Carrier Concentration area on another side. This Creates "Concentration Gradient". In one side more no. of holes and another side lesser number holes due to applied voltage, the holes in higher side are move from higher Concentration area to lower Concentration area. Such a movement of charge carriers, due to concentration gradient in a Semiconductor is called process of "Diffusion".

Both Drift & Diffusion currents are occur in the Semiconductor devices.

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Non-uniform doped semiconductor p-type bar.

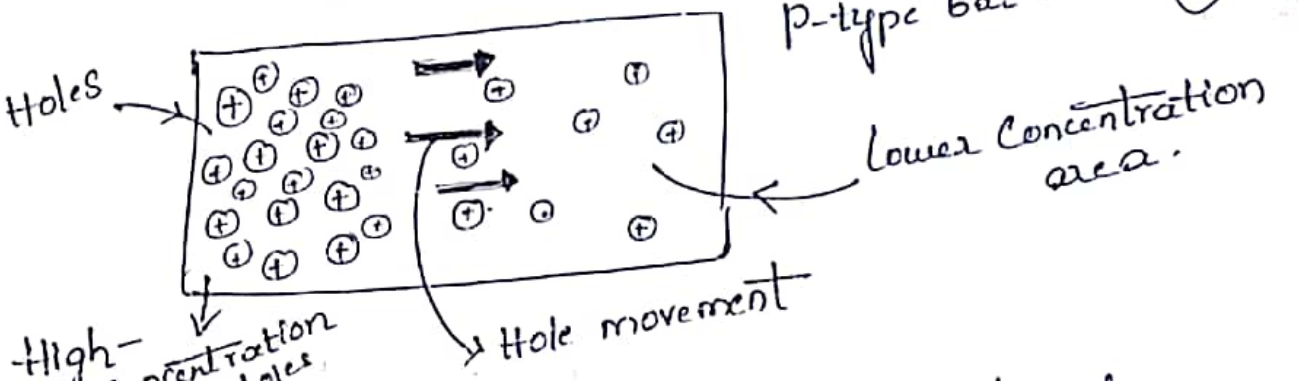
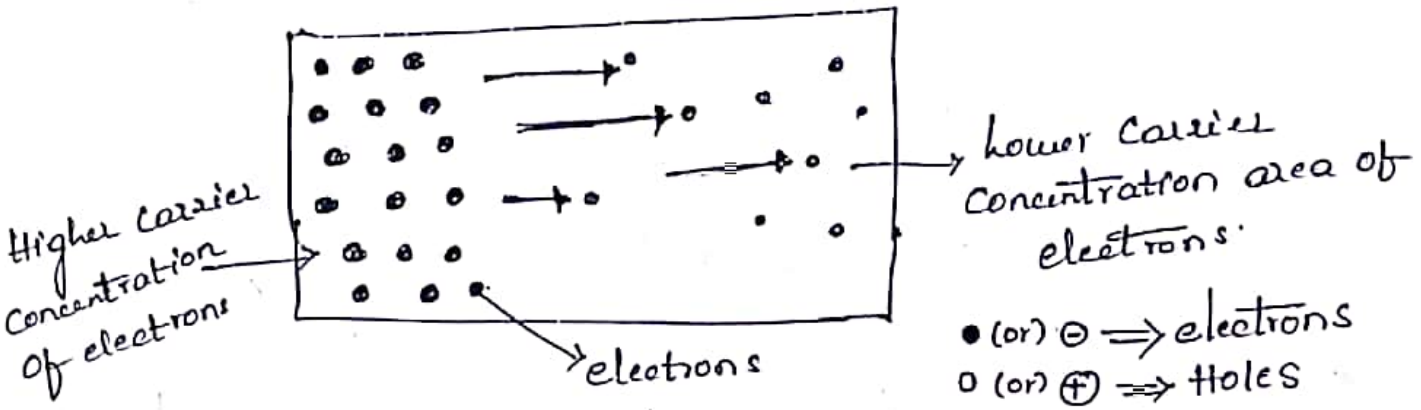


fig :- Diffusion in p-type material



● (or) ⊖ ⇒ electrons
○ (or) ⊕ ⇒ Holes

fig :- process of Diffusion in n-type material.

* process of Diffusion is due to movement of charge carriers.

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P-N Junction Diode :-

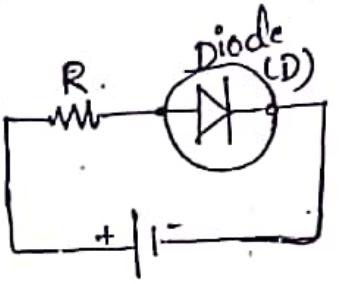
Introduction :-

"William Henry Eccles" was the first founder of Diod in 1919. It was derived from Greek roots as Di- means two "ode" - means Electrodes Combinedly called as Diode.

* Two types of Extrinsic Semiconductors n-type & p-type are chemically combined with a Special fabrication technique to form a p-n junction. Such a Semi-Conductor p-n junction forms popular Electronic device called "p-n junction diod
* p-n junction has two terminals called Electrodes one each from p & n regions.

anode cathode

Symbol of p-n junction Diode :-



(a) Anode ——▷|—— Cathode.

(b) Anode (Electrode 1) — P | N — Cathode (Electrode-2).

Ohmic contacts.

fig (a), (b) : Symbol and Schematic of p-n junction.

Construction :-

p-n junctions forms by Combining of p-type & n-type Semiconductors. It has two terminals called electrode i-e anode and cathode one each from p-region and n-region. To Connect n and p regions to the External terminals, a metal is applied to the heavily doped n and p-type Semiconductor regions. Such a Contact between

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a metal and a heavily/lightly doped semiconductor is called "Ohmic contact".

(18)

* In p-type majority carriers are Holes, minority carriers are electrons, n-type majority carriers are Electrons, minority carrier are Holes.
* When we are combining p and n type semiconductors it forms a junction.
* The p-n junction diode is as shown below:

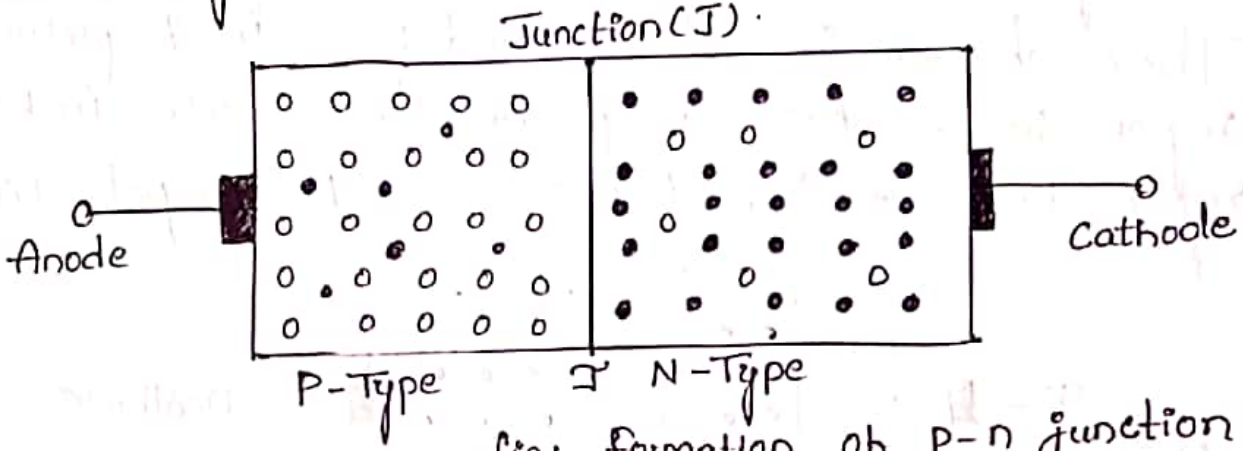

fig: formation of p-n junction

Working:

The electrons are majority charge carriers in n type these are attracted towards holes of p-side near the junction. These electrons are cross over the junction and recombine with holes it sees to be free carriers. This process of recombination of electrons with holes and similarly from p-side holes are attracted to electrons in n-side. This process of recombination of Electrons & holes is called "Diffusion". This recombination Exist only at nearer to the junction only, free electrons & holes get depleted near the junction.

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* Depletion region contains only negative ions on p-side positive ions on n-side of junction. These ions are "Immobile ions".

* Motion of electrons from n-side to p-side doesn't stop immediately, after the formation of Depletion region. But it cross the junction these electrons are repples -lo negative ions in Depletion region then it stops moment of electrons.

* These charged ions (electrons and holes) in Depletion region develope an Electric field in Depletion region known as "Junction potential / Barrier potential".

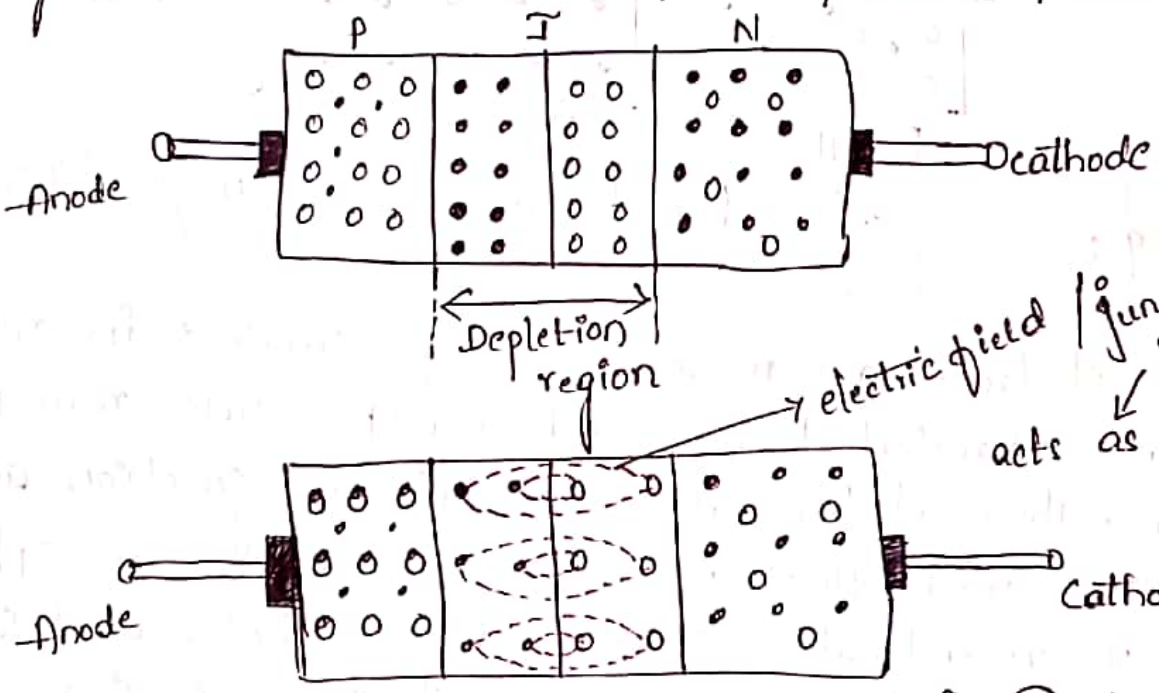

fig: formation of Barrier potential in Depletion region.

* Junction potential acts as "Barrier also called as "Barrier potential it restricts the flow of electrons and holes

Junction / Barrier potential for Si - 0.7V and,
for Ge - 0.3V

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Biasing of p-n junction Diode :-

Biasing : The process of applying External voltage to Electronic devices to establish Suitable working Conditions called "Biasing"

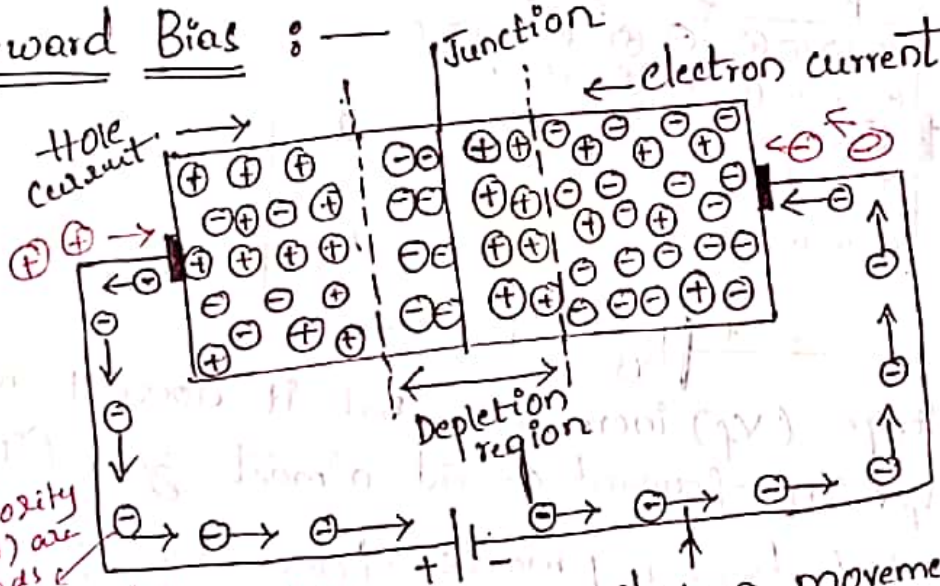
Types of Biasing :-

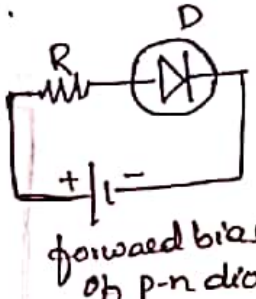
There are 2 types of Biasing those are

- ∝ forward Biac
- ∝ Reverse Bias

* p-n junction diode operated in these 2 two biasing Conditions.

Forward Bias :-





forward bias of p-n diode. where 'R' is forward resistance used to limit the amount of current

* When positive terminal of the battery is Connected to the p type and negative terminal to the N-type of the p-N junction diode, the bias applied is known as forward bias.

As shown in figure, the applied potential with External battery acts in opposition to the internal barrier potential and disturbs the equilibrium.

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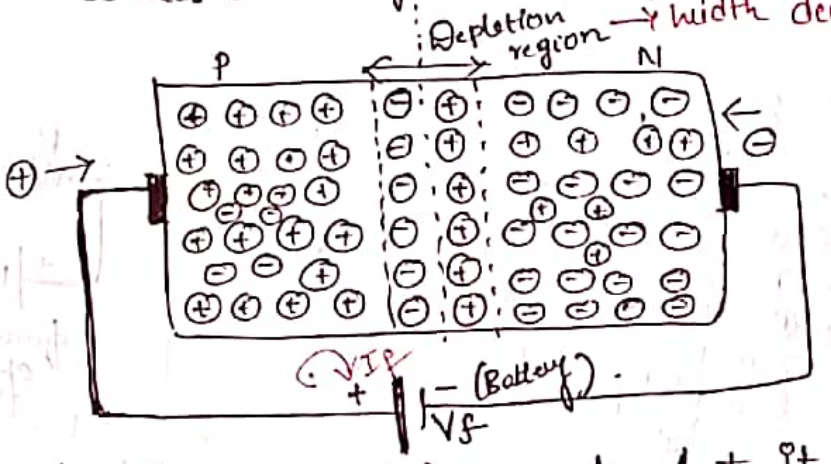
As soon as Equilibrium is disturbed by the application of an external voltage. Under the forward bias condition. The applied positive potential repels the holes in p-type region. so that holes moves towards the junction and applied negative potential repels the electrons in the n type region and the electrons moves towards the junction. Eventually when the applied bar. potential is more than the internal barrier, then in depletion region overcomes the problems of opposition of potential of electron from the junction and these electrons and holes are cross the junction and depletion layer. So depletion region in forward bias is reduces.



* forward voltage (V_f) increased, but it does not more than V_γ i.e $V_f < V_\gamma$ the forward current almost zero ($I_f = 0$). because potential barrier prevents holes from p-region and electrons from N-region to flow across the depletion region in the opposite direction.

* If forward voltage is more than V_γ (cut-in-voltage) $V_f > V_\gamma$ then the barrier potentials allows the electrons from n region to p region and holes cross junction from p region to n region.

Due to this, Depletion region decreases in forward bias Condition.

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Forward V-I characteristics of Diode :-

* The response of p-n junction can be easily indicated with the help of characteristics called V-I characteristics of pn junction diode.
* It is the graph of vtg applied across the p-n junction diode (V_f) and current flowing through the p-n junction (I_f).

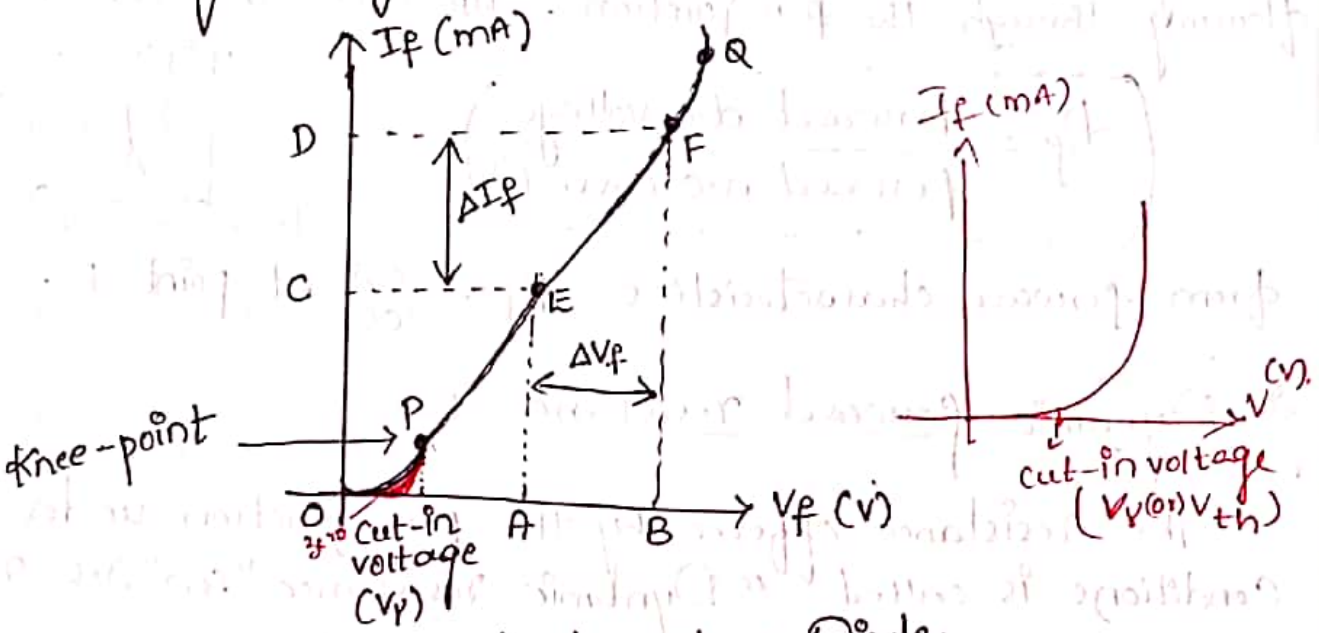

Fig : Forward characteristics of a Diode.

Basically forward characteristics can be divided into 2 regions

1. Region O to P :- If V_f is less than V_γ (cut-in-voltage) the current flowing is very small. practically this current is assumed to be zero.

2. Region P to Q and onwards :-

If V_f increases towards V_γ the width of depletion region goes on reducing, when V_f exceeds V_γ i.e $V_f > V_\gamma$ the depletion region becomes very thin and current I_f increases suddenly. This increase in the current is exponential as shown above figure.

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Diode Resistance under forward bias :-

Forward Resistance of Diode :-
Resistance offered by the p-n junction diode in forward bias condition is forward resistance.

1. Static forward resistance :-

Forward resistance is denoted as R_f and this can be calculated on a particular point on the forward characteristics.

Thus at a point E shown in the forward characteristics, the static resistance R_f is defined as the ratio of the d.c voltage applied across the p-n junction to the d.c current flowing through the p-n junction. It is also called as "d.c Resistance"

$$R_f = \frac{\text{forward d.c voltage}(V)}{\text{forward d.c current}(I)}$$

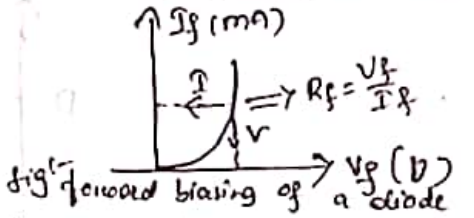


fig: forward biasing of a diode

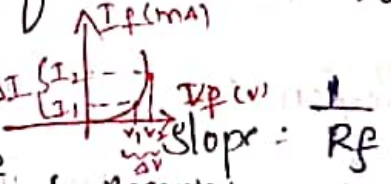
from forward characteristics $R_f = \frac{OA}{OC}$ at point E.

2. A.C / Dynamic forward resistance :-

The resistance offered by the p-n junction under a.c conditions is called "Dynamic resistance" (or) "A.C resistance".

"Dynamic resistance" is reciprocal of the slope of the forward characteristic.

It is also defined as ratio of change in applied voltage from point A to B shown in fig which is ΔV_f and their corresponding change in forward current from C to D i.e ΔI_f.

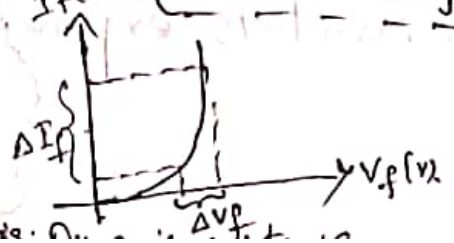


Thus slope of characteristics is $\Delta I_f / \Delta V_f$ where η = constant.

Slope $= \frac{1}{R_f} = \frac{1}{\Delta V_f / \Delta I_f}$

slope $= \frac{\Delta I_f}{\Delta V_f}$.

$$\therefore \left(r_f = \frac{\Delta V_f}{\Delta I_f} \right) \Rightarrow \left(r_f = \frac{1}{(\Delta I_f / \Delta V_f)} = \frac{\eta V_T}{I} \right)$$



$$\left(r_f = \frac{1}{\text{(slope of forward characteristics)}} \right)$$

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2. Reverse biasing of p-n junction diode :—

Definition :

If an External d.c voltage is Connected in such a way that the p-region terminal of a p-n junction is Connected to the negative of the battery and the n-region terminal of a p-n junction diode is Connected to the positive terminal of the battery, this biasing Condition is called "Reverse biasing" of p-n junction.

The below figure shows the Connection of p-n junction in reverse biar Condition.

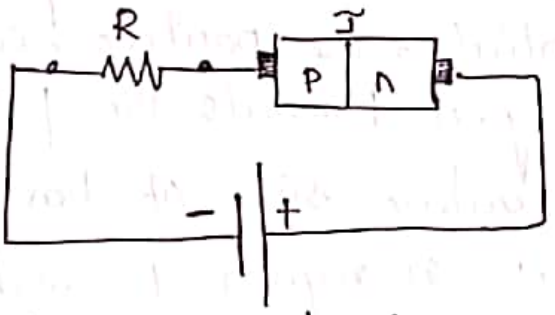

fig: Reverse biasing

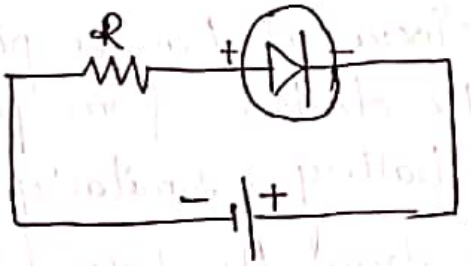

fig: Symbol representation

Operation :—

* When the p-n junction is reverse biased the negative termin attracts the holes in the p-region, away from the junction.
* The positive terminal attracts the free electrons in the n-region away from the junction.
* No charge carrier is able to cross the junction.
* As electrons and holes both moves away from the junction, so depletion region widens. This Creates more positive ions and hence more negative ions in n region. This is because of applied potential helps the Barrier potential as shown in below fig.

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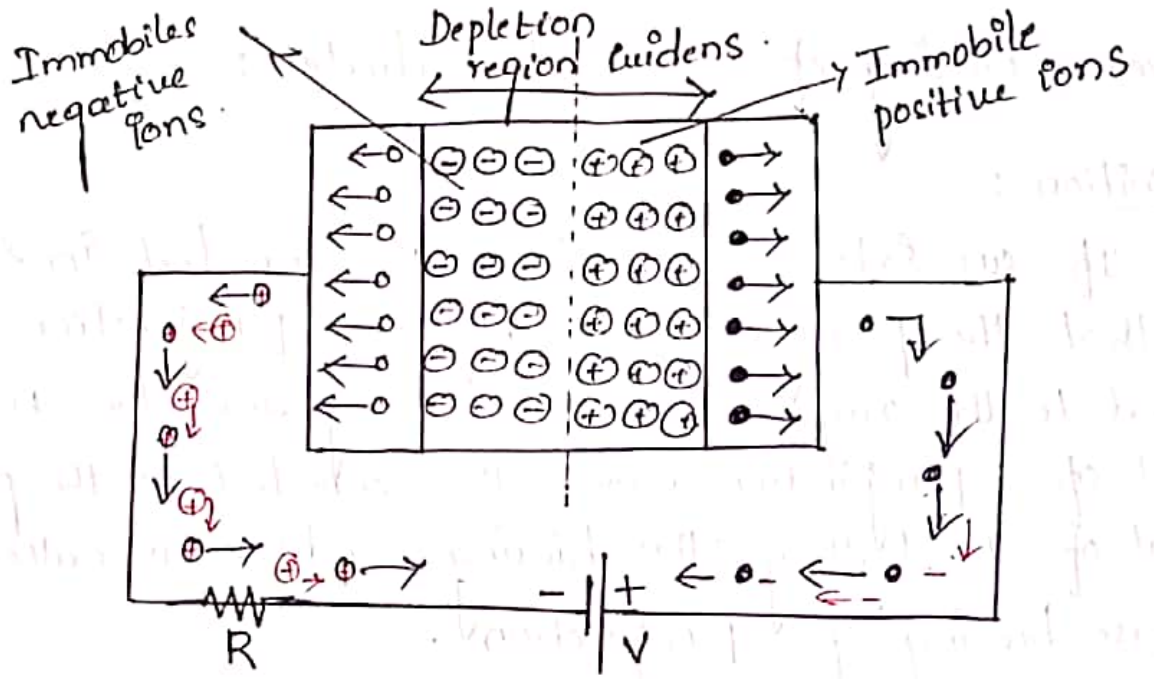

* Depletion region widens, barrier potential across the junction also increases, so the majority carrier (holes) from p to n electrons from n to p movement is stops.
* Due to increased Barrier potential, the positive side drags the electrons from p-region towards the positive of the battery. similarly negative side of barrier potential drags the holes from n-region towards the negative of battery.
* The electrons on p-side and holes from (on) n-region towards 't' are minority charge carriers, which constitutes the current in Reverse biased Condition. This current is called "Reverse Saturation Current" which is very small of the order of few microamperes for Ge, few nanoamperes for Si p-n junction diodes.

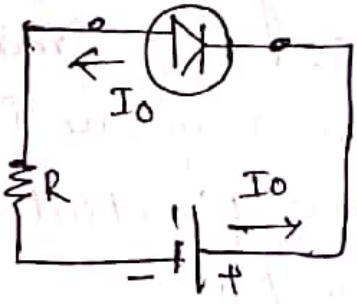

fig: Direction of reverse current.

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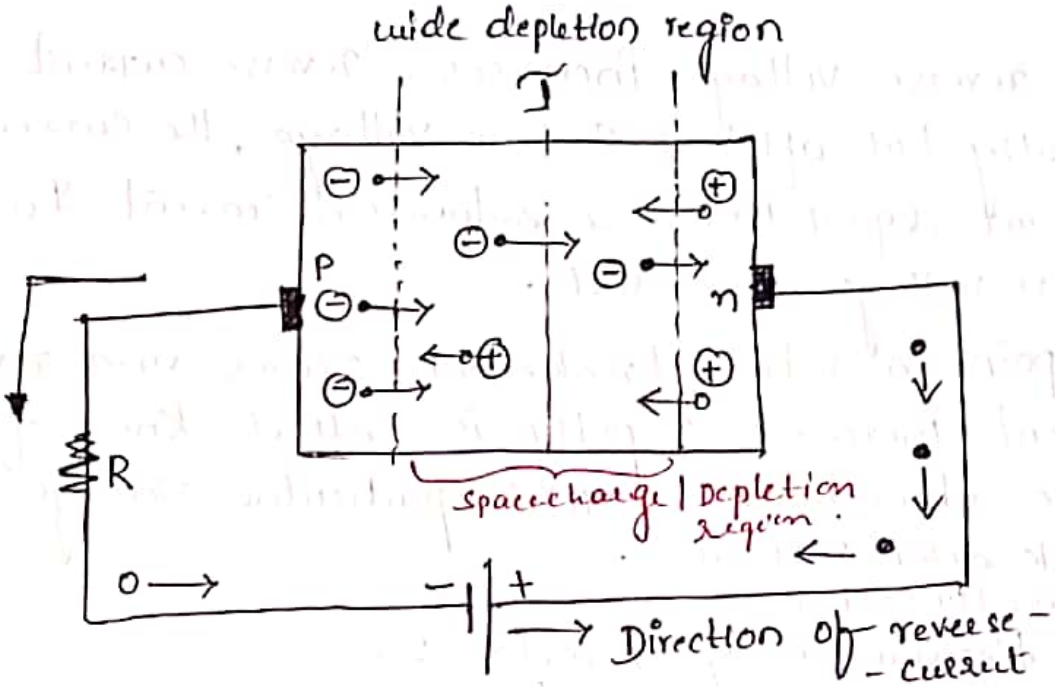


fig: flow of minority charge carriers in Reverse bias.

Reverse characteristics of p-n junction Diode :-

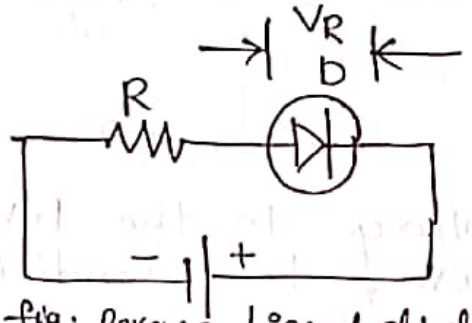
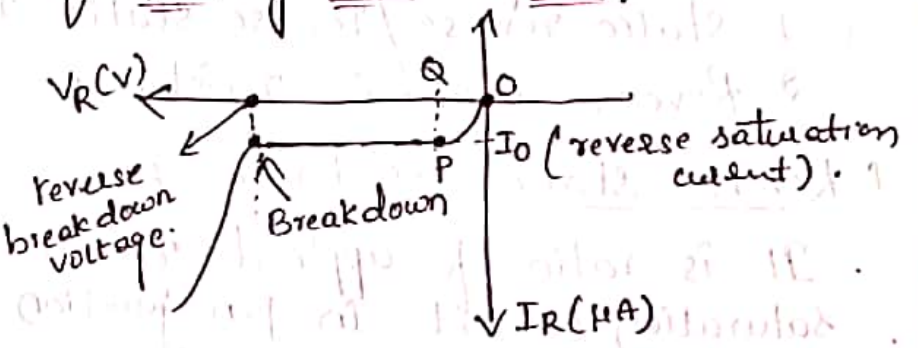


fig: Reverse biased diode.



The reverse voltage across the diode is V_R while the current flowing is reverse current. I_R flowing due to minority charge carriers. The graph of I_R Vs V_R is shown above.

* Reverse voltage is taken as negative because of applied polarity of reverse voltage is opposite to that of forward voltage.
* Reverse saturation current is also taken as "negative".

This can be plotted in third Quadrant

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* As reverse voltage increases, reverse current increases initially but after a certain voltage, the current remains constant equal to reverse saturation current I_o though reverse voltage increased.

* The point A where breakdown occurs and reverse current increases rapidly is called knee of the reverse characteristics. That particular voltage is called "Break-down voltage".

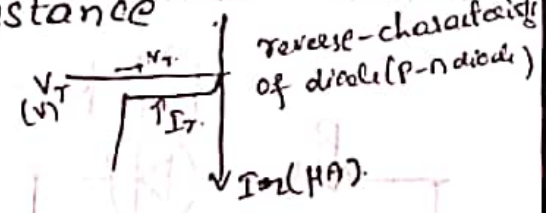
Diode Resistance (under R.B):—

Reverse Resistances of Diode :—

P-n junction offers large resistance in the reverse biased condition called "Reverse resistance".

These are 2 types.

1. Static reverse / Reverse static resistance
2. Reverse dynamic resistance.



1. Reverse static/dc resistance :—

It is ratio of applied reverse voltage to the reverse saturation current in p-n junction reverse bias condition. denoted by R_r

$$R_r = \frac{\text{Applied reverse voltage}}{\text{Reverse saturation current}} = \frac{OQ = V_o}{I_o}$$

2. Reverse Dynamic resistance :—

It is ratio of change in reverse voltage to change in reverse current.

$$r_r = \frac{\Delta V_R}{\Delta I_R} = \frac{\text{change in reverse voltage}}{\text{change in reverse current}}$$

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Complete V-I characteristics of a Diode :—

V-I characteristics is the plot between voltage and current.

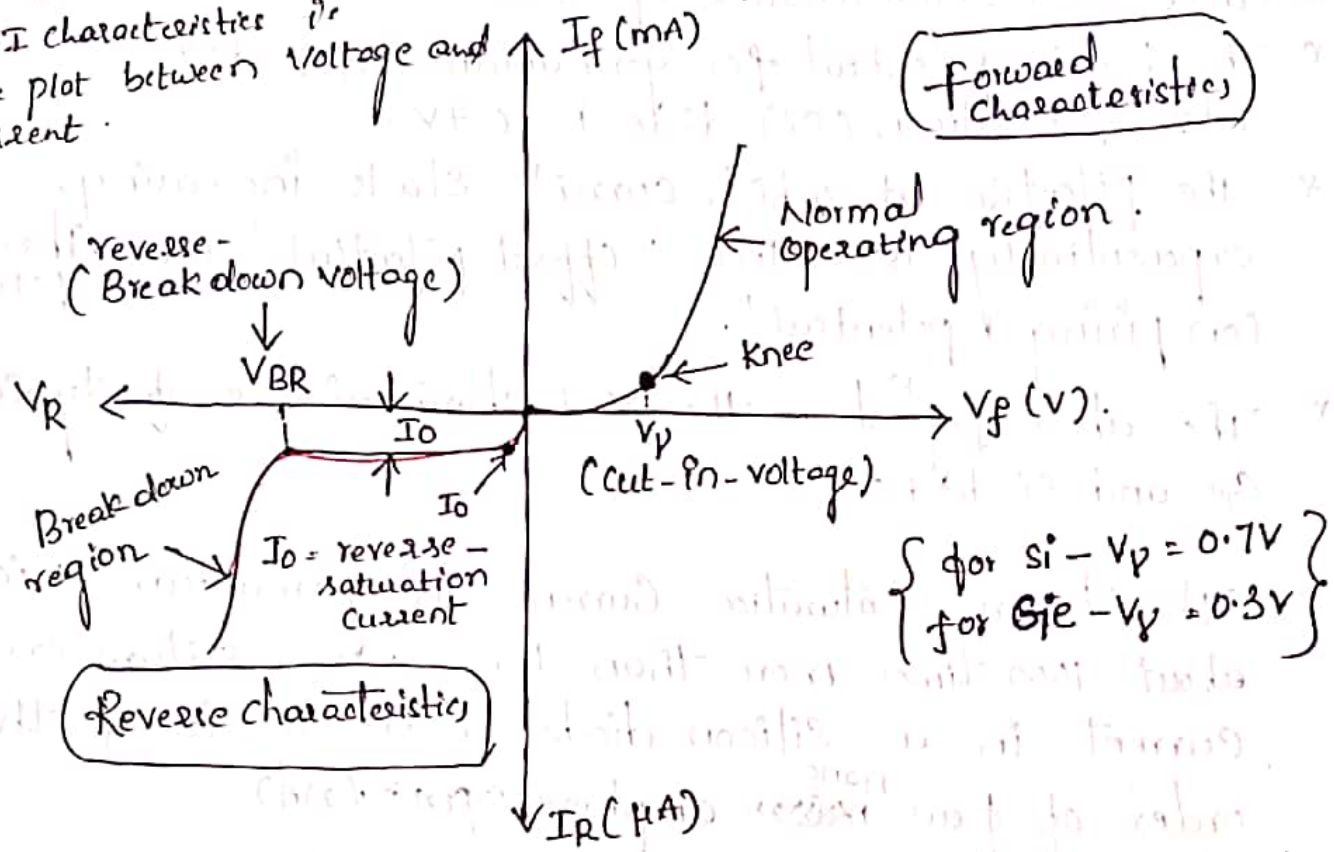

fig: V-I characteristics of a p-n junction diode.

i.e

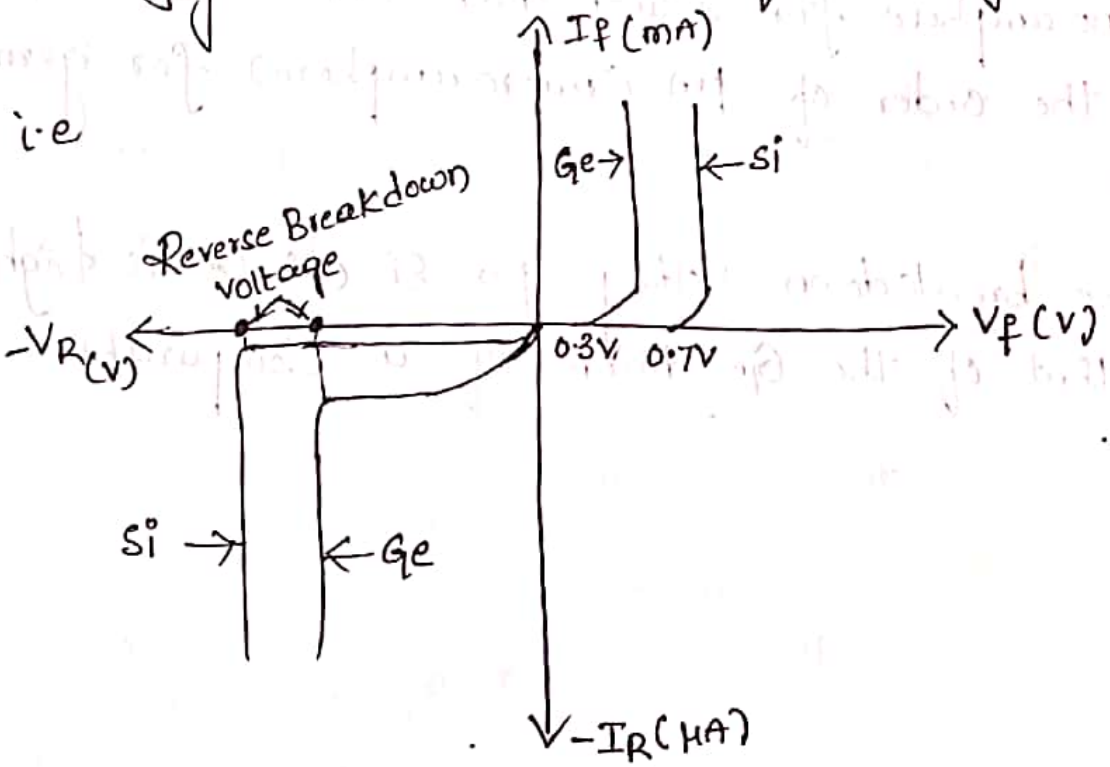

fig: V-I characteristics of typical Ge and Si diodes.

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* The Combined forword and reverce characteristics is called V-I characteristics of Diode.
* The Barrier potential for germanium (Ge) diode is 0.3V while for silicon (Si) diode is 0.7V.
* The potential at which current starts increasing exponentially is called "offset potential" (or) Threshold-potential (or) firing potential".
* The above fig (b) shows the V-I characteristics of typical Ge and Si diodes.
* The Reverse Saturation Current in germanium diode is about 1000 times more than the reverse Saturation current in a Silicon diode while it is of the order of few nano amphere (nA)
* The reverse saturation Current Io is of the order of nano amphere for silicon diode (nA) while it is of the order of μA (micro amphere) for germanium diode.
* Reverse breakdown voltage for Si diode is higher than that of the Ge diode of a Comparable rating.

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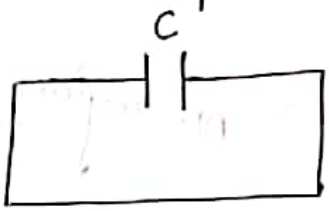
Diode Capacitance :—

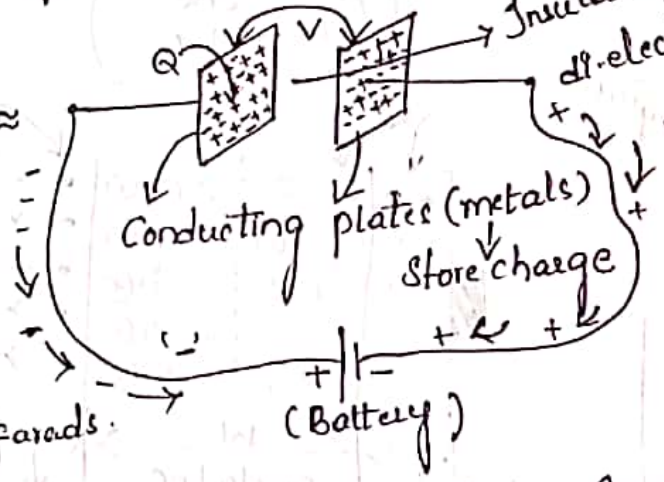
* In PN Junction, the Depletion layer will be working as a parallel plate Capacitor.
* The width of the depletion layer changes during biasing Therefore there are two types of Capacitance.
* Those are,

1. Transition Capacitance (C_T) : during reverse bias
2. Diffusion Capacitance (C_D) : during forward bias

What is Capacitance :—

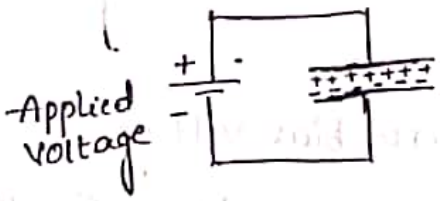
A Capacitor is a passive device component that stores an "Electric charge". The property of storing electric charge of capacitor is "Capacitance". Usually these having two parallel plates conducting these are seperated by "Di-electric".





$$C = \frac{Q\ (\text{Coulombs})}{V\ (\text{volts})} = \text{farads}$$

Capacitance is ratio of charge stored Q on Capacitor to the voltage across the Capacitor.



When the Capacitor is connected to a Circuit with supply voltage source, two processes, which are called charging & discharging the Capacitor will happens in Circuit specific Condition.

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1. Transition Capacitance :-

* In Reverse bias condition, the majority charge carriers (electrons) in n-region and holes in p-region move away from the junction. This increases the "width of the Depletion region".
* As the charged particles move away from the junction there exists a xcharge with respect to the applied voltage.
change in
* The change in charge 'dQ' with respect to the change in voltage 'dv' is nothing but "Capacitive Effect". Such Capacitance is called "Transition Capacitance". (or) "Space-charge Capacitance" (or) "Barrier Capacitance" (or) "Depletion layer Capacitance".
* It is Denoted by "C_T" it is given by

$$C_T = \frac{dQ}{dV}$$

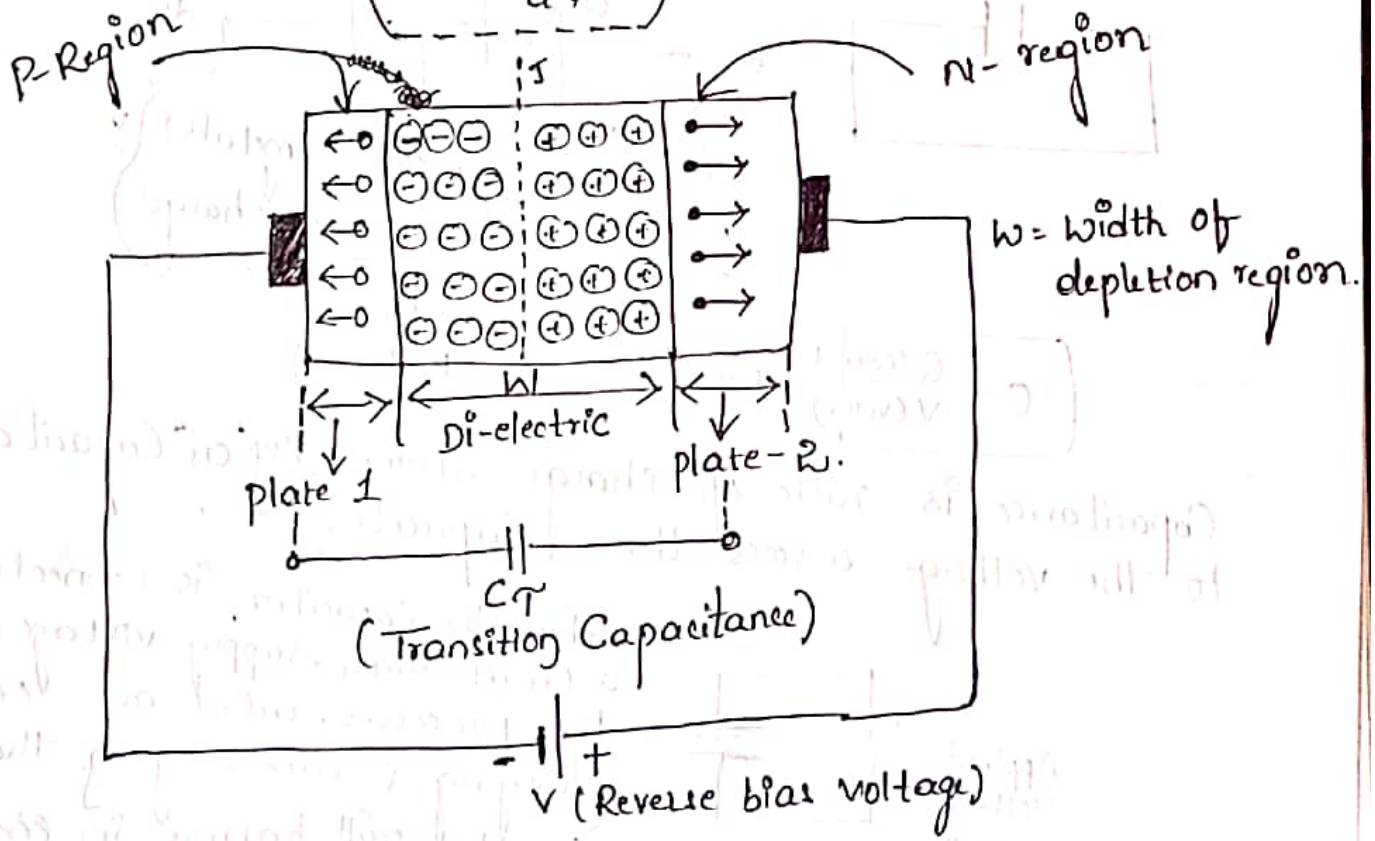

Fig: Transition Capacitance in reverse bias Condition

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This Capacitance is very important as it is not constant but depends on the magnitude of the reverse voltage. If 'W' is the width of the depletion region then the Transition Capacitance is given by,

$$C_T = \frac{\varepsilon A}{W}$$

permitivity means ability of a substance to store electrical energy in an "Electric field".

Where,

A = Area of Cross section of the junction.
ε = permitivity of the Semiconductor.
W = width of Depletion region.

As the reverse biased applied to the diode increases, the width of the depletion region (W) increases. Thus the transition Capacitance C_T decreases. In short, the Capacitance can be Controlled by the applied voltage. The Variation of C_T with respect to the applied reverse bias voltage is shown in below.

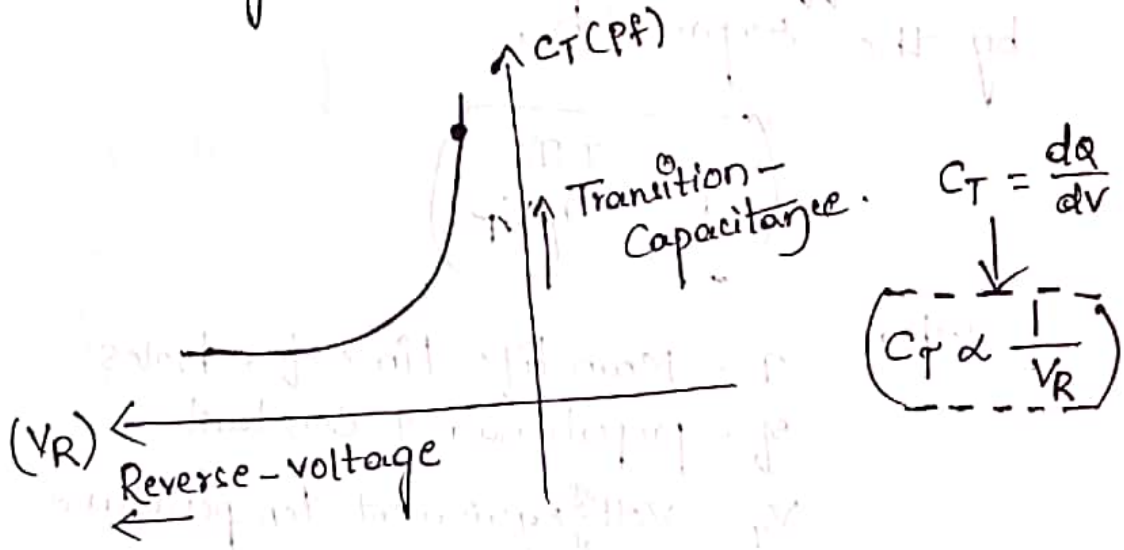

fig: C_T against the Reverse voltage

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2. Diffusion Capacitance :—

⇒ During forward biased Condition, an another Capacitance comes into Existence called "Diffusion-Capacitance" (or) "storage Capacitance" denoted as "C_D".

* In forward biased condition, the width of the depletion region decreases and holes from p side get diffused in n-side while electrons from n-side move into p-side.
* As the Applied voltage increases, Concentration of injected charged particles increases.
* This rate of change of the injected charge with applied voltage is defined as a "Capacitance" called "Diffusion Capacitance".

$$C_D = \frac{dQ\ (C)}{dV\ (V)}$$

The Diffusion Capacitance can be determined by the Expression.,

$$C_D = \frac{\tau I}{\eta V_T}$$

Where τ = Mean life time for holes
η = proportionality constant
V_T = Voltage equivalent temperature at
I = forward Current.

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So, diffusion Capacitance is proportional to the current for forward bias condition the value of diffusion Capacitance is of the order of nano farads to micro farads while transition Capacitance is of the order of pico farads. So C_D much larger than C_T.

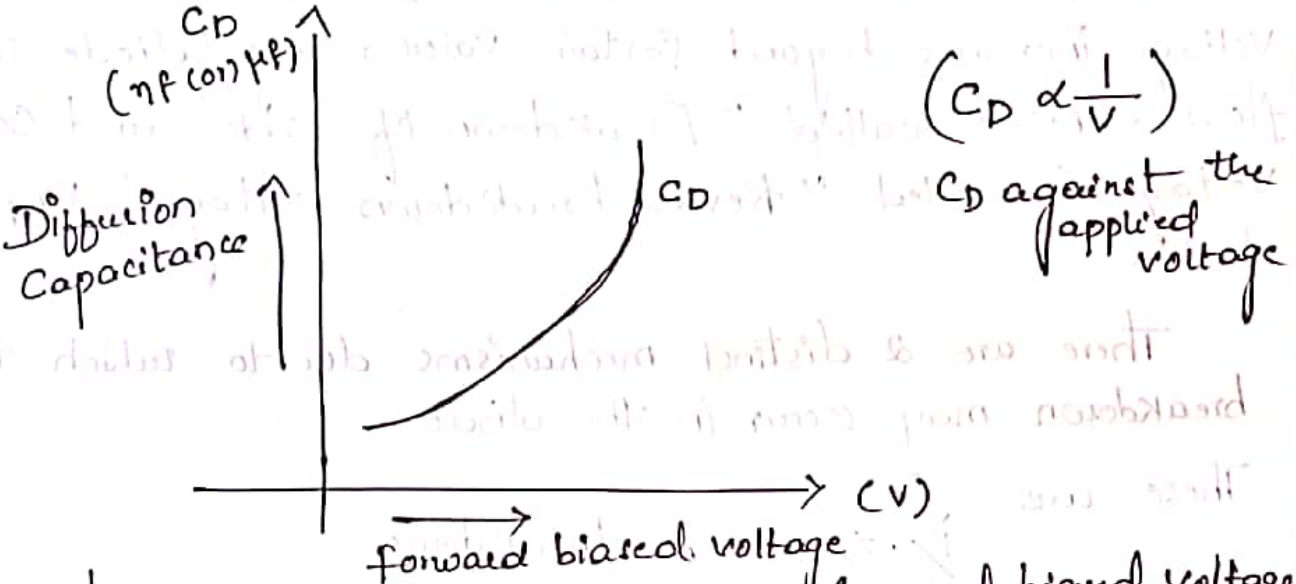

fig: diffusion Capacitance versus applied forward biased voltage

However, In forward biased condition, C_D appears in parallel with the forward resistance which is very very small. Hence the time constant which is function of product of the forward resistance and C_D is also very small for ordinary signals.

$$\left(\tau = r_f C_D = \text{Diode time Constant}\right)$$

τ is Mean life time of the minority carriers.

$$\therefore C_D = \frac{\tau}{r_f} = \frac{\tau I}{\eta V_T} \quad (1/r_f) \qquad \therefore r_f = \frac{\eta V_T}{I}.$$

$$C_D = \frac{\tau}{r_f} = \frac{\tau}{\frac{\eta V_T}{I}} = \frac{\tau \cdot I}{\eta \cdot V_T} //.$$

r_f = forward A.C resistance.

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Break-down Mechanisms in Reverse-biased p-n junction diode :-

Break-Down Mechanism :-

In Reverse-biased condition as long as the reverse voltage is less than breakdown voltage, the diode current is small and almost constant at I_o. But when reverse voltage increases beyond certain value, large diode current flows. This is called "Breakdown of diode" and corresponding voltage is called "Reverse breakdown voltage" V_{BR} of diode.

There are 2 distinct mechanisms due to which the breakdown may occur in the diode

These are

1) Avalanche breakdown
2) Zener breakdown.

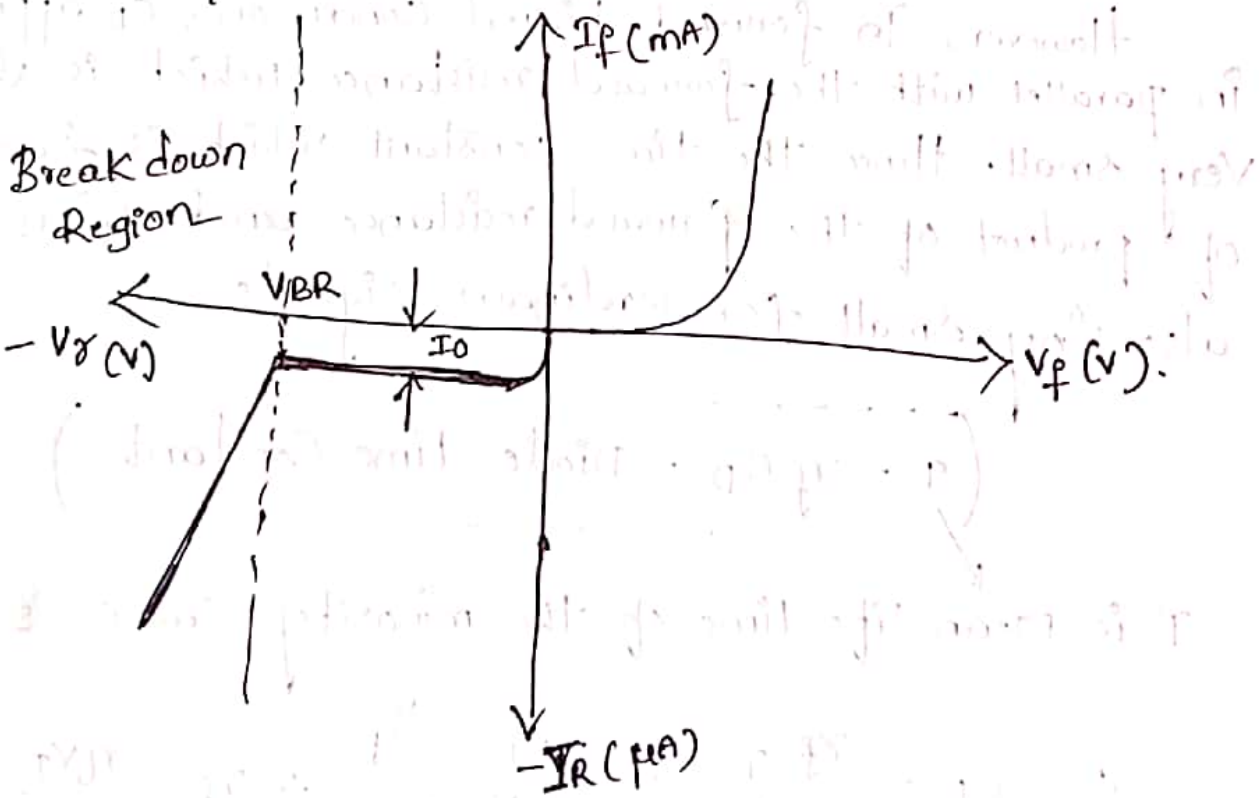

fig: Diode - characteristics

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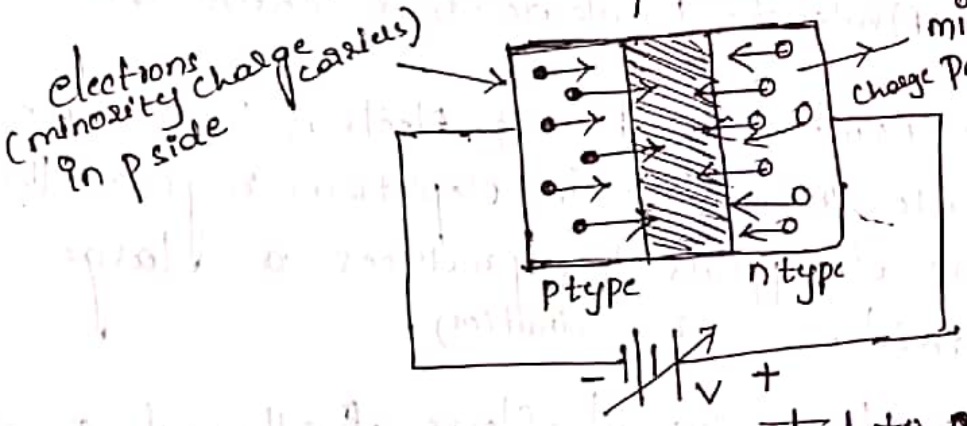
(1). Avalanche Breakdown :—

* As the reverse voltage increasrs, at particular value the velocity of minority carriers increases.
* Due to velocity, the same kinetic energy is associated with the minority carriers.
* Due to high velocity of carriers, the collision of minority carriers with the atoms takes place.
* The Collisions makes the electrons to break the Covalent bonds and becomes free electrons.
* The Newly generated carriers also get accelerated kinetic energy due to high velocity & high reverse voltage they also again colloide with another atoms to generate more minority carriers. This process is called "Carrier Multiplication".



In reverse bias + is connected to n type, '-' is connected to p type, current flows through depleting layer due to minority charge carriers only.

Here p-type having electrons are minority charged pair carriers, In n-type having holes are minority carriers, Depletion region Consits these minority Charged Carriers, due to these small current flows which is "reverse saturation Current".

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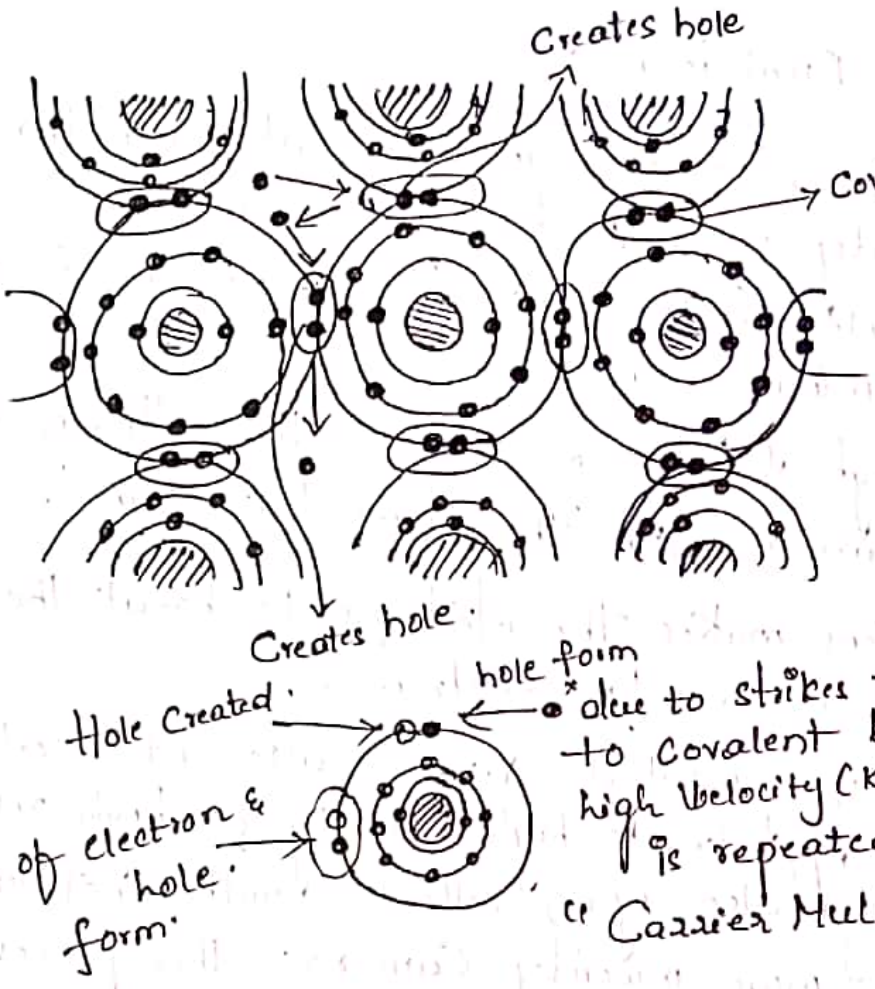

fig: Process of Carrier Multiplication in Avalenche Breakdown mechanism.

* Finally large number of holes & electron pairs are form these are recombine in depletion region then this pairs are disappears this produces a large amount of current. recombination.
* This large amount of current flows through junction due to this; breaking of the PN junction forms.
* This Effects the Breakdown region to damage the diode. this Effect is called- "Avalanche Breakdown" effect.

The mechanism of avalanche breakdown causes the reverse breakdown of P-N junction diode which destroys the device".

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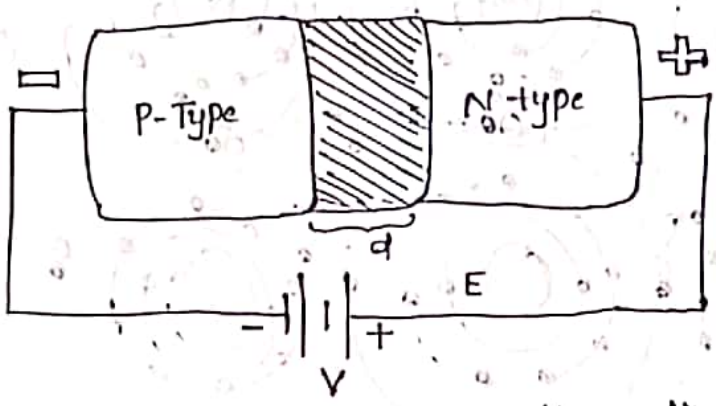
2). Zener breakdown :—



E = Electric field.
d = width of depletion layer
V = Applied voltage

$$E = \frac{V}{d}$$

The Electric field E is more then the width of depletion layer is less. When a p-n junction is heavily doped the depletion layer is very narrow. So under reverse bias conditions, the electric field across the depletion region and high reverse voltage, it is intense.

Such an intense field is enough to pull the electrons out of the valence bands of the stable atoms. So this is not due to collision of Carriers with atoms Such a Creation of free electrons is called Zener effect which is different than the avalanche effect.

" These Minority charge Carriers Constitute Very large Current and mechanism " is called " Zener breakdown ".

* The Diodes having reverse breakdown voltage between 3V to 8 / less than 5V show the Zener-mechanism of breakdown. This occurs for only Heavily doped diodes.

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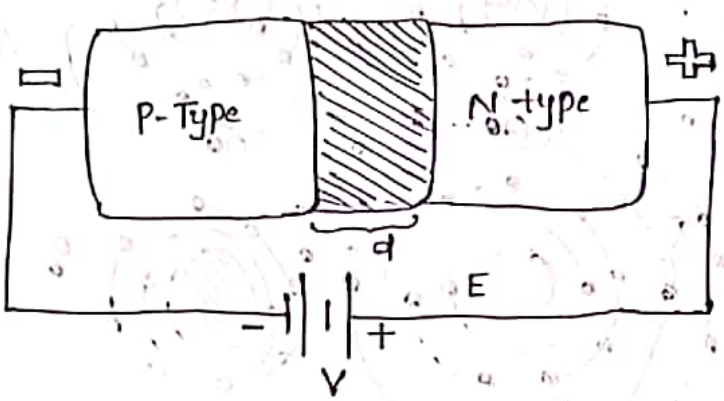
2). Zener breakdown :—



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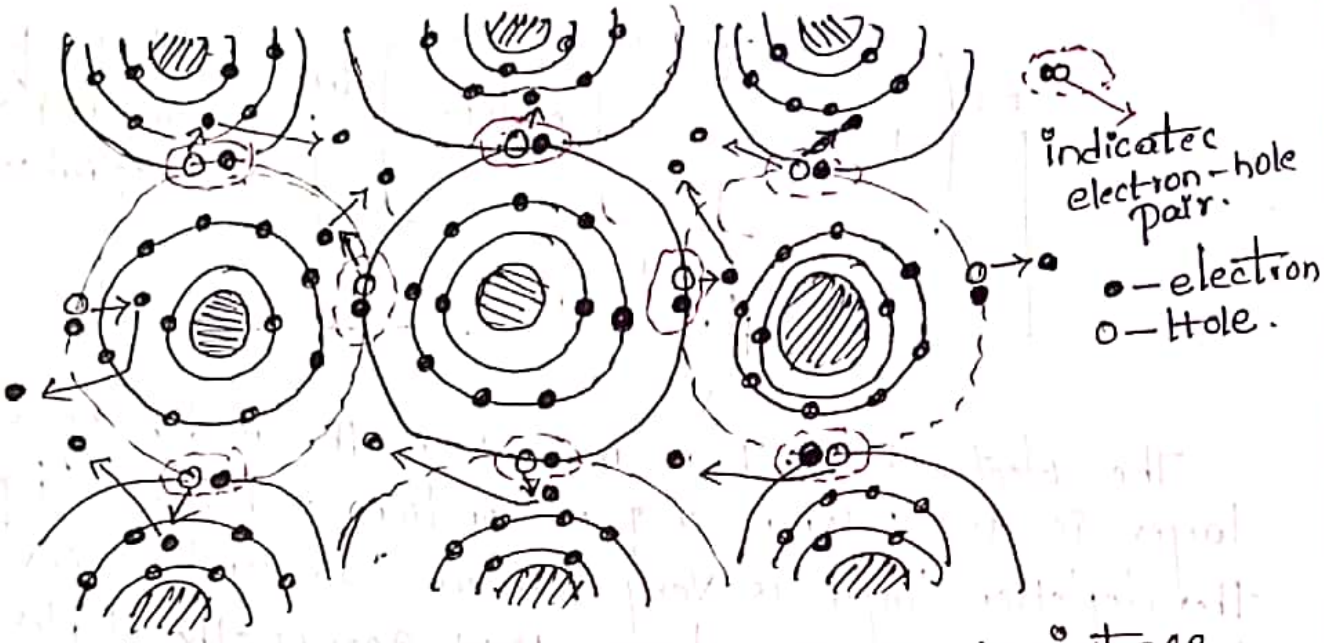

fig:- Breaking of covalent bonds due to intense electric field - form electron-hole pairs - due to this large current flows.

* For the Diodes having reverse breakdown rating between 5V to 6V, both Zener and avalanche mechanisms occure simultaneously.

* practically, In reverse biased condition, to avoid reverse breakdown, the voltage appearing across the diode must be less than its peak inverse voltage (PIV) rating.

PIV :- The breakdown voltage rating of a diode can be adjusted by changing the doping levels in the junction, at the time of manufacturing.

This decides the practical safe operating voltage rating of diode. It is called "peak-Inverse voltage" rating of diode.

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Current Components in a p-n junction Diode :-

* When p-n junction diode is forward biased, a large forward current flows, which is mainly due to majority carriers.
* The Depletion region near the junction is very very small under forward bias condition (f·B condition)
* In f·B condition holes get diffused into n side from P side while electrons get diffused into p-side from n side.
* so on p-side, the current carried by electrons which is diffusion current due to minority carriers (electrons) is decreases exponentially with respect to distance measured from the junction.
* The current due to electrons, on p-side which are minority carriers denoted as I_{np}.
* Ily, holes The current due to holes on n-side which are minority charge carriers denoted as I_{pn} with respect to distance measured from the junction. this current also decreases exponentially
* If distance is denoted by x.

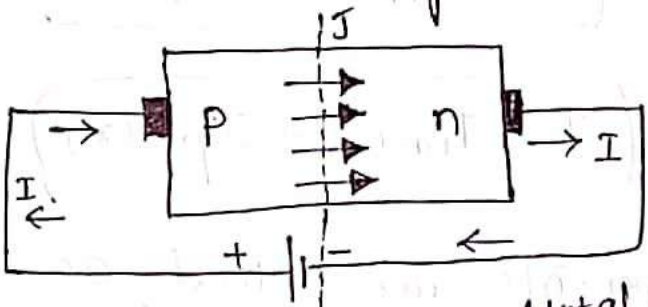
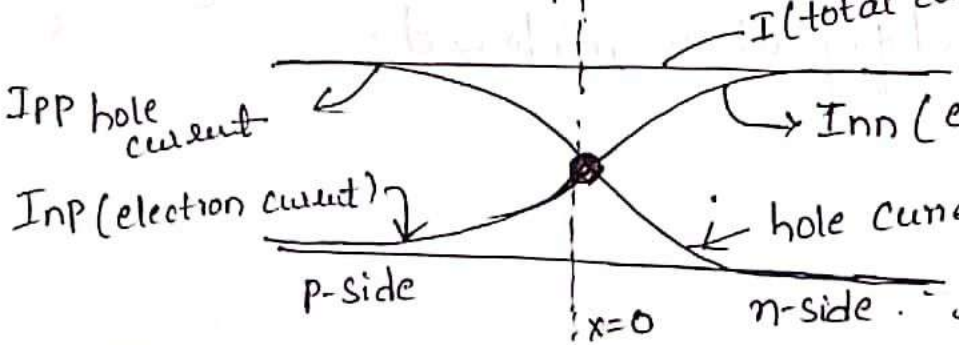


fig: Current Components.



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$I_{np}(x)$ = Current due to electrons in p-side as a function of 'x'.

$I_{pn}(x)$ = Current due to holes in n-side as a function of x.

At the junction $x = 0$:—

Electrons Crossing n side to p side Constitute Current $-I_{np}(0)$ in the same direction, as holes crossing the junction from p-side to n-side Constitute a current $I_{pn}(0)$.

Hence, Total Conventional current I is

$$I = I_{pn}(0) + I_{np}(0)$$

$I_{pn}(x)$ and $I_{np}(x)$ are olecreases on nside and p-side as we move away from junction.

on p-side exist a current due to holes (magority carriers) is $I_{pp}(x)$ = Current due to holes in p-side.

lly $I_{nn}(x)$ = Current due to electrons in n-side.

∴ on p-side, $I = I_{pp}(x) + I_{np}(x)$.

∴ on n-side, $I = I_{nn}(x) + I_{pn}(x)$

* The current Components are plotted as a function of olistance in fig above mentioned.

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from the figure, the Current decreases towards the junction (Ipp) at the junction enters the n side and becomes Ipn which further decreases exponentially.

Ily the current Inn decreases towards the junction, at the junction enters the p-side and becomes Inp which also further decreases exponentially.

So, finally Conclusion is,

Sum of the currents Carried by electrons and holes at any point inside the diode always Constant equal to forward current I.

Diode Current Equation :—
(V-I Characteristic equation of Diode).

The Diode Current Equation is gives the relationship between voltage (V) and Current (I) is given by

$$I = I_0 \left(e^{\frac{V}{\eta V_T}} - 1\right)$$

Where, I = Diode Current

I_0 = Diode reverse saturation Current at room temperature

V = Voltage externally applied to the diode

η = Constant (1 for Ge, 2 for Si)

V_T = Thermal voltage. $= \frac{KT}{q}$ volts

$V_T = \frac{KT}{q}$ $\boxed{V_T = KT}$ volts. 8.62×10^{-5} ev/°K

where K = Boltzmen Constant $= 1.3806 \times 10^{-23}$ J/K.

q = charge of e $= 1.6 \times 10^{-19}$ Coulombs

At room temp - T = 27° + 273° = 300° K

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V_T of semiconductor depends on temperature.

$\therefore V_T = \frac{KT}{q} = \frac{T}{q/K} = \frac{T}{11600}$ (where $\frac{q}{K} = \frac{1.6\times10^{-19}}{1.3\times10^{-23}} = 11600$)

at room temperature $V_T = \frac{300}{11600} \approx \frac{300}{2}$

∴ At room temperature of 27°C i.e $T = 27+273 = 300^0K$ and the value of $V_T = 26$ mV.

$V_T = K\cdot T$
$= 8.62\times10^{-5}\times300$
$= 0.02586 \simeq 0.026$
$V \simeq 26$ mV at room temp.

V_T can be expressed as

$$V_T = \frac{T}{\left(\frac{1}{K}\right)} = \frac{T}{\left(\frac{1}{8.62\times10^{-5}}\right)} = \frac{T}{11600}$$

$$\left(V_T = \frac{T}{11600}\right)$$

for, forward biased V must be taken as positive and we get current I positive which is forward current.

for, reverse biased, V must be taken negative and we get negative current I which indicates that it is reverse current.

Current equation $I = I_0\left[e^{V/\eta V_T} - 1\right]$

divides by Area of cross-section of junction 'A' on both sides

$$\frac{I}{A} = \frac{I_0}{A}\left[e^{V/\eta V_T} - 1\right)$$

$$\therefore J = J_0\left(e^{V/\eta V_T} - 1\right) \text{ A/m}^2.$$

where J = forward current density

J_0 = Reverse saturation current density.

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Nature of V-I characteristics from equation of diode :—

Consider a current equation of diode as

$$I = I_0 (e^{V/\eta V_T} - 1)$$

for forward bias :— → index has positive sign.

due to this exponential $V/\eta V_T$

V is positive, so, $1 << e$ hence neglect 1

we get, $$I_f = I_0 e^{\frac{V}{\eta V_T}}$$

It indicates, once bias voltage exceeds cut in voltage, the forward current increases exponentially.

for Reverse bias :—

The bias voltage V is negative, due to this exponential index has negative sign.

so, $e^{-V/\eta V_T} << 1$ hence neglecting $e^{-V/\eta V_T}$

we get $$I_R = I_0 (-1) = -I_0$$

$$I_R = -I_0$$

It indicates under reverse bias, the current is reverse saturation current which is negative indicating i.e it flows in opposite direction to that of forward current.

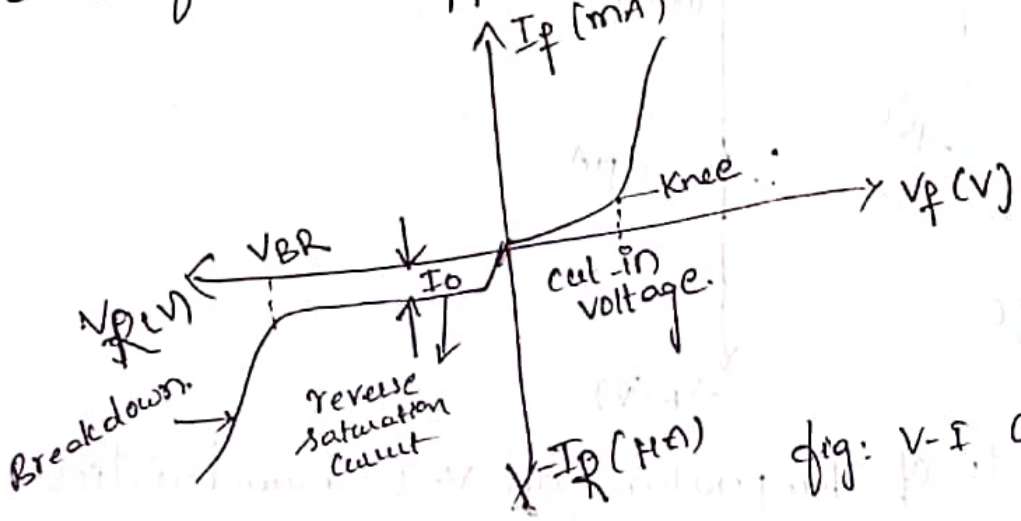

fig: V-I Characteristics of p-n junction diode

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Temperature Dependance on V-I Characteristic of Diode :—

V-I characteristics of diode is a plot between Voltage and current Variation, Temperature dependance on V-I characteristics of diode means how does the voltage and current of the diode can be change by changing the temperature. In this, we are seperately shows the what is the effect of temperature on current and what is the effect of temparature on voltage.

i.e., if we are increasing / decreasing temperature, the volt-amphere characteristics of diode changes significantly. This change in V-I characteristic is observe in both forward and reverse bias condition.

Let us Consider V-I characteristics of Si- Diode.

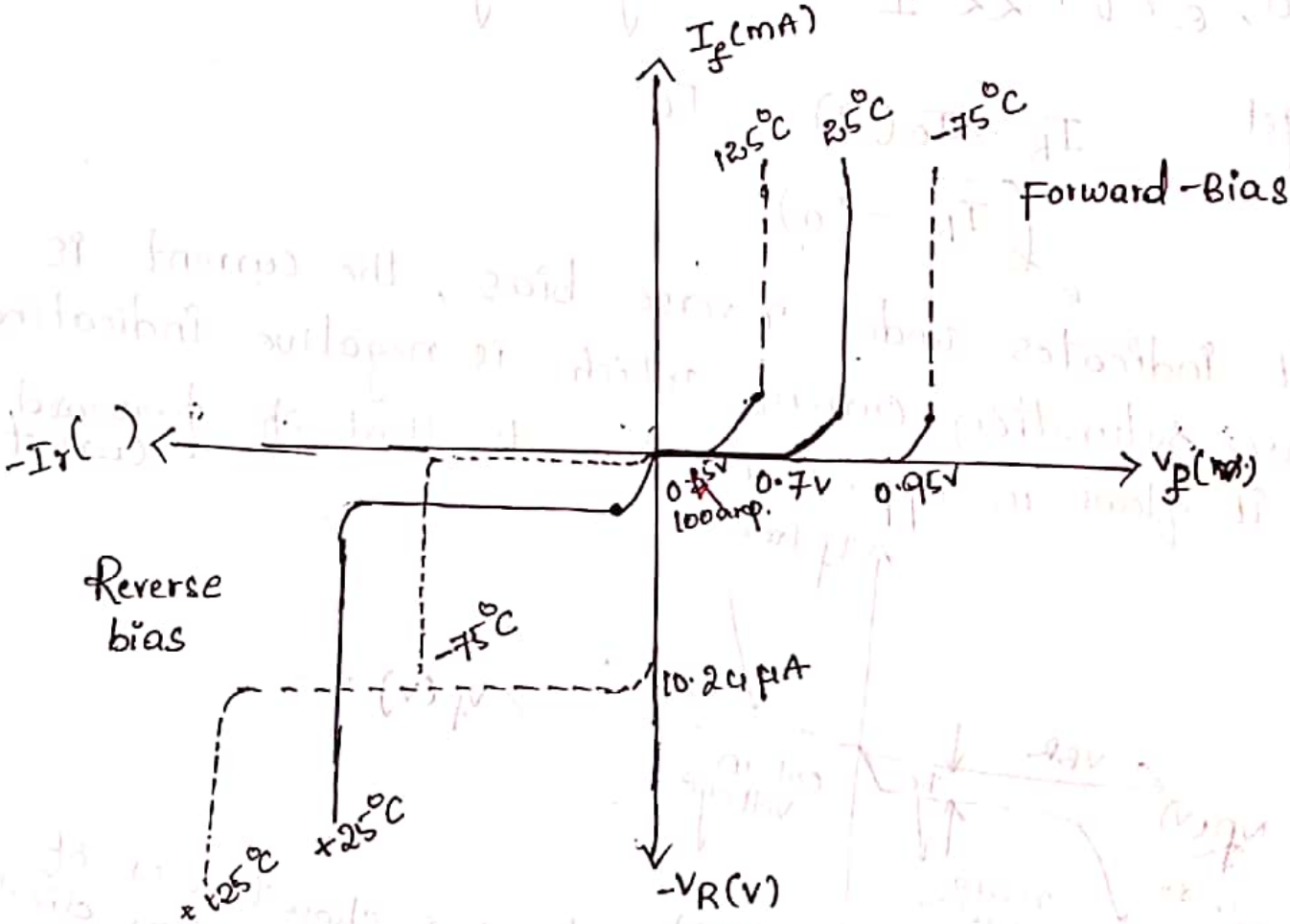

fig: Effects of Temperature on V-I characteristics

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Forward bias Condition :-

*** In Case of forward bias region, the characteristics of si-diode shift to the left at the rate of 2.5mv/C° (2.5mv per degree Centigrade) rise in temperature. and

if we decrease the temperature at the rate of 2.5mv/C° the characteristics of si-diode shifts to the right.

for ex :- $25^\circ C \longrightarrow V_f = 0.7V$,

$\Longrightarrow$ for 100°c rise in temperature i.e., $100 + 25 = 125^\circ C$

$\therefore V_f = 100 \times 2.5mV = 0.25V$.

i.e V_f reduced (↓) by 0.25 V.

New Voltage across diode is reduced by 0.25V i.e

Temperature $\propto \frac{1}{V_f}$ $V_{f(new)_1} = (0.7 - 0.25)V$ $V_f \propto \frac{1}{T}$

$V_f \rightarrow \boxed{V_{f(new)_1} = 0.45V}$

$\Longrightarrow$ for 100°c reduces in temperature i.e., 100-25 = 75°C

$25 - 100^\circ C = -75^\circ C$

$\therefore V_f = 100 \times 2.5mV = 0.25V$

New voltage across diode is increased by 0.25V.

i.e., $(V_f)_{new_2} = (0.7 + 0.25)V$

$V_f \rightarrow \boxed{V_{f(new_2)} = 0.95V}$

* i.e., If increase the temperature voltage across the diode is reduced, this is not reduced in voltage across the diode is not random. This voltage across the diode is not random voltage but it is equal to the barrier potential at this current rises exponentially.

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So, we can say Barrier potential is increases when decrease in temperature, Barrier potential is decreases when increase in temperature.

This new plot of forward V-I characteristics shows below:

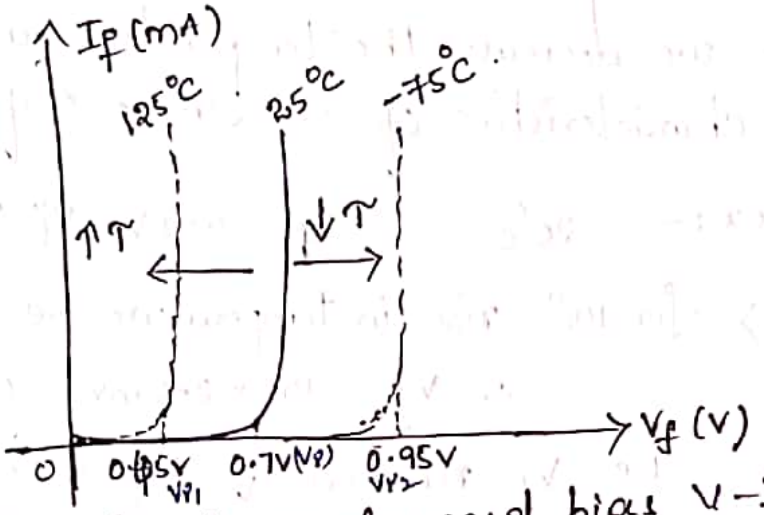
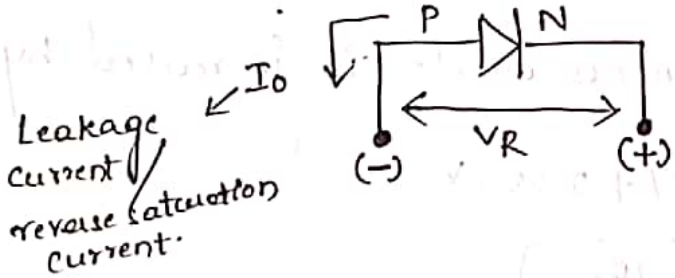


fig: Temperature Effect on forward bias V-I characteristics of diode.

Reverse bias Condition :—

In this condition, positive terminal is connected to n-type negative terminal of battery is connected to p-type Let us take a connection of diode in reverse bias:



V_R is negative.

For reverse bias condition :→

*** "The Reverse saturation Current I_o (or) I_s doubles for every 10°C rise in temperature"

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Ex: case (1) for 100°C rise in temperature to 25°C
i.e 100 + 25 = 125°C.

We know that for every 10°C rise in temperature reverse saturation current doubles.

i.e

25°C ⟶ 10nA
35°C ⟶ 20nA
45°C ⟶ 40nA
55°C ⟶ 80nA
160
320
640
1280
125°C ⟶ 10,240nA (or) 10.24μA.

∴ The new reverse saturation current (I_S) is 10.24μA.
i.e I_S (reverse-saturation current) increases if we increase in temperature.

Similarly, by using same above process if we calculate at −75°C i.e decreasing temperature at +25°C

i.e +100°C ← 25°C − 100°C = −75°C.

for every 10°C reduces in temperature the reverse saturation current also reduces, very small current.

i.e Temperature increases ⟶ Reverse saturation current increases.

Temperature decreases ⟶ Reverse saturation current decreases.

Breakdown voltage at 25°C

∴ The Reverse breakdown voltage of diode may increase (or) decreases depends on Zener potential.

we have to be careful in reverse bias Condition, I_S increases if we increase in temperature it damage the diode. The reverse saturation current will should be closer to 10pamp for High temperature applicatio

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I_s closer to 10 pA → for High temperature applications.

In case of 'Ge' the reverse saturation current is high so we not prefer Ge in practical applications.

for Si have reverse saturation current is less than the 'Ge'.

The temperature dependance on voltage & current can be taken by the following equations

We know Diode equation of current $I = I_0(e^{V/\eta V_T} - 1)$.

for Current :- $I_{O2} = I_{O1}\, 2^{(T_2 - T_1)/10}$

Where $T_2 = T_1 + 10$

I_{O1}, I_{O2} are the effects of reverse saturation current I_O

I_{O1} = Value of I_O at temperature T_1

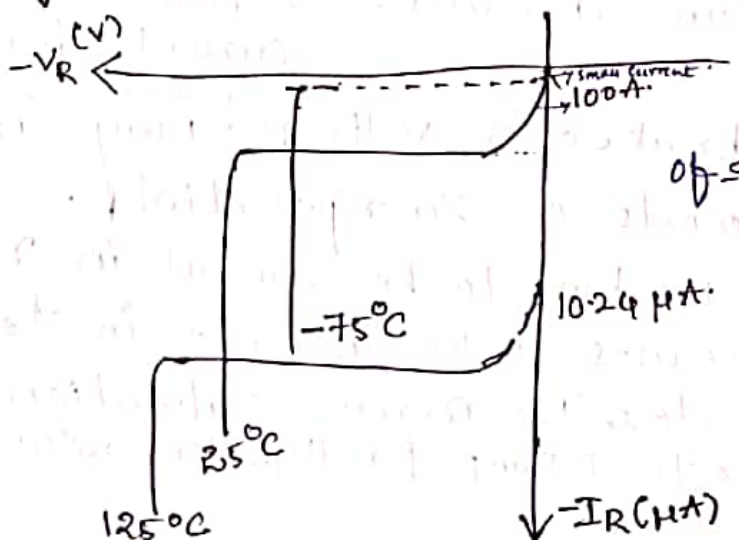
I_{O2} = Value of I_O at temperature T_2.

$T_2 = T_1 + 10$

i.e for every 10°C rise in temperature current gets doubled.

for Voltage :- $\frac{dV}{dT} = -2.5\ mV/C^o$.

For every one degree Centigrade rise in temperature the cut-in voltage of diode decreased by 2.5 mV.



Effect of Temperature on (V-I) characteristics of Reverse bias Condition.

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Energy band Structure / Diagram of PN Junction diode :-

Energy band :- The electrons in same orbit exhibits different energy levels. The grouping of this different energy is called "energy-band".

Energy bands are classified into mainly 3-types

(1). Valence band
(2) Conduction band
(3) forbidden band (or) gap

Along these bands another energy level is present which is "fermi energy level".

* "Valence band is formed due to merging of energy level associated with the "valence electrons".
* "Conduction band is formed due to merging of energy levels associated with the "free-electrons".
* forbidden gap is used to separating the Conduction & Valence band which is present between Conduction & Valence band.

Fermi Energy level :- Fermi level is a direct level which has 50% propbability of occupation by an electron at any temperature, in the energy band diagram.

for intrinsic semiconductor, the number of electrons in Conduction band is equal to number of holes in Valence band. So probability of these two also equal

i.e $$P_c(e) = P_v(+)$$

probability of electrons in conduction band $= P_c(e)$

probability of holes in Valence band $= P_v(+)$

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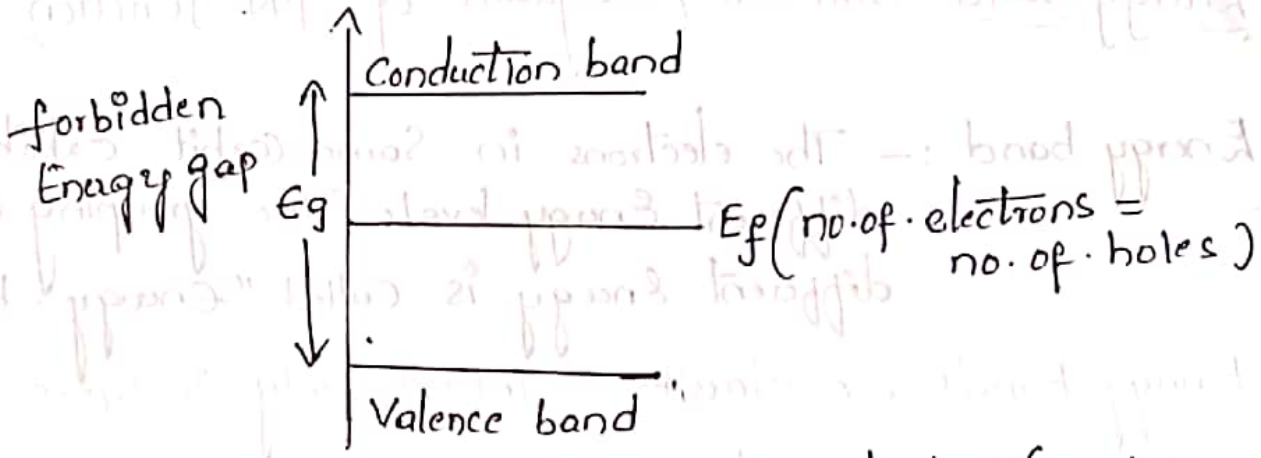

fig : Fermilevel of Intrinsic Semiconductor ($e = h$)

* If the electrons are more than the holes the fermilevel moves up, similarly number of holes are more than the electrons fermilevel moves down.

Fermi-level of Extrinsic Semiconductor :-

In Extrinsic, there are 2 types ① P-Type ② N-Type

* In p-type, the conduction mainly happens due to holes, In n-type the Conduction happens due to electrons.

P-Type :- The Condition is $P_c(e) < P_v(H)$ (or) $P_v(H) > P_c(e)$

Where $P_c(e)$ = The probability of finding by electron in Conduction band.

$P_v(H)$ = The probability of finding by hole in the valence band.

So, E_f (fermi-level) is very close to Valence-band

$$P_v(H) > P_c(e)$$

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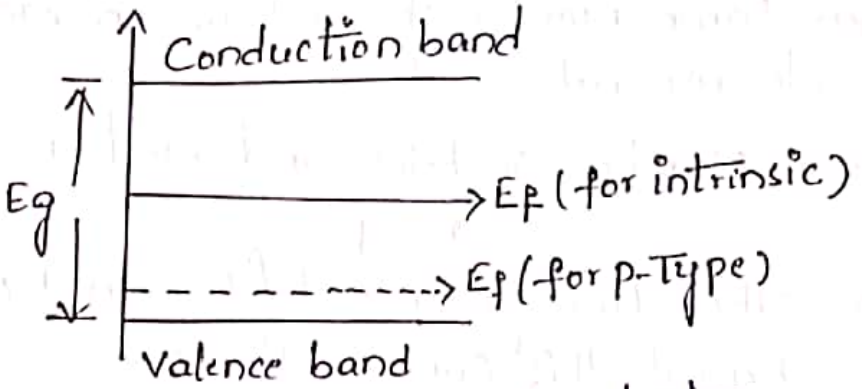
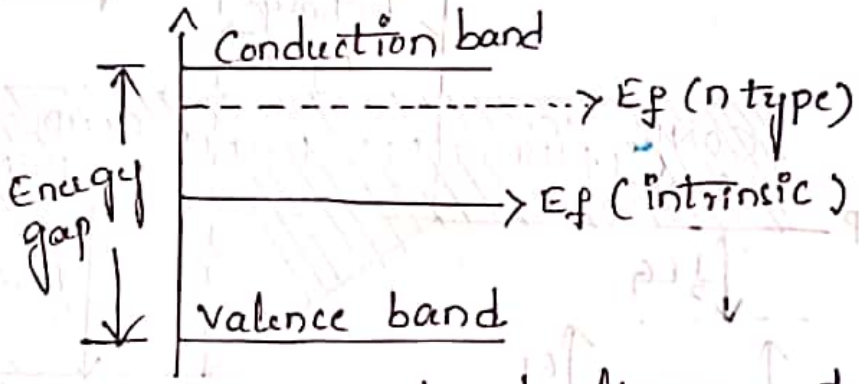


fig: fermi-level of p-Type Semiconductor.

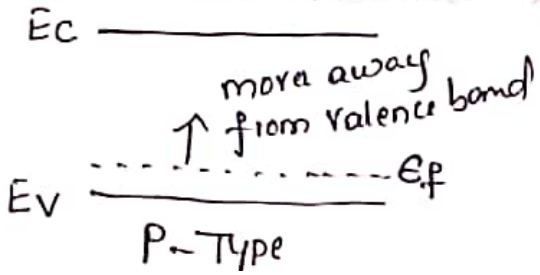
N-Type :- The Condition is $P_c(e) > P_v(H)$

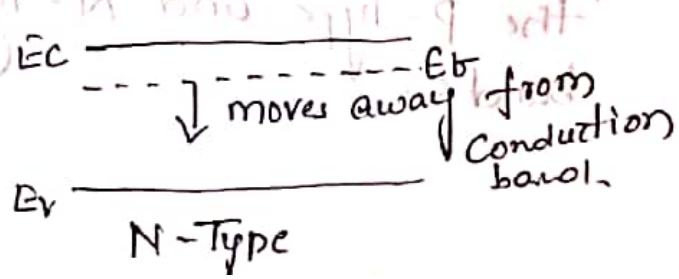
Here, the probability of finding electrons in Conduction band is greater than the probability of finding hole in the Valence band. So, the fermilevel is very close to Conduction band.



Band Structure (or) Energy band diagram for P-N-junction :-

When forming P-N junction holes are diffused from p to n side, so p-side number of holes are reduced, then the fermienergy level moves away from Valence band. Ily electrons diffused from N→P so, In n-side number of electrons are reduced then the fermi-energy level moves away from Conduction band.





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* When Same number of electrons on n-side and holes on p-side are diffused.

i.e., Number of holes and electron are equal

$$n = p$$

Then, the two fermi-level (fermilevel of n & p) are Equal this can be shown.

* In order to make Equal number of holes, electrons in terms of fermilevel, the p-Type Semiconductor moves up and n-type Semi-conductor moves down, between these two slant suface Exist. This region of slant space is " Depletion region.

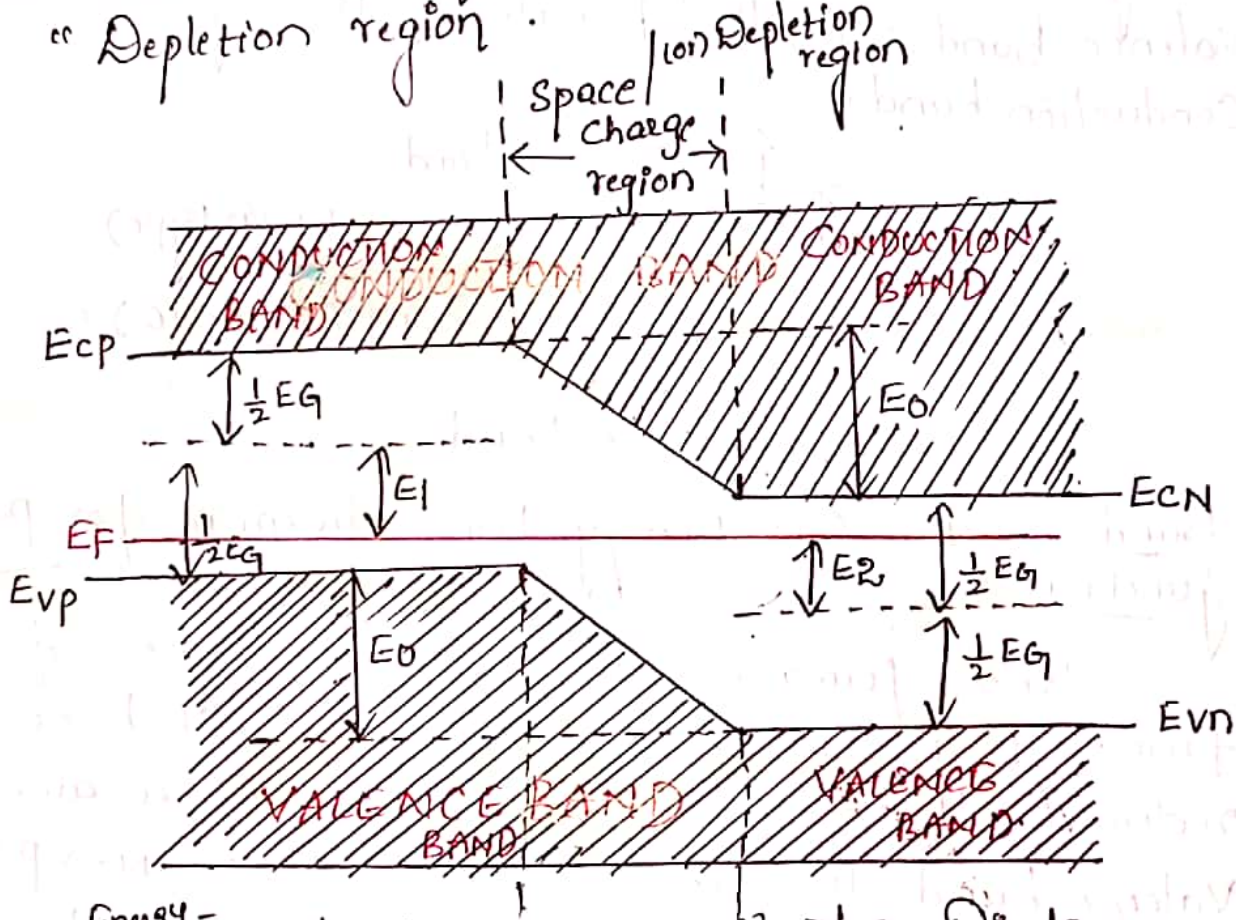

fig:- Band structure of p-N junction Diode.

From the structure, p-N junction forms by Combining the p-Type and N-Type Semiconductor's Enagy bands.

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from this,

E_0 = potential energy of electrons ($\bar{e}$) at the junction

$$\therefore E_0 = (E_{CP} - E_{CN}) + (E_{VP} - E_{VN})$$

$$E_0 = E_1 + E_2$$

$$E_F - E_{VP} = \frac{1}{2} E_G - E_1 \longrightarrow (1)$$

$$E_{CN} - E_F = \frac{1}{2} E_G - E_2 \longrightarrow (2)$$

Add (1) & (2)

$$E_1 + E_2 = E_G - (E_{CN} - E_F) - (E_F - E_{VP})$$

$$\therefore \boxed{E_0 = E_G - (E_{CN} - E_F) - (E_F - E_{VP})} \text{ //}.$$

Where E_{CP} = Conduction band Edge in P-type material

E_{CN} = Conduction band Edge in N-type material

E_{VP} = ~~Conduction~~ valence band Edge in P-type material

E_{VN} = valence band Edge in N Type material.

E_F = fermi-level

E_G = forbidden-Energy gap //.

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PROBLEMS - on Diode Current Equation

1. A Silicon diode has a reverse Saturation Current of 7.12 nA at room temperature of 27°C. Calculate its forward current if it is forward biased with the voltage of 0.7 V ?

Given that,

Reverse Saturation Current = $I_0 = 7.12\ nA = 7.12 \times 10^{-9} A$

Applied voltage $V = 0.7V$

At room temperature of 27°C mean

$T = 27^\circ C + 273 = 300^\circ K$

for Silicon diode $V_\gamma = 0.7V$ and $\eta = 2$

The Diode - current equation is

$$I = I_0\left[e^{(V/\eta V_T)} - 1\right)$$

$$= 7.12 \times 10^{-9}\left[e^{\frac{0.7}{2 \times V_T}} - 1\right]$$

$$= 7.12 \times 10^{-9}\left[e^{\frac{0.7}{2 \times 0.026}} - 1\right]$$

$$= 7.12 \times 10^{-9}\left(e^{13.461} - 1\right)$$

$$= 7.12 \times 10^{-9}\left(700,815.545 - 1\right)$$

$$= 7.12 \times 10^{-9}\left(700,814.545\right)$$

$$= 4,989,799.56 \times 10^{-9}$$

$$= 4.989 \times 10^{6} \times 10^{-9}$$

$$I = 4.98 \times 10^{-3} \approx 4.98\ mA \approx 5\ mA\ //.$$

Where

$V_T = K \cdot T$

at room temp

$V_T = 8.62 \times 10^{-5} \times 300$

$= 0.0258V$

$V_T = 0.026V.$

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(2). The voltage across a Silicon diode at room temperature of 300°K is 0.71 V when 2.5 mA current flows through it. if the voltage increases to 0.8 V, Calculate the New diode current?

The current equation of diode is

$$I = I_0 (e^{V/\eta V_T} - 1)$$

At 300°K $V_T = 26\,mV = 26 \times 10^{-3} V$

$V = 0.71\,V$ for $I = 2.5\,mA$, $\eta = 2$ for Si

$$\therefore \quad 2.5 \times 10^{-3} = I_0 \left[e^{\left(\frac{0.71}{2 \times 26 \times 10^{-3}}\right)} - 1 \right]$$

$$2.5 \times 10^{-3} = I_0 \left[e^{13.653} - 1 \right]$$

$$2.5 \times 10^{-3} = I_0 \left(850{,}007.116 - 1 \right)$$

$$2.5 \times 10^{-3} = I_0 \left(850{,}006.116 \right)$$

$$I_0 = \frac{2.5 \times 10^{-3}}{850{,}006.116}$$

$$= \frac{2.5 \times 10^{-3}}{8.5 \times 10^{5}} = \frac{2.5}{8.5} \times 10^{-3} \times 10^{-5}$$

$$= 0.294 \times 10^{-8} = 0.294 \times 10^{-8} \times \frac{10}{10}$$

$$I_0 = 2.94 \times 10^{-9} \text{ A}.$$

Now $V = 0.8\,V$.

$$I = 2.93 \times 10^{-9} \left[e^{\left(\frac{0.8}{(2 \times 26 \times 10^{-3})}\right)} - 1 \right]$$

$$= 2.93 \times 10^{-9} \left[e^{15.38} - 1 \right]$$

$$= 2.93 \times 10^{-9} \left(4780233.73 - 1 \right)$$

$$= 2.93 \times 10^{-9} \times 4780232.73$$

$$= 2.93 \times 10^{-9} \times 4.78 \times 10^{6}$$

$$I = 14.0054 \times 10^{-3} \simeq 14.1\,mA.$$

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(37) A Ge diode has a reverse saturation current of 3 μA. Calculate the forward bias voltage at the room temperature of 27°C and 1% of the rated current is flowing through the forward biased diode. The Diode forward rated current is 1A ? (38)

Given values are

$I_0 = 3\,\mu A$

$T = 27^\circ C = 27 + 273 = 300^\circ K$

$\eta = 1$

$I_{rated} = 1A$ for diode

$\therefore I = 1\%$ of I_{rated}

$I = 1/100 \times (1) = 0.01A$

$V_T = KT = 8.62 \times 10^{-5} \times 300 = 0.026V$

According to Diode equation

$$I = I_0\left(e^{V/\eta V_T} - 1\right)$$

$$0.01 = 3 \times 10^{-6}\left(e^{V/1 \times 0.026} - 1\right)$$

$$3333.333 = e^{\frac{V}{0.026}} - 1$$

$$\frac{V}{0.026} = 3333.333 + 1$$

$$e^{V/0.026} = 3334.333$$

.... Taking Natural log on both sides

$$\ln\left(e^{V/0.026}\right) = \ln(3334.333)$$

$$\frac{V}{0.026} = 8.112$$

$$V = 8.112 \times 0.026$$

$$\boxed{V = 0.2109V}$$ //.

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④ A Diode operating at 300°K at a forward voltage of 0.4V carries a current of 10mA. When voltage is changed to 0.42V, the current becomes twice, Calculate the value of reverse saturation current and η for the diode?

$V_1 = 0.4V$, $I_1 = 10\,mA$

$V_2 = 0.42V$, $I_2 = 2I_1 = 2\times10 = 20\,mA$.

Now, $I = I_0\left(e^{\frac{V}{\eta V_T}} - 1\right)$

$$10\times10^{-3} = I_0\left(e^{\frac{0.4}{\eta\times0.026\times10^{-3}}} - 1\right) \longrightarrow (1)$$

$$20\times10^{-3} = I_0\left(e^{\frac{0.42}{\eta\times0.026\times10^{-3}}} - 1\right) \longrightarrow (2)$$

In forward bias condition $1 << e^{V/\eta V_T}$ .. neglecting 1.

$$\therefore \quad 10\times10^{-3} = I_0\, e^{\frac{15.38}{\eta}} \longrightarrow (3)$$

$$\therefore \quad 20\times10^{-3} = I_0\, e^{\frac{16.153}{\eta}} \longrightarrow (4)$$

Dividing (3) by (4)

$$\frac{1}{2} = \frac{e^{15.38/\eta}}{e^{16.153/\eta}}$$

$$2\,e^{15.38/\eta} = e^{16.153/\eta}.$$

Taking Natural Logarithm of both sides

$$\frac{16.153}{\eta} = \ln 2 + \frac{15.384}{\eta}$$

$$\frac{1}{\eta}(16.153 - 15.384) = 0.6931$$

$$\eta = 1.109$$

$$I_0 = 9.45\,nA$$

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(5). A Silicon diode has a Saturation Current of 7.5 μA at room temperature 300K. Calculate the Saturation Current at 400K?

Given $I_{O1} = 7.5 \times 10^{-6}$ A at $T_1 = 300K \Rightarrow 27^{\circ}C + 273K$.

$T_1 = 27^{\circ}C$

Ily $T_2 = 400K = 127^{\circ}C + 273^{K} =$.

$T_2 = 127^{\circ}C$

∴ The Saturation Current at 400K is

$$I_{O2} = I_{O1} \times 2^{(T_2 - T_1)/10}$$

$$= 7.5 \times 10^{-6} \times 2^{(127-27)/10}$$

$$I_{O2} = 7.5 \times 10^{-6} \times 10^{10} = 7.68 \text{ mA} //.$$

(6). The Reverse Saturation current of the ~~transistor~~ diode is 2 μA at room temperature of 25°C and increases by a factor of 2 for each temperature of 10°C. find the reverse saturation Current of the ~~transistor~~ diode at a temperature of 75°C?

Given $I_{O1} = 2\mu A$ at $T_1 = 25^{\circ}C$, $T_2 = 75^{\circ}C$

∴ The Reverse Saturation Current of the transistor at $T_2 = 75^{\circ}C$ is

$$I_{O2} = I_{O1} \times 2^{(T_2 - T_1)/10} = 2 \times 10^{-6} \times 2^{\left(\frac{75-25}{10}\right)}$$

$$= 2 \times 10^{-6} \times 2^5 = 64\mu A$$

$$I_{O2} = 64\mu A$$

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Problems on Resistance (Static / Dc and Dynamic / Ac)

(1). Find the value of Dc resistance and ac resistance of a germanium junction diode at 25°C with I_0 is 25 μA and at an applied voltage of 0.2V across the diode ?

Given $I_0 = 25\mu A$

$T = 25°C = 25 + 273 = 298\ K$

$V = 0.2V$

$\therefore \boxed{I = I_0(e^{V/\eta V_T} - 1)}$

$= 2.5 \times 10^{-6}\left(e^{\frac{0.2}{26 \times 10^{-3}}} - 1\right)$

$I = 54.79\ mA$.

Dc resistance :—

$\boxed{R_f = \frac{V_f}{I_f}}$ → for forward bias.

$R = \frac{V}{I} = \frac{0.2V}{54.79mA} = 3.65\Omega$ $\boxed{R = 3.65\Omega}$

Ac resistance :—

For Ge ⇒ $\eta = 1$ $V_T = \frac{KT}{q} = 25.71\ mV$

A.C resistance $\boxed{r_f = \frac{\eta V_T}{I}}$ → under reverse bias

$r_f = \frac{\eta V_T}{I} = \frac{25.71 \times 10^{-3}}{54.79 \times 10^{-3}}$

$\therefore \boxed{r_F = 0.47\Omega}$

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12). Calculate the Dynamic forward and reverse resistance of a PN junction diode when the applied voltage is 0.25V at T = 300K given $I_0 = 2\mu A$.

Given $V = 0.25\,V$

$T = 300K$

$I_0 = 2\mu A$

At $T = 300K$, $V_T = 26\,mV$

Assuming it to be silicon diode $\eta = 2$

$$\therefore I = I_0\left(e^{V/\eta V_T} - 1\right)$$

$$= 2\times10^{-6}\left(e^{0.25/2\times26\times10^{-3}} - 1\right)$$

$$I = 0.24\,mA$$

For Ge diode, $\eta = 1$

$$I = I_0\left(e^{V/\eta V_T} - 1\right)$$

$$= 2\times10^{-6}\left(e^{\frac{0.25}{26\times10^{-3}}} - 1\right)$$

$$I = 0.03A$$

$$r_f = \frac{\eta V_T}{I} = \frac{26\times10^{-3}}{0.03} = 0.867\,\Omega$$

$$r_f = 0.867\,\Omega$$

Reverse Resistance $(r_f) = \frac{V}{I_0} = \frac{0.25}{2\times10^{-6}} = 125\,K\Omega$.

$$r_f = \frac{V}{I_0}$$

$$r_f = 125\,K\Omega$$

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* The voltage across a Si – Diode at room temperature (300K) is 0.7 volts. When 2 mA current flows through it. If the voltage increases to 0.7V. Calculate the diode current (assume $V_T = 26mV$).

Given data

at room temperature $T = 300\,K$

voltage across a silicon diode $V_{D1} = 0.7V$

Current through the diode $I_{D1} = 2\,mA$

When voltage increases to 0.75V V_{D2} then,

$$\frac{I_{D2}}{I_{D1}} = \frac{I_o\left(e^{V_{D2}/\eta V_T} - 1\right)}{I_o\left(e^{V_{D1}/\eta V_T} - 1\right)}$$

$$= \frac{\left(e^{(0.75/2\times 25.7\times 10^{-3})} - 1\right)}{\left(e^{0.7/2\times 25.7\times 10^{-3}} - 1\right)} = \frac{2172608.828}{821326.3605}$$

$$= 2.64$$

$$\therefore \frac{I_{D2}}{I_{D1}} = 2.64 \quad (\text{where } I_{D1} = 2\,mA)$$

$$I_{D2} = I_{D1} \times 2.64 = 2.64 \times 2 \times 10^{-3}$$

$$\boxed{I_{D2} = 5.3\,mA}$$

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(5). A Silicon diode has a Saturation Current of 7.5 μA at room temperature 300K. Calculate the Saturation Current at 400K?

Given $I_{O1} = 7.5 \times 10^{-6}$ A at $T_1 = 300K \Rightarrow 27^{\circ}C + 273K$

$T_1 = 27^{\circ}C$

Ily $T_2 = 400K = 127^{\circ}C + 273^{K} =$

$T_2 = 127^{\circ}C$

∴ The Saturation Current at 400K is

$$I_{D2} = I_{O1} \times 2^{(T_2 - T_1)/10}$$

$$= 7.5 \times 10^{-6} \times 2^{(127-27)/10}$$

$$I_{O2} = 7.5 \times 10^{-6} \times 10^{10} = 7.68 \text{ mA} //.$$

(6). The Reverse Saturation current of the ~~transistor~~ diode is 2 μA at room temperature of 25°C and increases by a factor of 2 for each temperature of 10°C. Find the reverse saturation Current of the ~~transistor~~ diode at a temperature of 75°C?

Given $I_{O1} = 2\mu A$ at $T_1 = 25^{\circ}C$, $T_2 = 75^{\circ}C$

∴ The Reverse Saturation Current of the ~~transistor~~ at $T_2 = 75^{\circ}C$ is

$$I_{O2} = I_{O1} \times 2^{(T_2 - T_1)/10} = 2 \times 10^{-6} \times 2^{\left(\frac{75-25}{10}\right)}$$

$$= 2 \times 10^{-6} \times 2^5 = 64\mu A$$

$$I_{O2} = 64\mu A$$

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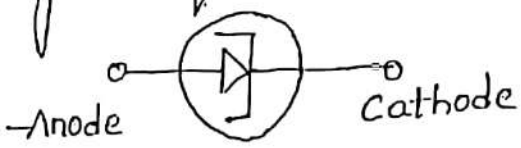
TUNNEL DIODE :-

→ Tunnel Diode Symbol
→ Tunnel Diode basics
→ Tunnel Diode structure
→ Tunnel Diode Working
→ Tunnel Diode characteristics
→ Band diagram's (Tunnelling of Electrons)
→ Advantages & Disadvantages
→ Applications

1. Symbol :- The Symbol of Tunnel Diode is



2. Basics :-

* It is invented by "Leo Esaki" in 1957. Based on that he have received Nobel in 1973.
* Sony have manufactured tunnel diode 1st in 195 From 1960 onwards other Companies like "General Electrical" have started manufacturing of tunnel di
* The Basic operation of Tunnel diode is, it is us for "fast-switching" characteristic
* It is (Tunnel diode) utilized in Microwave wave applications.
* The working of Tunnel diode is based on "Quantum Mechanical Tunneling".
* (i) Highest from room temperature, Solid state Oscil -t are based on (RTD) "Resonant Tunnelling diode".
(ii) Metal Insulator Metal (MIM) : mostly it is used in "Research based Applications".
* It is also called as "ESAKI DIODE".

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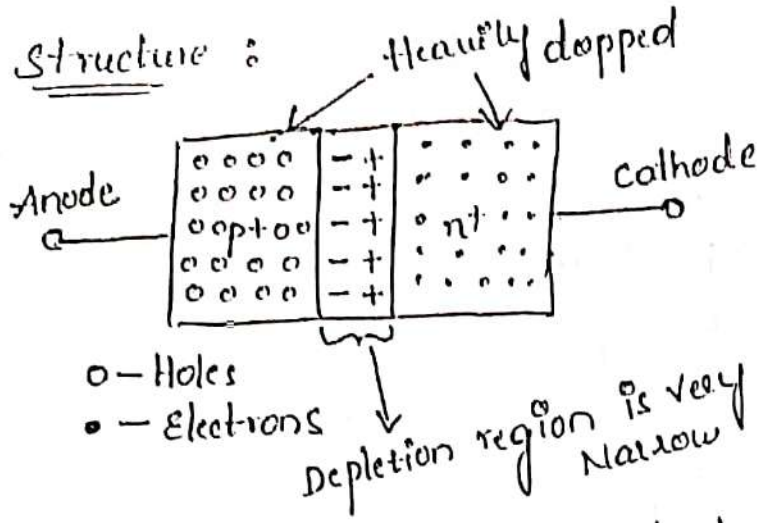
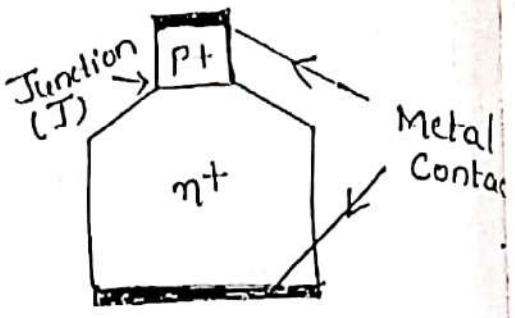
Structure :





* The structure of Tunnel diode include p+ and n+ m
These are Heavily - doppeal.
* Heavily - dopped means, the dopping Concentration a
P and n type Semiconductor materials are very hi
* Due to this heavily dopped p and n type Semicond
the "Depletion region" is very narrow (small), tha
the normal p-n junction diode.
* In the fabrication of tunnel diode, the p+ materia
is very small than the n+ material i.e size of
p-type is very small, than the n-type material.
* At the top of p-type and at bottom of n-type ma
a metal contacts are present shown in figure (b
* In Tunnel diode. P and n materials are fabricated wi
the materials are
  - ∝ Gallium Arsenide (GaAs)
  - ∝ Gallium Antimonide (Gasb)
  - ∝ Si (Silicon)
* A Junction is present in between p and n type
of Tunnel diode.
* The main difference between the Tunnel diode &
p-N diode is, In tunnel diode the p and n
are heavily dopped but in p-N junction diode

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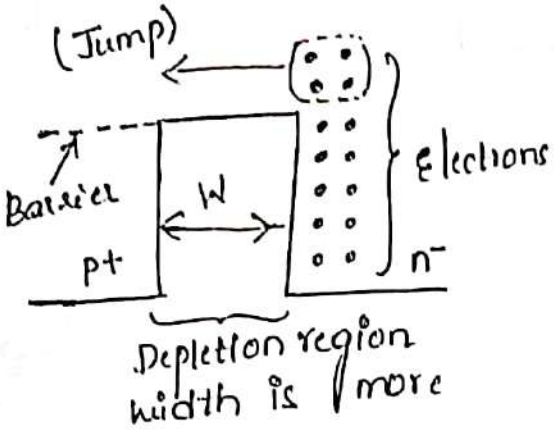
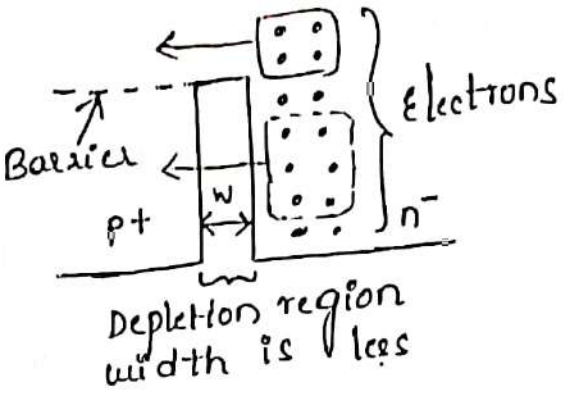
Working :—



(a) In Normal P-N Diode



(b) In Tunnel Diode

* In Normal p-n diode, the depletion region width is more due to lightly dopped. When the diode is forward bias, those electrons have greater potential Energy than Barrier potential, those electrons only Jump from n-type to p-type material these are participated to flow of current.

* In Tunnel diode, the depletion region width is less due to heavily dopped. When the tunnel diode is forward bias, those electrons have greater potential Energy than the Barrier potential Energy those electrons are jumps from n-type to p-type material along with these electrons, those electrons have lower potential Energy than the Energy of Barrier potential, those electrons are also penetrate through the junction from n-type to p-type materials. these all electrons are participated to flow of current. This process is "Tunnelling of electrons". Tunnelling means "penetration of electrons through the barrier Eventhough the " Energy is less than the barrier potential.

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So, Quantum Mechanics Explains, when the depletion region width is less then electrons are easily penetrate through the junction (Depletion region) Even though the electrons are having less barrier potential than the Energy of barrier potential. Energy of

Characteristics :—

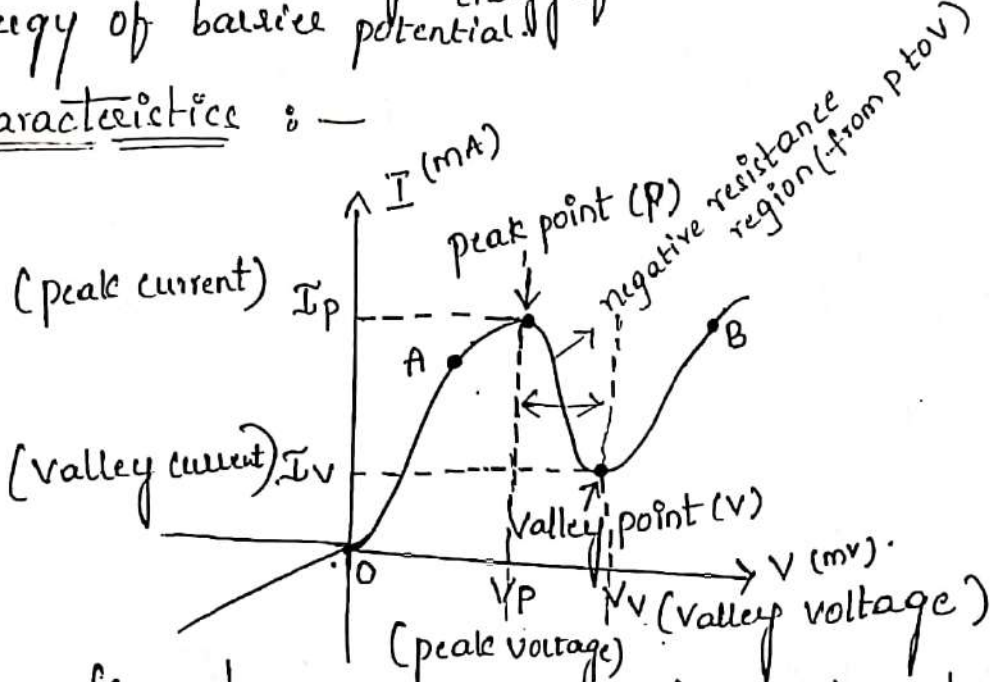

fig: characteristics (V-I) of Tunnel Diode (F·B)

* When the Tunnel diode is in forward bias the p-type material is connected to positive teminal an n-type material is connected to negative teminal of battery.
* Then the Tunnel diode is starts to conduct the ap voltage increases, the voltage across diode and current are increases exponentially and reached a point 'A' is shown in above figure.
* When applied voltage increases more than the curre also increases upto the point 'p' which is peak poi indicated as 'p' as shown above. The corresponding current and voltage is called as "peak current" (I_p) and "peak voltage". (V_p)
* If we further increase voltage greater than the peak volta the current will decreases upto the point 'v' which " "valley point". The corresponding current

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Case 2 :- When the bias is applied (-forward bias).

When the diode is in -forward bias, the voltage increases the gap between conduction and valence band is reduce then the flow of current will occur. Due to increment of voltage (F.B) the holes and electrons are recombine, and again bonds will breakup the free-electrons will occur. due to these free-electrons the current will flows throught the tunnel diode upto point A. as shown in characteristic of V & I

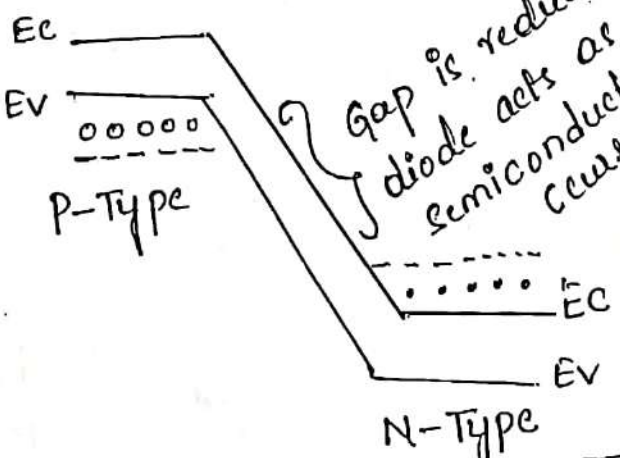

fig :- Forward bias of Tunnel diode [at point A].

Case 3 :- Further increment of Forward bias (voltage)

In this case, we are going increase the forward bias ie increases applied voltage further then the gap between conduction band and valence band is always equal (parallel) ie there is no gap between the conduction and valence bands of p-type and n-type materials. In this Very high amount of current will flows throught the diode. This current is called as "peak current" (Ip). This can be shown in characteristics curve of V-I of tunnel diode.

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and voltage is called as "valley current" (I_V) and the region between peak point and valley voltage (V_V). valley point is "negative resistance re

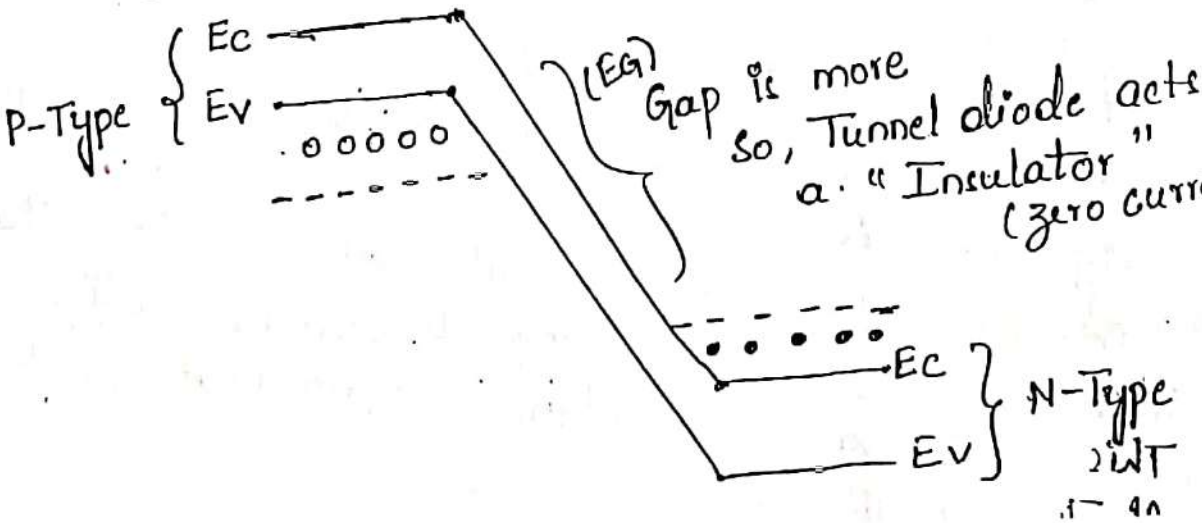
* Further increment of voltage (applied voltage) the dio again starts to conduct then this diode acts like a normal diode then the current increases from th valley point again when we are increase the applied volt

Tunnel diode Band Diagram :-

* By using Band diagram, try to understand what hap inside tunnel diode with the Energy band diagram. Co the Energy band diagram are going to Explain wha happens in the characteristics of Tunnel-diode.
* The characteristics of Tunnel diode is Explained by using Energy band diagram in different cases.

Case (i) :- No bias [point 0]

When No bias is applied to tunnel diode then th gap between the Conduction band and Valence band of p-type and n-type material is very high In this, total number of electrons and holes are equ then there is zero current occur i.e no current fl through the diode and voltage is also zero.



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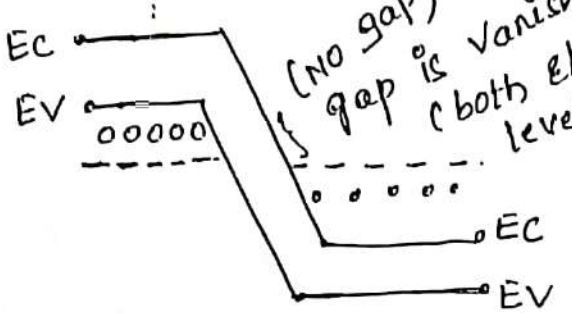

fig: forward bias (point 'p')

Case (4) :— Further increment of voltage in forward bias i.e voltage increases greater than the peak voltag which is greater than the peak voltage then the level of p and n-type materials are shifted and Exchange their positions, due to high increment of applied voltage, the Electrons level is cross the holes level in valence band of p-type material and Holes level is decreases than the Electrons level in Conduction band of n-type material. Then this case the current flow is decreases upto the point 'V' which is called as "valley point". The corresponding current is "valley current" and voltage is "valley voltage".

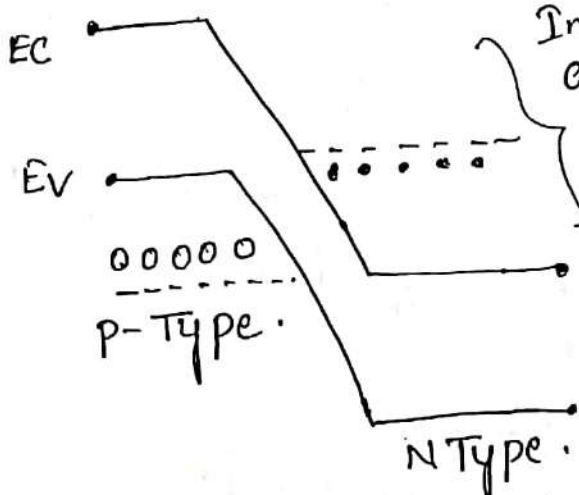

fig: forward bias (point V).

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Case 5 :-

* After decreasing the Current (valley current) ag
this valley current increases at point B cu
further increment of applied voltage. then the
diode will works as in normal forward bias, thi
case voltage increases then the current increa
reached at point 'B' shown in characteristic cu

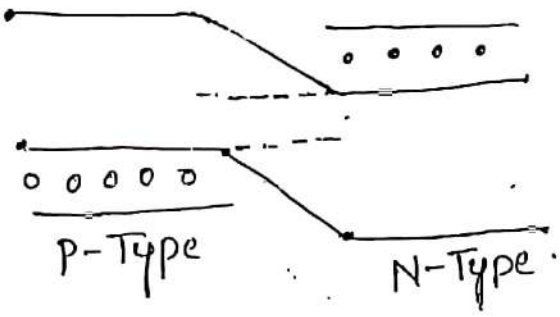

fig: forward bias (point - B)

Advantages :-

1. Low Noise
2. Ease of operation
3. High speed
4. Low power

Disadvantages :-

1. voltage range over which it can be operated is
2. Being two terminal device there is no isolation between two regions.

Applications :-

* Tunnel diode is used an ultra high speed switch
* As logic memory storage device
* As Amplifier
* As a Microwave oscillator
* In relaxation Oscillator circuits.

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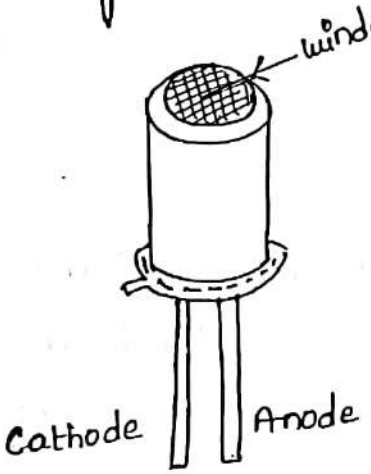
PHOTO-DIODE :—

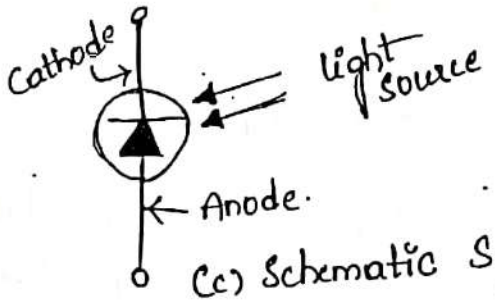
Definition :— A photo diode is a reverse biased silicon (or) Germanium pn junction in which reverse current increases when the junction is exposed to light.

The Reverse-current in a photo-diode is directly proportional to the intensity of light falling on its pn junction. This means at greater the intensity of light falling on the pn junction photo-diode, the greater will be the reverse current.

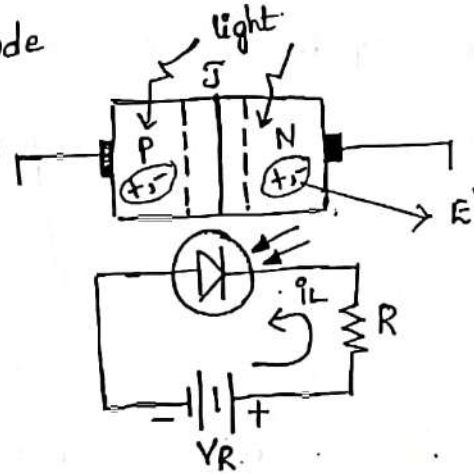
Photo diode package :— The figure (a) shows a typical photo-diode package. It consists of a pn junction mounted on an insulated substrate and sealed inside a metal case. A glass window is mounted on top of the case to allow light to enter and strike the pn junction. The two leads Extending from the case are labelled anode and cathode. The Cathode is typically identified by a tab Extending from the side of the case.



(a) package



(c) Schematic Symbol.



(b) principle of operation

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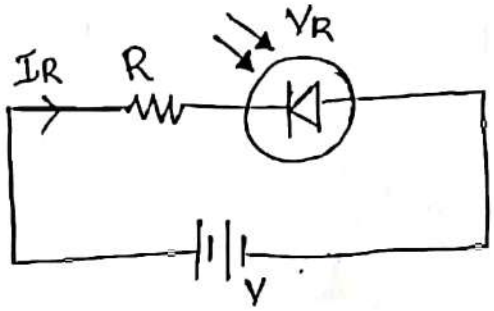
principle :—

The photodiode is connected in reverse biased condition. The Depletion region width is large. under normal condition it carries small reverse current due to minority charge carriers. when light is incident through glass window on p-n junction, photons in the light bombard the p-n junction and some energy is imparted to the valence electrons. Due to this, valence electrons are dislodged from the covalent bond and become free electrons. Thus more electron-hole pairs are generated. Thus total number of minority charge carriers increases and hence the reverse current increases. This is basic principle of operation of photodiode.

Operation :—



The above figure shows the basic photo-diode circuit. The circuit has reverse biased photo-diode, resistor R and dc supply. The operation of the photo diode is as under:

(i) When no light is incident on the p-n junction of photo diode the reverse current I_r is extremely small. This is called "dark current".

The resistance of photo diode with no incident light is called dark current resistance (R_R)

Dark-resistance of photo diode $R_R = \frac{V_R}{\text{Dark current}}$.

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Case (ii) :- When light is incident on the p-n junction of photo-diode, the reverse current, I_r is Extremely increases. i.e., there is a transfer of Enegy from the incident light (photons) to the atoms in the junctio This will Creates more free Electrons (and more holes). These additional free Electrons will increases the reve Current.

Case (iii) :- As the intensity of light increases, the reverse current I_R goes on increasing till it becomes maximu This is called "Saturation current".

Characteristics of photo-diode :-

1) Reverse Current illumination Curve :-

The fig (a) shows the graph between (I_R) and illumination (E) of a photo-diode. The reverse current is shown on the Vertical axis and is measured in μA. The illumination is indicated on the horizontal axis is measured in mW/cm². The graph is a straight line passing through the origin.

$\therefore \quad I_R = mE$

Where m = slope of the straight line.

m = Sensitivity of photo diode

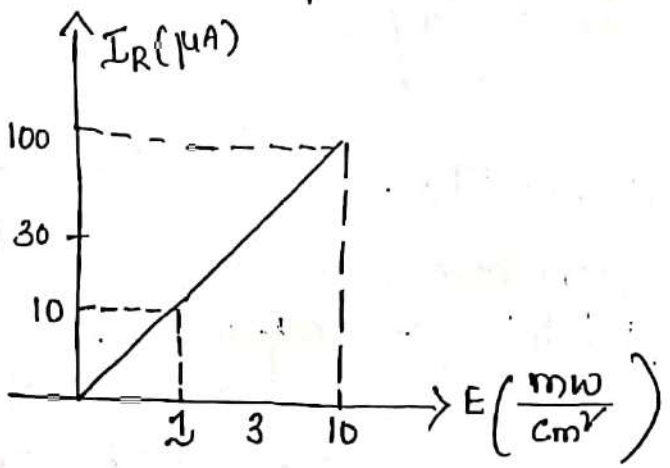

fig (a) Reverse Current - illumination curve.

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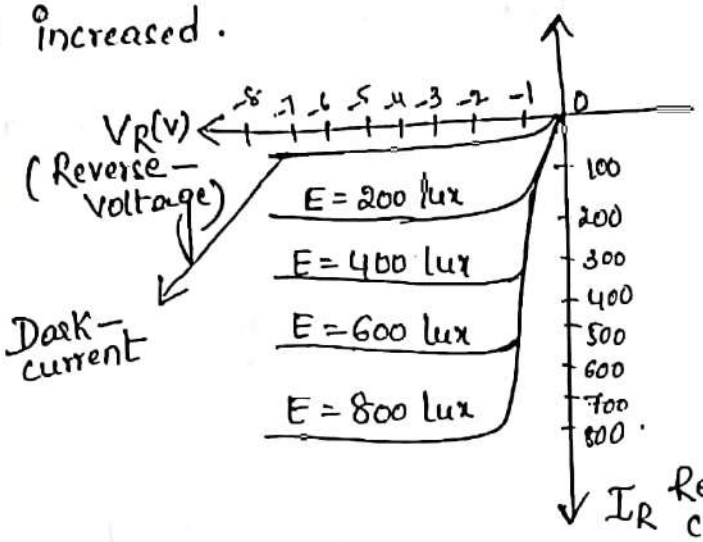
(ii) Reverse-voltage and Reverse Current Curve :-

It shows the graph between reverse current (I_R) and reverse voltage (V_R) for various illumination levels. It is clear that for given reverse-biased voltage V_R, the reverse current I_R increases, as the illumination (E) on the pn junction of ph... is increased.



fig(b) Reverse voltage (Vs) Reverse Current Curve.

Advantages :-

1. Can be used as Variable resistance device
2. Highly sensitive to the light
3. The speed of operation is very high. The Switching Current and hence the resistance value from high to low or otherwise is very fast.

Dis-advantages :-

1. The Dark Current I_λ is temperature dependent,
2. The Overall photodiode characteristics are temperature dependent hence have poor temperature stability.
3. The Current and change in Current is in the range of μA which may not be sufficient to drive other circuits. Hence amplification is necessary.

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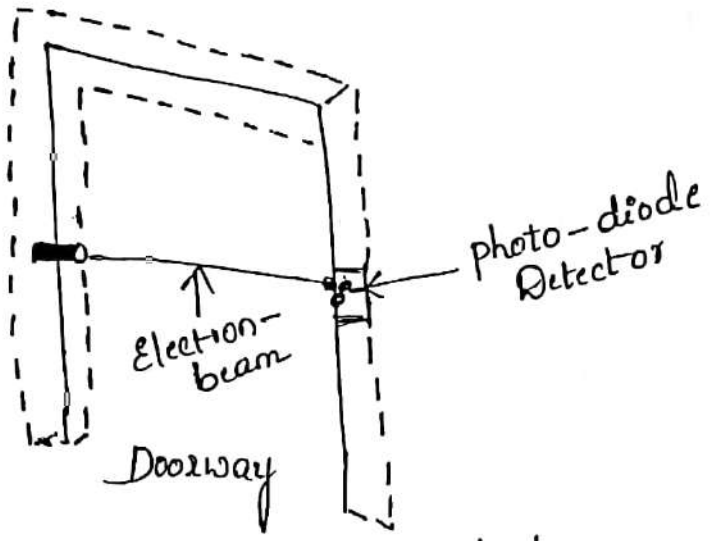
pplications :—

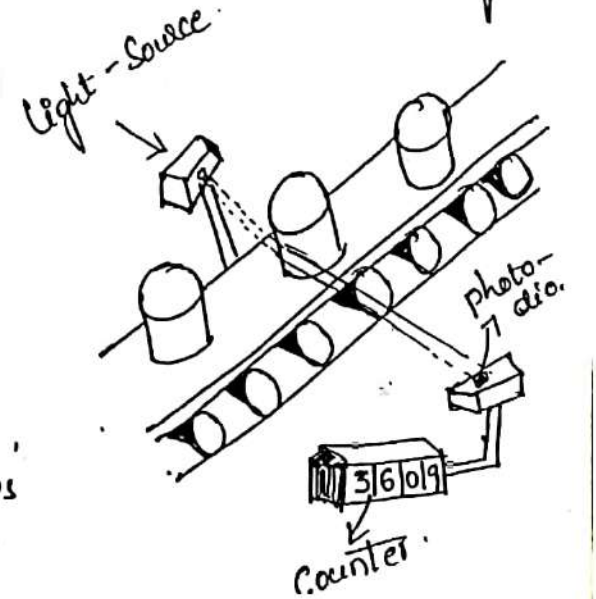
(i) Alarm Circuit using photo-diode :—

The figure shows the use of photo-diode in an alram system. Light from a light source is allowed to fall on a photo-diode fitted in the doorway. The reverse current I_R will continue to flow so long as the light beam is not broken. If a person passes through the door, light beam is broken and the reverse current drops to the dark current level. As a result, an alarm is sounded.



(ii) Counter Circuit using photo diodes :—

A photo diode may be used to count items on a conveyor belt. figure shows a photo diode circuit used in a system that counts objects as they pass by on a conveyor. In this circuit, a source of light sends a concentrated beam of light across a conveyor to a photo-diode. As the object passes, the light beam is broken, I_R drops to the dark current level and the



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Problems :—

1. A photo diode is Exposed to light with an illumination 2.5 mw/cm^2. If the sensitivity of the photo-diode for the given conditions is 37.4 μA/mw/cm^2. find the reverse current through the device ?

$$\text{Reverse Current} = \text{Sensitivity} \times \text{Illumination}$$

$$= m \times E$$

$$= 37.4 \times 2.5$$

$$I_R = 93.5\,\mu A$$

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VARACTOR DIODE :-

- What is Varactor diode
- Symbol
- Structure
- Working principle
- Characteristics
- Advantages and Disadvantages
- Applications

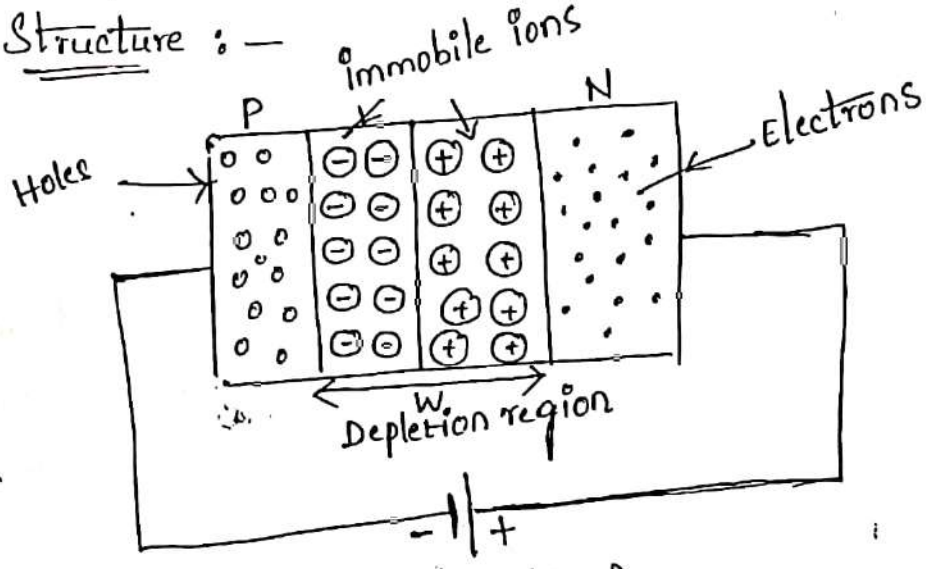
What is Varactor Diode :-

Varactor diode, also known as Variable Capacitor diode is a junction diode and its junction Capacitance (Transition Capacitance) can be varied Electrically (by changing voltage applied).

Symbol :-

Here, arrow '↗' indicates Variable (can vary the voltages, currents).
two parallel lines 'II' indicates Capacitor.

Structure :-



(Reverse bias)

fig :- Reverse biased P-N Junction diode

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When the Diode is reverse biased, a Depletion region formed as shown in figure. The larger the reverse bias applied across the diode, the width of the Depletion layer 'W' becomes wider. By decreasing the reverse bias voltage, the depletion region width W becomes Narrower. In this region, the depletion region acts like a insulator preventing Conduction between N and P layers of the diode, just like a "Di-Electric". The 'P' and 'N' layers acts like a plates of the Capacitor. The structure of P-N junction diode in reverse biased condition is just like a Capacitor. So it is called as Varactor (or) Vari-cap diode i.e Variable Capacitor Diode.

When the reverse biased voltage increases the width of Depletion layer increased and Capacitance becomes Smaller. The Capacitor C_T of a Varactor diode is Determined using the Equation,

$$C_T \propto \frac{A}{W_d}$$

$$\left(C_T = \frac{\varepsilon A}{W} \right)$$

Where ε = permitivity of Semiconductor material

A = Area of Cross-Section of the junction

W = width of the Depletion region

The width of the Depletion region increases, when the reverse bias voltage is increases.

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.e width increases the distance between the parallel of plates of the capacitor increases.

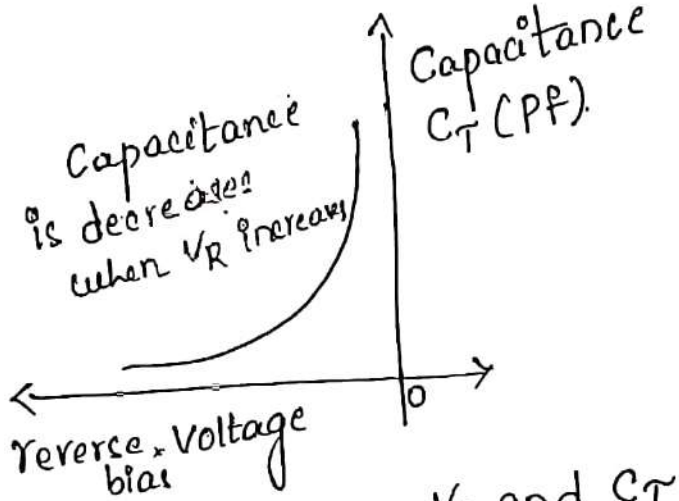
$$C_T \propto \frac{1}{W}$$

The width of Depletion region increases, the Transition Capacitance is decreases.

. Transition Capacitance Vary inversly with the reverse voltage (C_T).

∴ Varactor diode is a "Variable Capacitor" diode.

haracteristics :—



g :—

The characteristics between V_R and C_T.

from the above figure, the capacitance is inversely proportional to the reverse bias voltage.

i.e $C_T \propto \frac{1}{V_R}$

i.e width is increases when the reverse bias voltage increases

$C_T \propto \frac{1}{W} \longrightarrow (1)$

$V_T \propto W$

$W \propto V_T \longrightarrow (2)$

width increases, Capacitor will decreases

$C_T \propto \frac{1}{W}$.

from (1) & (2). $\left(C_T \propto \frac{1}{V_R}\right)$

totally V_R increases, C_T decreases and viceversa.

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Advantages :-

- Varactor diode has Low noise - it generates less noise as compared to other p-N Junction diode
- It is portable due to the small size
- Lightweight and more reliable
- Low - cost

Disadvantages :-

* These are specially designed only to the work in the reverse biased mode, thus it possesses the least significance when operated in forward biasing.

Applications :-

* FM radio and Tv receivers
* Self - adjusting bridge circuits
* Adjustable bandpass filters
* Tuning of LC resonant circuits in microwave multipliers.
* Very Low noise microwave parametric amplifier

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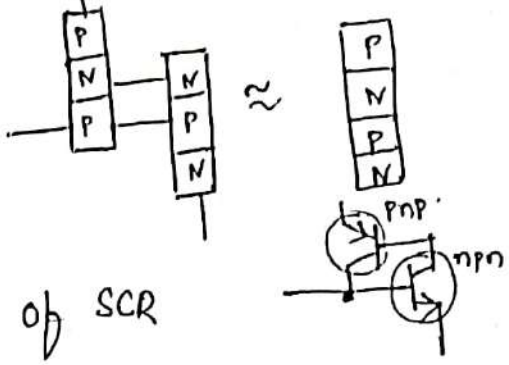
Silicon Control Rectifier :— (Controlled rectifier (or) Thyristor)

- Meaning of SCR
- Symbol of SCR
- Construction of SCR
- Working/operation of SCR
- Characteristics of SCR
- Advantages & Disadvantages of SCR
- Applications



Meaning of SCR :- SCR is an unidirectional device like diode. it allows to flow current in only one direction. SCR has a built in feature to Switch "ON" and "OFF". SCR is abreuated as "Silicon Controlled Rectifier".

Symbol :-

Diodes turned as uncontrolled rectifiers as they conduct whenever anode vtg (i/p) is greater than cathode but in SCR - doesn't conduct even though Anode vtg > cathode vtg unless the gate is triggered.

By providing triggering pulse then control operation.

Construction :-

The SCR is a four layer p-n-p-n device where p and n layers are alternately arranged.

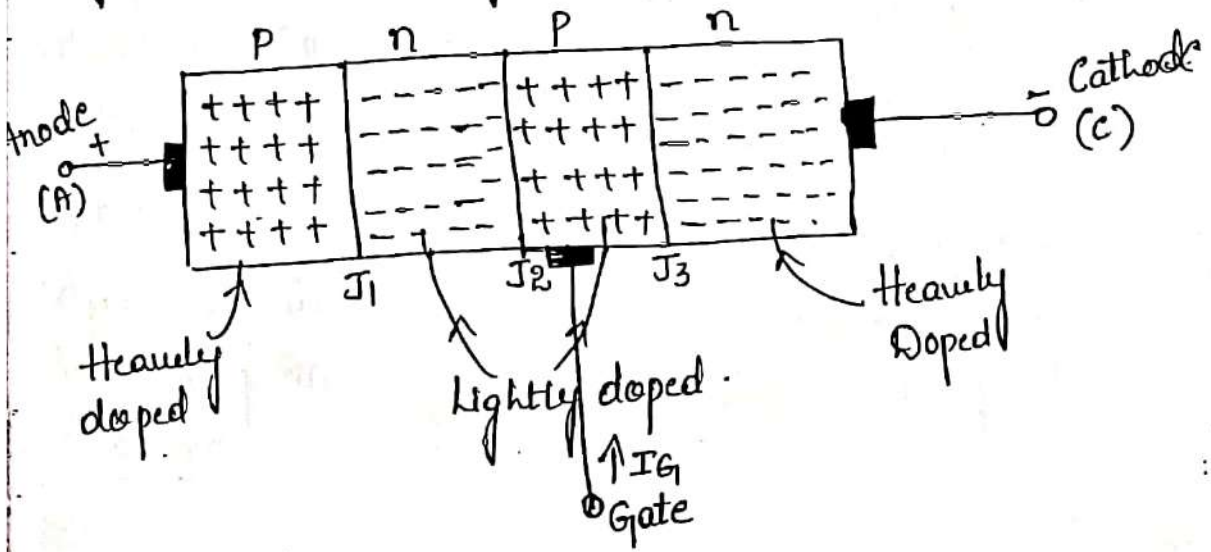


fig :- physical Structure of SCR

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* The outer layers are heavily doped. There are three p-N junctions called J_1, J_2, J_3. The outer p-layer is called "Anode".
* While outer n-layer is called "cathode". Middle p la is called "Gate".
* Anode must be positive with respect to Cathode to forward bias. The SCR but this is not sufficient to turn ON SCR. Current must be passed through the terminal, Thus it is a Current operated device.

Operation of SCR :—

* The operation of SCR is divided into two categori

When Gate is open :—

Case (1) :— Consider that the anode is positive with re to Cathode and gate is open. The Junction J_1 forward bias & J_3 is also in forward bias and Junction J_2 is Reverse biased

$J_1, J_3 \longrightarrow$ forward bias

$J_2 \longrightarrow$ Reverse bias

There is a Depletion region around J_2 and onl leakage current flows which is negligibly sm practically SCR said to be "off". This is calle the "forward blocking state" of SCR.

The voltage applied to anode and cathe with anode is positive, cathode is negat The positive voltage is called as "forward voltage"

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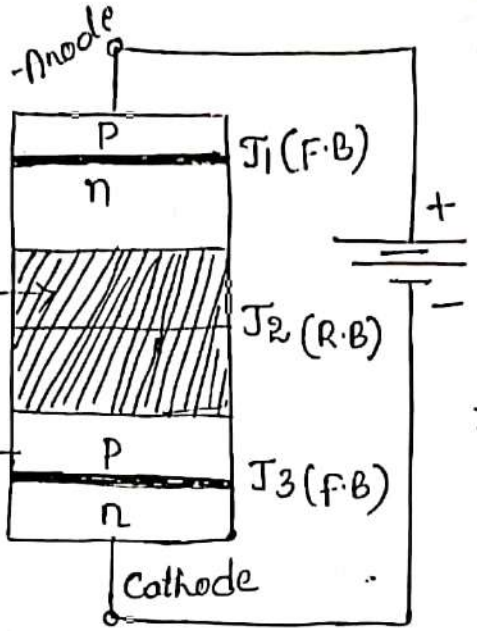
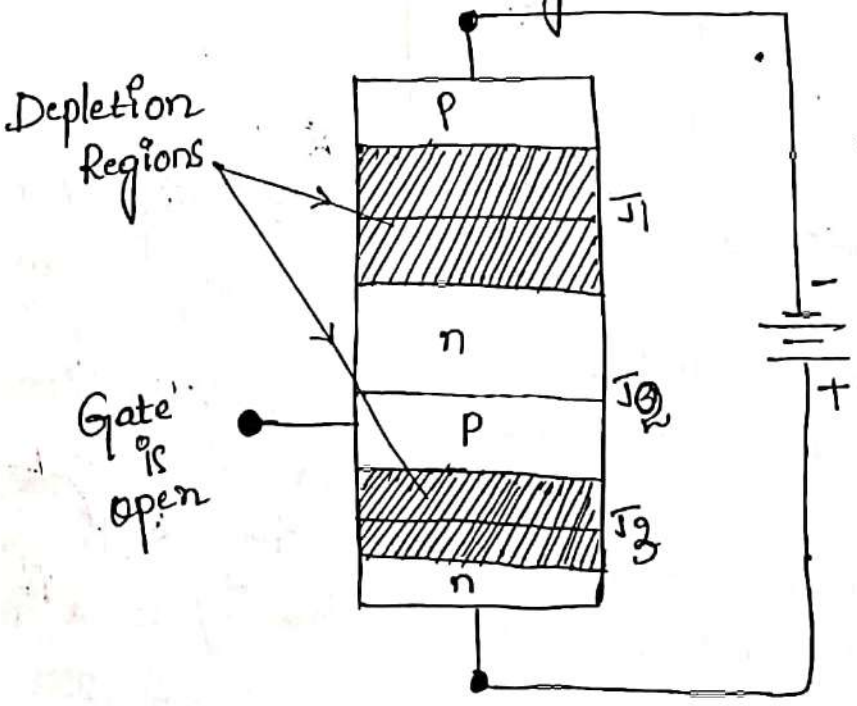


J1, J3 are forward bias
J2 is Reverse bias

se (2) :-

With gate open, if cathode is made positive with pect to anode, the junction J1, J3 becomes the reverset ised and J2 forward biased. The Current flowing is akage Current, which can be neglected (flowing small amount of current). it is very small. The voltage applied to make thode positive is called "Reverse voltage" and SCR is said nly be in "Reverse blocking State".



J1, J3 are Reverse biased
J2 is forward-biased.

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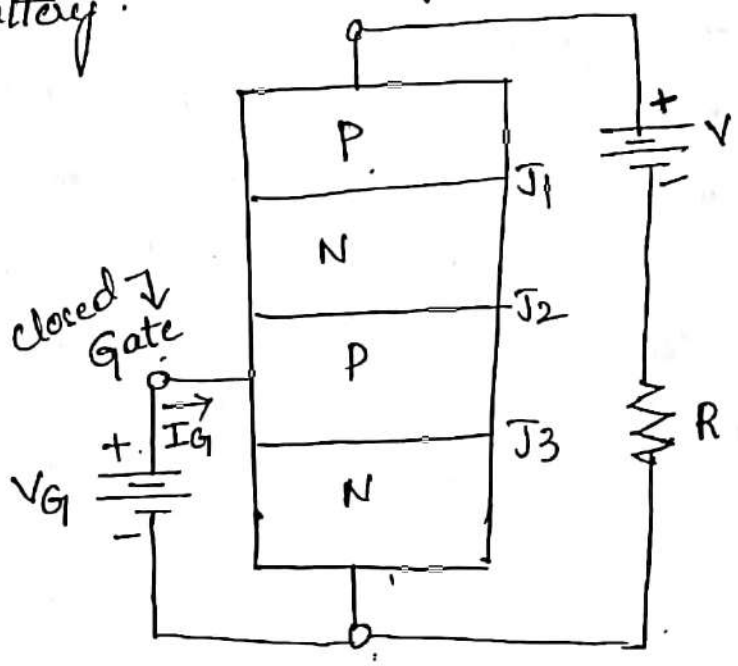
* In forward blocking state, if the forward voltage is increased, the current remains almost zero upto certain limit. At a particular value the reverse biased Junction J_2 breaks down and SCR conducts heavily. This voltage is called "forward breakover" V_{BO} of SCR. In such case SCR is said to be 'ON' or triggered.

2) When Gate is closed :—

* Consider that the voltage is applied between gate and Cathode when the SCR is in forward blocking state. The Gate is made positive with respect to the Cathode. The Electrons from n-type cathode which are majority in number, cross the junction J_3 to reach to positive of battery.



* While holes from p-type move towards the negative battery. This constitutes the gate current. This current increases the anode current as some of the electrons cross junction J_2 as anode current increases more electrons cross the junction J_2 and the anode current increases. Due to the regenerative action, within short time, the Junction J_2 breaks and SCR conducts heavily.

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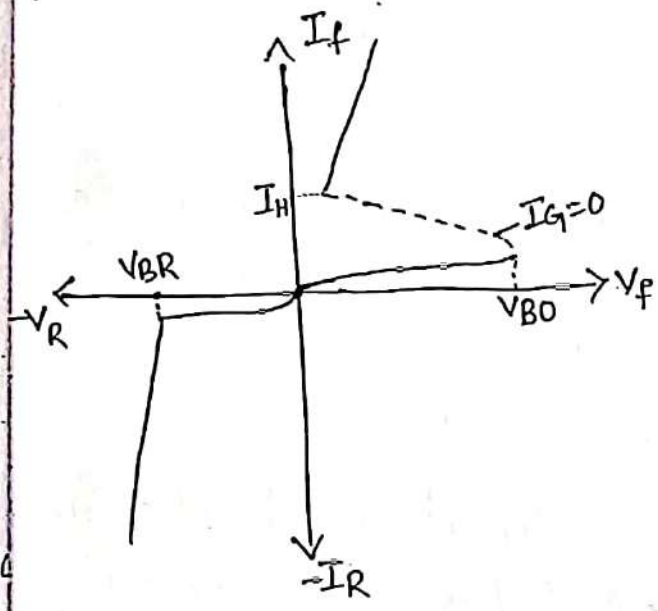
haracteristics :—

When a small positive voltage is applied to gate and anode is connected to positive terminal of the supply as on. The junction J_3 is forward biased, junction J_2 is reverse sed. The electrons from N_2 layer starts moving across junction J_3 where as the holes from P_2 layer cross nction J_3. As a result the gate current starts flowing hich increases the anode current.

The increased anode current make more electrons available at junction J_2. This process continues and junction J_2 breakdown and the SCR starts conducting.

Note that the anode voltage required for conduction when gate is positive is less than the breakover voltage.



g: characteristics of SCR

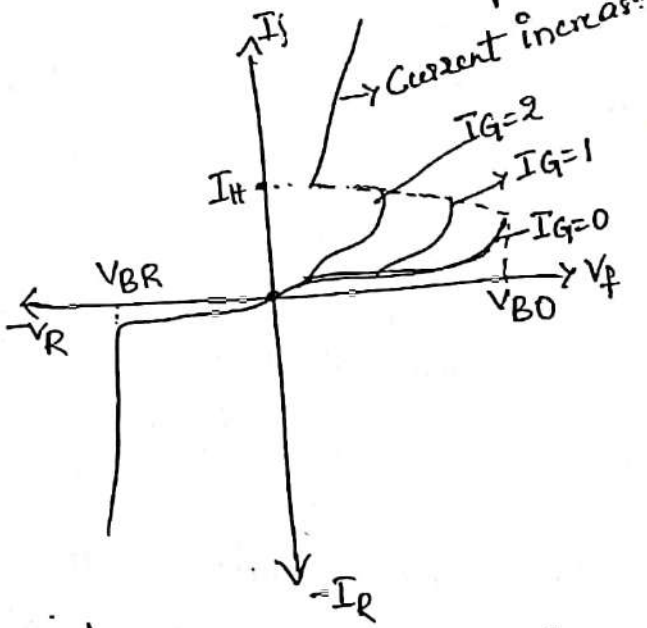


fig: Characteristics of SCR for different values of I_G.

When anode is negative with respect to cathode, the ve between V and I is known as reverse characteristics. hen reverse voltage is applied to SCR the current through he SCR is very small (leakage current).

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When reverse voltage increased gradually a stage reached at which the avalanche breakdown occurs and SCR starts Conducting heavily. Then the voltage is called reverse breakdown voltage. The characteristics as shown above figure.

Break over voltage :- (V_{BO})

It is defined as the voltage at which the SCR enters the Conduction region.

Holding Current (I_H) :-

This is the value of anode current below which SCR Switches from ON state to OFF state.

forward blocking region :-

The region corresponds to OFF condition of SCR when anode is positive with respect to Cathode.

Reverse blocking region :-

The region Corresponds to OFF Condition of the SCR when anode is negative with respect to Cathode.

Reverse Breakdown voltage :-

The reverse voltage at which the device breaks into the avalanche region is called "Reverse breakdown voltage"

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dvantages :—

* Simple turn on latching device, (Easy to turn ON)
* Turn ON gain is very high
* Low cost
* High voltage and High current device
* It is simple to control dc power (donot able to control AC power easily) → not simple

sadvantages :—

* In Ac circuit, it needs to be turned ON each cycle.
* The gate current Cannot be negative
* It cannot be used at higher frequencies.

pplications :—

* Relay control (ON/OFF)
* Heater Control
* Battery chargers
* Inverters
* Regulated power Supplies

Note :—

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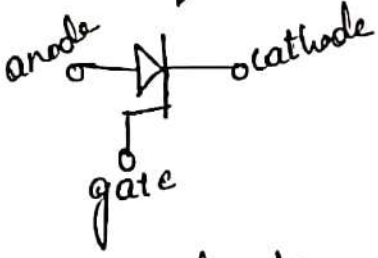
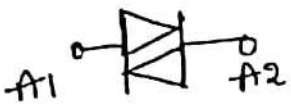
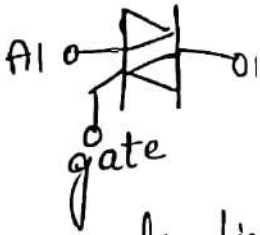
Comparison :—

Comparison between SCR, DIAC, TRIAC :—

Parameter	SCR (Silicon-Controlled Rectifier)	DIAC (Diode for AC)	TRIAC (Triode for
Full form	Silicon-Controlled Rectifier	Diode for Alternating-Current	Triode fo Alternati Current
Symbol			
Direction of current	Only unidirection	Bi-direction	Bi-directio
Controlled	Controlled device	un-Controlled device	Controlled device
power	High	low	high
Applications	Inverters, Chopper, 3-phase rectifiers	Trigger-circuits	fan contr light dir

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AC :—

Meaning of DIAC & use of DIAC
Symbol
Construction
operation
characteristics
Advantages & Disadvantages
Applications

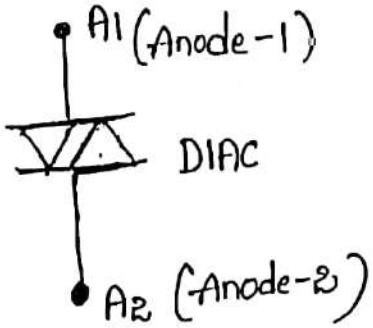
aning of DIAC :— DIAC is abrevated as "Diode-for-
— Alternating Current".

DIAC is a device which has two electrodes. It is a member of the thyristor family.

e :— The advantage of using this device is that it can be turned on or off simply by reducing the voltage level below its avalanche breakdown voltage.

* It is mainly used in triggering of thyristor.

mbol :—



The figure shows a Symbol of DIAC which resembles Connection of two diodes in Series. Also it can be lled as "transistor" without "Base".

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Construction of DIAC :—

It is a Device which consists of four layers and t
terminals. The Construction is almost same as transistor
but there are certain points which deviate from the Constr
from the transistor.

* There is no base terminal in the DIAC.
* The three regions have almost the same level of d

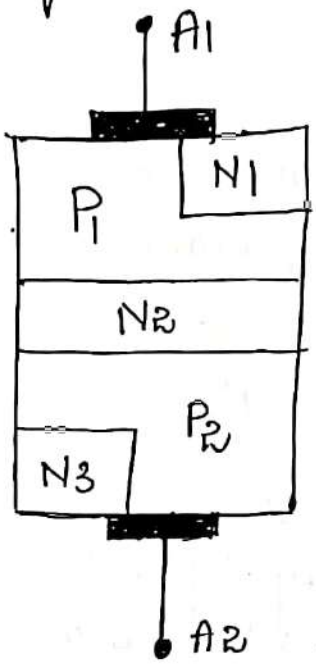

fig: Construction of DIAC

Operation :— from the figure, we see that it has tw
P-type material and three n-type materials. Also it do
ave any gate terminal in it.

ase(i)
* The DIAC can be turned on for both the polarity of
voltages. when A2 is more positive with respect to
A1 then current does not flows through the Correspond
N3-layer but flows from P2-N2-P1-N1.

Through these layers only Current will flows
N3 layer does't involves during this Operation of
flow of Current.

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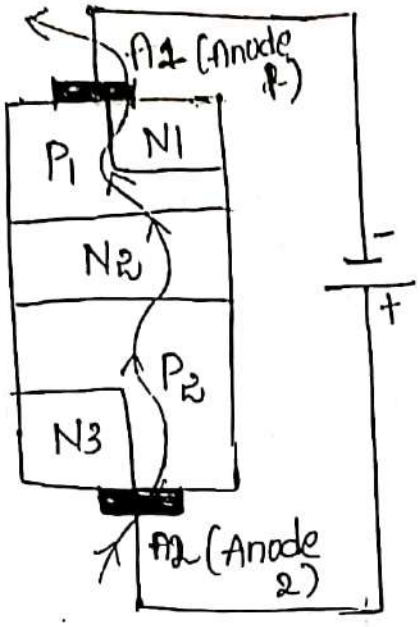
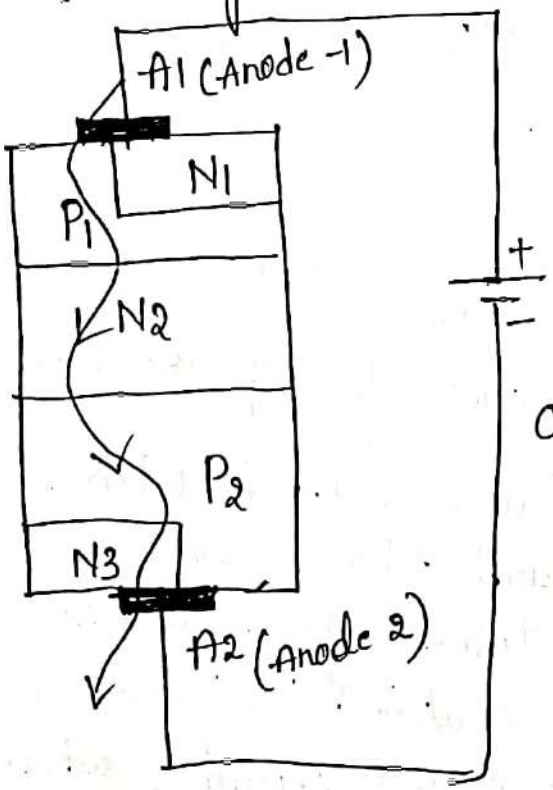


Current flows through the layers of

$P_2 \rightarrow N_2 \rightarrow P_1 \rightarrow N_1$

g :- A_2 is more positive than A_1 (i.e A_1 = negative, A_2 = positive).

e (ii) :- When A_1 is more positive than A_2 i.e A_2 is gative, A_1 is positive, Current does not flows through Corresponding N_1 layer but flows from $P_1 - N_2 - P_2 - N_3$ rough these layers Only Current will flows, N_1 layer esn't involves during the operation.



Current flows through the layer of

$P_1 \rightarrow N_2 \rightarrow P_2 \rightarrow N_3$.

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The Construction resemble the diode Connected in when applied voltage is small in Either polarity, a small current flows which is known as leakage Current because of drift of Electrons and holes in the depletion region. Although a small Current flows, but it is not Sufficient enough to produce avalanche breakdown so the device remains in the non-Conducting state.

Characteristics :—

When the applied voltage in Either polarity Exceeds breakdown voltage, diac Current rises and the device Conducts in accordance with its V-I characteristics.

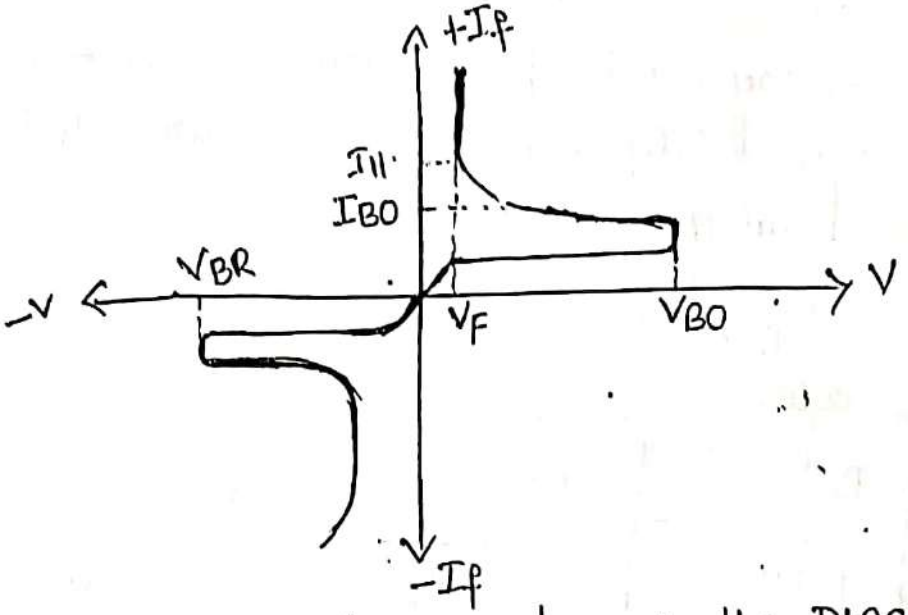

fig: V-I characteristics of the DIAC

* The DIAC acts as a Open Circuit when the voltage is less than its avalanche breakdown voltage. When the device has to be turned off, the voltage must be reduced below its avalanche breakdown voltage
* The DIAC acts as closed Circuit, when the voltage is applied to DIAC, small Current flows if we increases the voltage, the voltage start

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decreasing, further increment of voltage suddenly is current increases at particular a voltage.

Advantages :—

Does not Switch sharply at a low voltage condition at a low current level done by SCR or TRIAC.

At a to It has ON state voltage drop until its current falls below the holding level.

voltage drop increases, Current is increases.

Disadvantages :—

The main disadvantage of using DIAC is that it needs least 30V across it to break over. So the magnitude the level of incoming mains needs to be at least +/- 30V minimum before the triac can be triggered. So there is no by this dimmer can put out 100% voltage to the load and also - no control (not we gate terminal) here like a TRIAC

Applications :—

It can be used in the lamp dimmer circuit

used in heat control circuit.

Speed Control of a universal motor

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RIAC :—

- Meaning of TRIAC
- Use of TRIAC
- Symbol
- Equivalent circuit of TRIAC
- Operation of TRIAC
- characteristics of TRIAC
- Different modes of conduction
- Advantages & Disadvantages
- Applications of TRIAC

eaning of TRIAC :—

TRIAC is abreviated as "TRIODE for Alternating Current" (or) "TRIODE A·C Switch". TRIODE is advanced version of DIODE In Diode once it is in forward bias it will conducts, but in TRIODE by having control signal the conduction will happen based on triggering of control signal which is "Gate".

TRIODE is having 3-terminals – Anode 1 (or) MT_1
Anode 2 (or) MT_2
Gate

* Gate is a control terminal

se of TRIAC :—

* TRIAC is a bilateral device because it can operates in both the biasing conditions (or) both the directions.
unlike SCR we can trigger in both of the directions (both forward and reverse biasing conditions).
It is the main advantage and difference than SCR.

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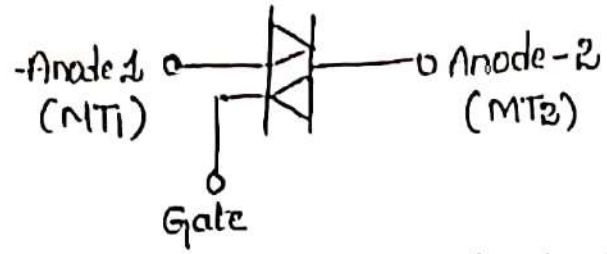
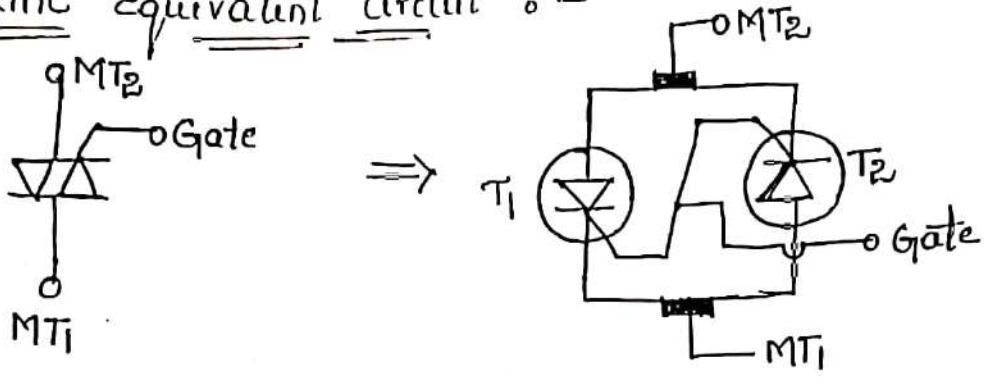
Symbol :-



* Two-SCR's are back to back connected and a "Com
-taminal for both the SCR's is Gate which is a Cont

TRIAC Equivalent circuit :-



Basic structure of TRIAC is,

* Two SCR's are back to back connected then it can
structured as follows

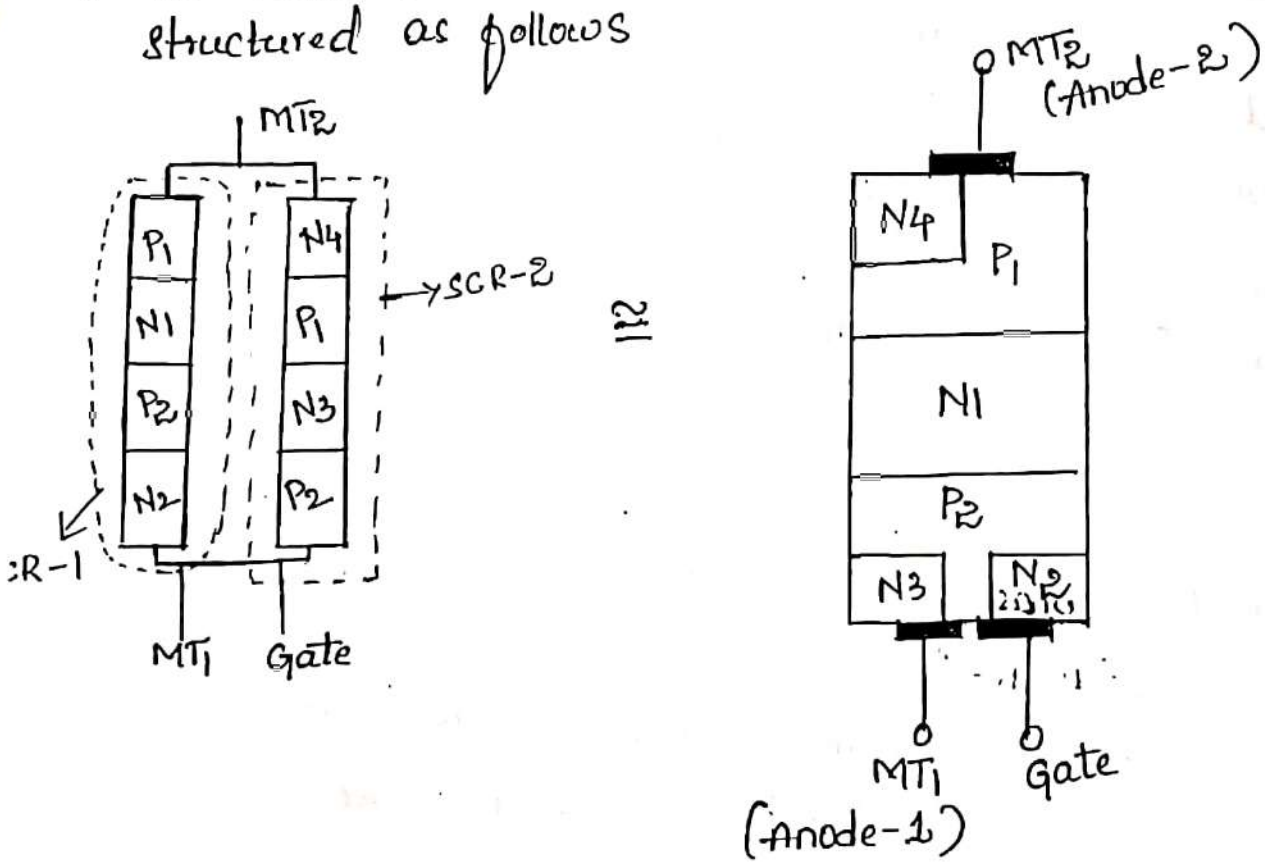


fig :- Basic Structure of TRIAC

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Operation :-

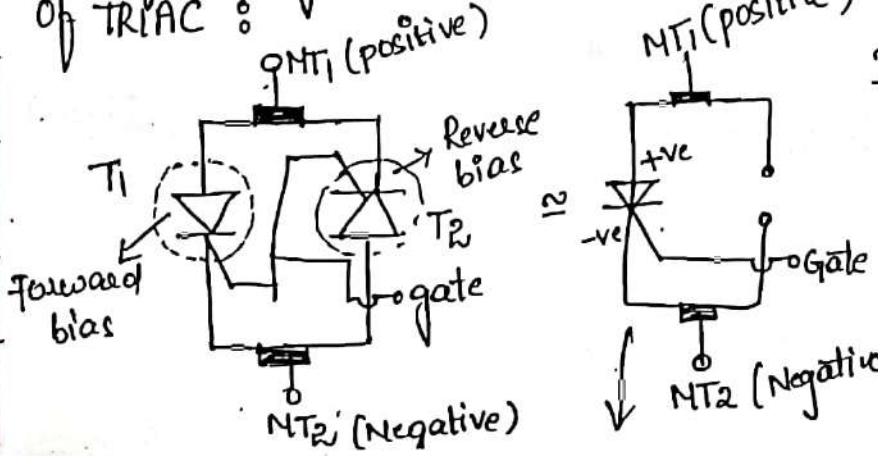
During the positive half cycle MT_1 is positive with respect to MT_2, where as MT_2 is positive with respect to MT_1 during negative half cycle.

When MT_1 is positive, MT_2 is negative - T_1 SCR is acts as a forward bias, T_2 - SCR is acts as reverse bias Then due to forward bias of T_1 - SCR, it will conducts then the operation of these T_1 is same as Silicon-controlled Rectifier (SCR) - forward bias. Then the characteristics curve will appear at the forward bias condition of SCR which is same as forward characteristics of SCR.

Next case, we consider MT_1 is negative, MT_2 is positive then T_1 - SCR acts as Reverse bias, T_2 - SCR acts as forward bias, this SCR is same as SCR operation but it's characteristic curve will represent on reverse bias characteristic on the graph because of using a controller of gate it will control the operation of SCR and it works as both the direction.

The characteristic curve represents on reverse-bias side.

The following circuit connections are shows the operation of TRIAC :



In this case

T_1 = Forward bias

T_2 = Reverse bias

∴ SCR - T_1 acts as same operation of SCR forward bias

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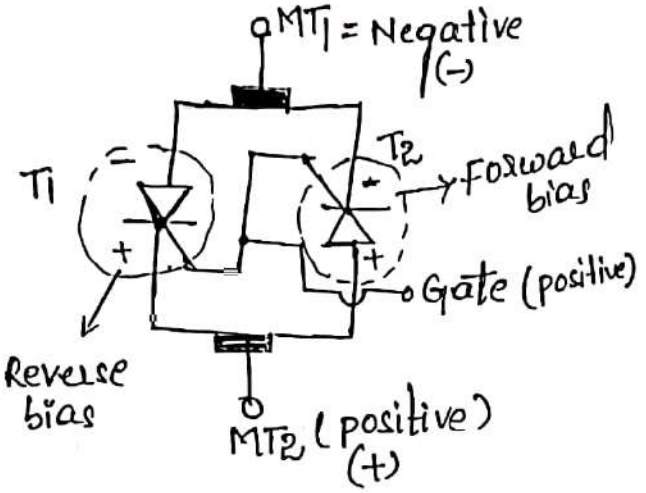
case-2 :- MT_1 = Negative , MT_2 = positive

In this case T_1 - Reverse bias
T_2 - Forward bias (same as SCR, represents curve reverse of



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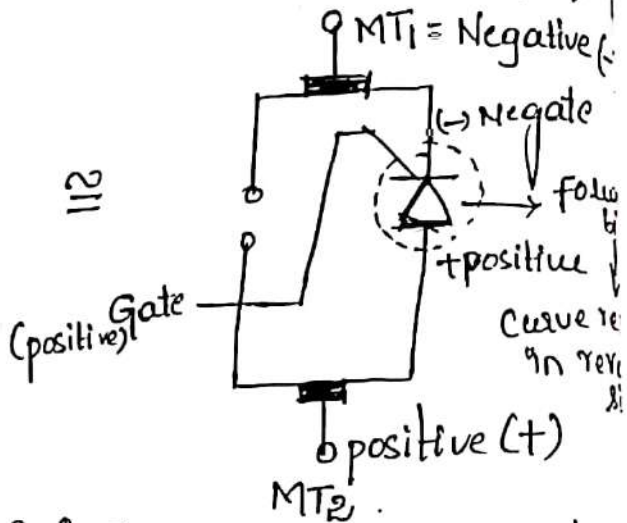

Characteristics of TRIODE AC :-

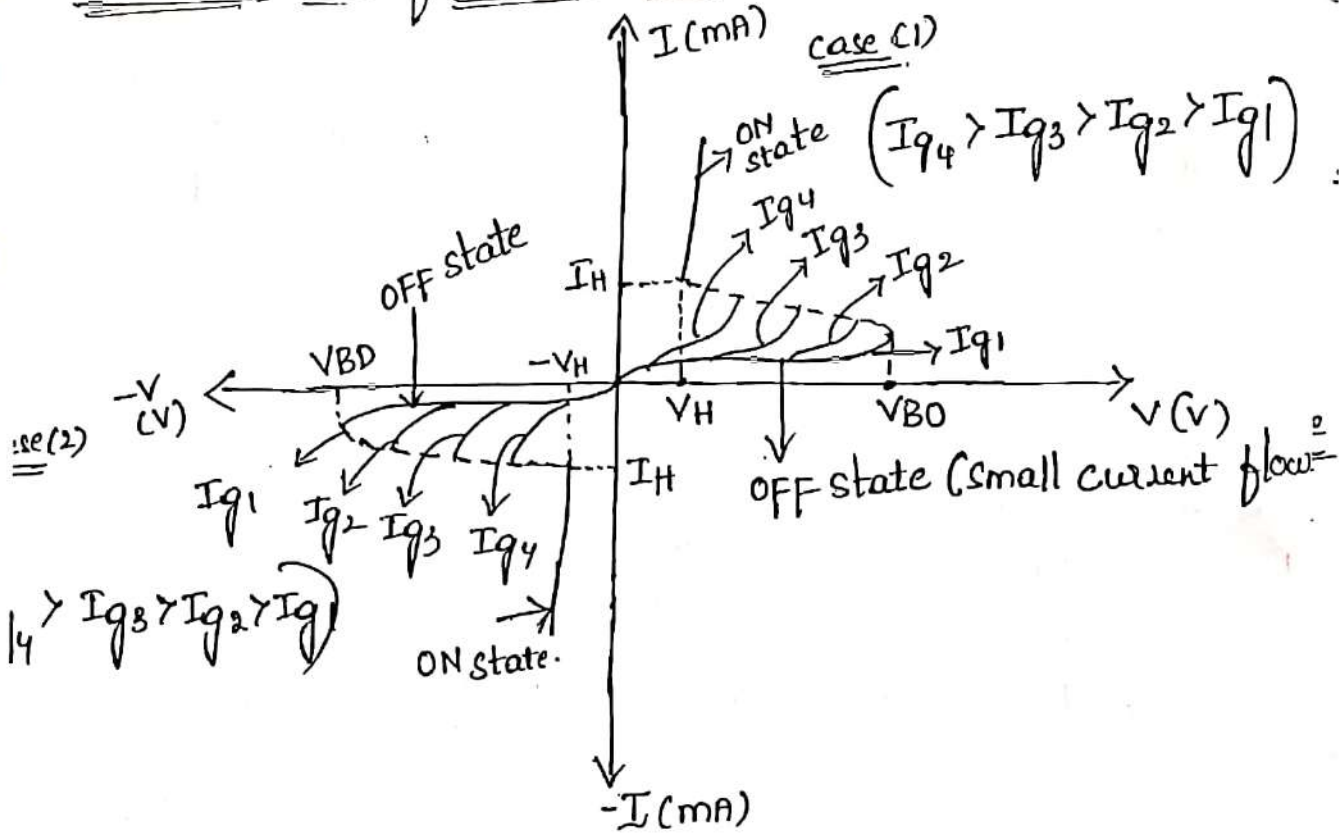

fig :- characteristics of TRIAC (TRIODE AC Switch)

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e 1 :- When the anode terminal of SCR (MT_1) is connected to positive terminal and MT_2 is connected to negative terminal of the battery. The Junction J_1 and J_3 forward bias, Junction J_2 is reverse bias. Hence no current flows through SCR but a small amount of current flows which is "Leakage current" practically. This state is cut-off state (or) cut off region.

* When the anode MT_1 voltage increased a stage is reached when the junction J_2 breakdown and T_1-SCR switches to a highly conducting state so the amount current increases sharply.
* This process will repeated for greater (or) increasing the Gate voltage. Then the gate current also increases.
* In the characteristics of TRIAC, different curves are obtained for different values of Gate currents which is always.... $I_{g4} > I_{g3} > I_{g2} > I_{g1}$

e 2 :- When the terminal MT_1 is negative
MT_2 is positive

In this case, the operation of SCR is same as case 1 but the curve will represents on reverse biase. conditive. Here T_1 SCR is reverse biased, T_2 SCR is forward biased. Same process will follows by increasing gate voltage we can get the different values for each value of gate voltages & gate currents.
i.e here also the condition is

$\cdots\cdots I_{g4} > I_{g3} > I_{g2} > I_{g1}$

* at a particular voltage current will sharply decreases here. The curve shown in figure as

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Break over voltage (V_{BO}) :-

It is Defined as, the voltage at which the SCR Enters the Conduction region.

Holding current (I_H) :-

This is the value of anode Current below which the SCR Switches from ON state to OFF state.

Forward blocking region :-

The region Corresponds to OFF Condition of SCR when anode is positive with respect to Cathode.

Reverse blocking region :-

The Region Corresponds to OFF Condition of the SCR when anode is negative with respect to cathode.

Reverse breakdown voltage :-

The reverse voltage at which the device breaks in the avalanche region is called "Reverse breakdown voltage".

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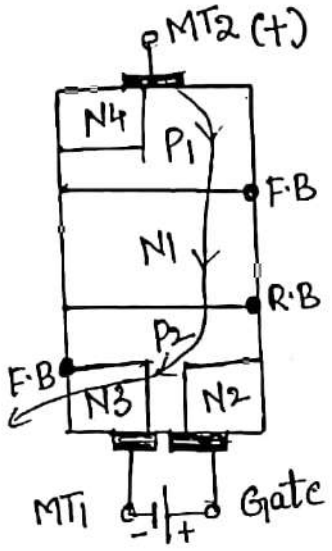
Different modes of Conduction in TRIAC :-

The four - different modes of TRIAC are considered are :

Mode :- Gate is positive, MT_2 - positive, MT_1 - Negative

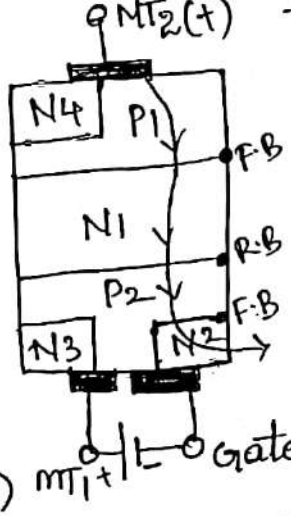


current flows through the layers are from

$MT_2 \rightarrow P_1 - N_1 - P_2 - N_3$

These layers are conducting layers due to connection s of three teminals.

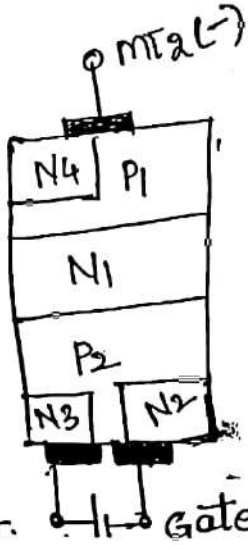
Mode :- In this case MT_2 = positive, MT_1 = positive Gate = Negative.



The current will flows through the layers are

$MT_2 \rightarrow P_1 - N_1 - P_2 - N_2$

Mode :- MT_1 = positive MT_2 = Negative Gate = Negative



In this case the current will flows through the layers are

$MT_1 \rightarrow P_2 - N_1 - P_1 - N_4$

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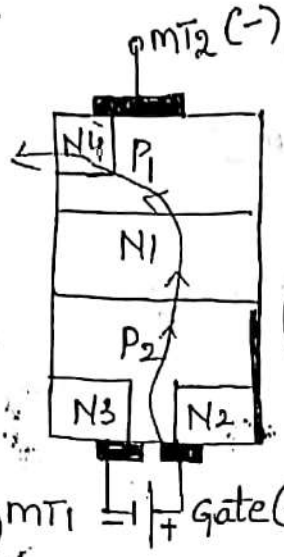
4th mode :-



MT_1 = Negative
MT_2 = Negative
Gate = positive

Then the current will flows

(Gate → P_2 → N_1 → P_1 → N_4)

1st mode

MT_1 = + (positive)
Gate = + (positive)

represents the characteristic curve in I-Quadrant

↓

Represents forward bias characteristics in Ist Quadrant

(operation is same as forward-SCR)

2nd mode

MT_1 = +ve
Gate = -ve

↓

II-Quadrant

⇓

Neglect

3rd mode

MT_1 = -ve
Gate = -ve

↓

III-Quadrant

↓

represents the reverse-bias characteristic's of SCR in TRIAC.

(here also operation same as forward SC but direction of cu

4th mo

MT_1 = -

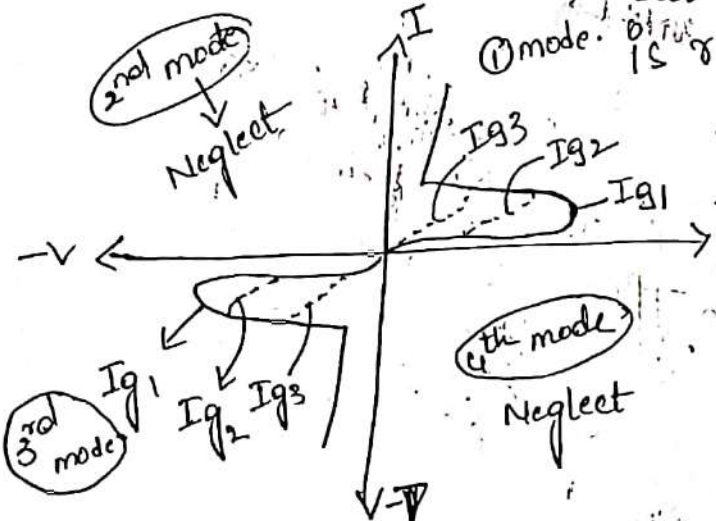
MT_2 = +

IV Q

⇓

Neg

① mode. is reverse of forwa SC



Characteristics of TRIAC using Different mode

dvantages :-

* TRIAC turns off when the voltage is reduced to zero.
* Single gate controls conduction in both directions.
* Triac with high voltage, currents ratings are available
* TRIAC is a Bi-directional device, it conducts in both direction.

disadvantages :-

* Gate has no control over conduction once, TRIAC is turned ON as in the case of SCR.
* TRIAC has very high switching delay
* TRIAC is not suitable for DC power applications.

pplications :-

* Used in Lamps control (Light dimmers)
* Speed controls of fans
* choppers design
* AC phase control (switching phase control)
* These are used in both into AC and DC circuits however the original design was to replace the utilization of two SCR's in AC circuits.

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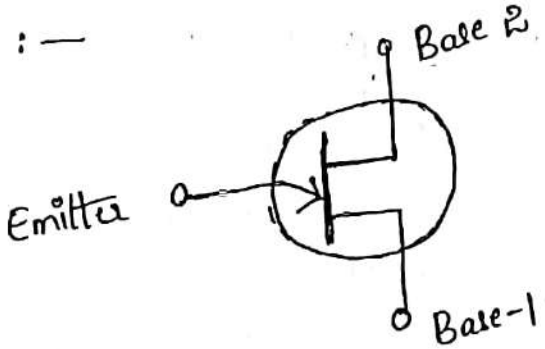
UJT :- (Uni-Junction Transistor)

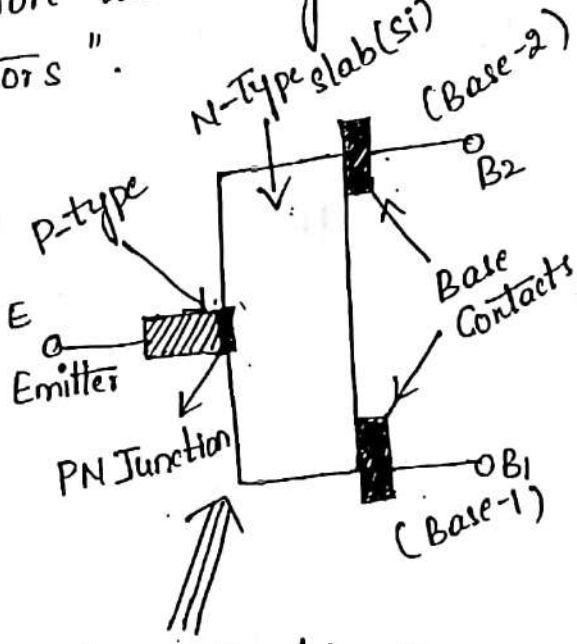
Meaning of UJT
Symbol
Construction / Structure
Working / Operation of UJT
Characteristics of UJT
Advantages & Disadvanges
Applications

Meaning of UJT :-

UJT is abrevated as "Uni-Junction Transistor".
It is a three terminal device semiconductor Switching device. It has only one PN Junction thats way it called as a "Uni-Junction Transistors".

Symbol :-





Structure :-

The Basic Structure of UJT is shown in figure.

* It Consists of lightly doped N-Type Silicon bar with heavily doped p-type material diffused to its one side closer to B2 for producing single PN Junction. BUJT has 3 terminals are Emitter, Base 1, Base-2 (Here the Emitter leg is [illegible] and arrow indicates the

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Equivalent Circuit :-

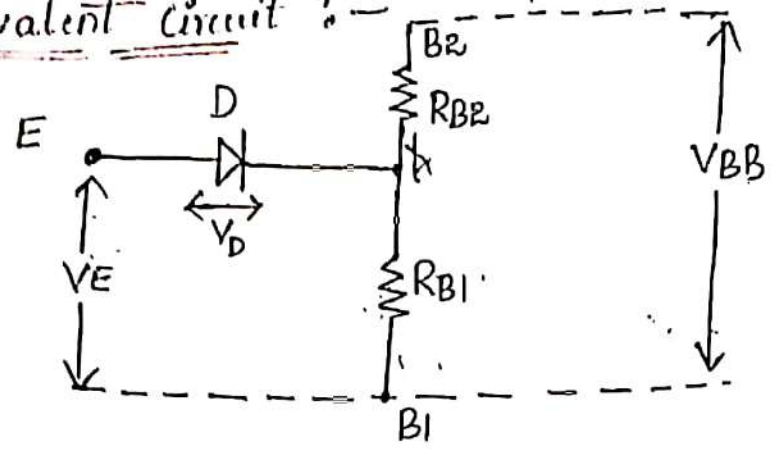

fig :- Equivalent Circuit of UJT

from the figure shown above inter base resistances B_2 and B_1 of silicon bar is given by

$$R_{BB} = R_{B1} + R_{B2}$$

If V_{BB} is applied between two Bases, with Emitter o Voltage gradient is established along the silicon N bar

The voltage across R_{B1} is given by

$$V_A = \frac{R_{B1} \cdot V_{BB}}{R_{B1} + R_{B2}} \simeq \left(\frac{R_{B1}}{R_{B1} + R_{B2}}\right) \cdot V_{BB}$$

Where,

$$\therefore \quad V_A = \eta V_{BB} \qquad \eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

η — is the Intrinsic Standoff ratio

$$\left(\eta = \frac{R_{B1}}{R_{B2} + R_{B1}}\right)$$

Typical value of η ranges from 0.56 to 0.75.

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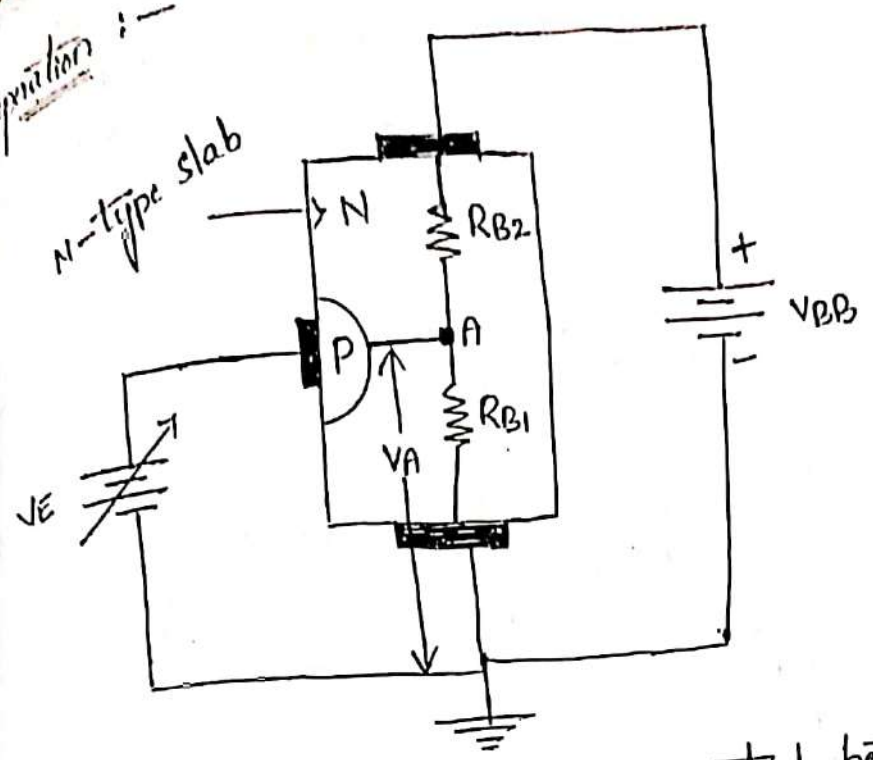
peration :—



The supply voltage V_{BB} is connected between B_1 & B_2 while variable Emitter voltage V_E is applied to Emitter shown in figure.

The potential of A is decided by η ($V_A = \eta V_{BB}$)

Case (i) :— When $V_E < V_D + V_{RB1}$ (or) $V_E = 0$

when no voltage applied at the Emitter, the P-N junction is reverse biased. Hence Emitter current I_E will not flow. Then UJT is said to be "Off".

Case (ii) :— $V_E \geq V_D + V_{RB1}$

The diode drop V_D is generally between 0.3 to 0.7 V

$$V_p = V_A + V_D = \eta V_{BB} + V_D$$

* When $V_E > V_p$ then the P-N junction becomes forward biased and Current I_E flows.
* Due to this the charge carriers are injected in the R_{B1} region of the bar then Conductivity increases.

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* This makes the p-n junction more forward biased, further increases the current and more charge C are injected.
* Under these conditions, the UJT is said to be "on"

UJT characteristics :—

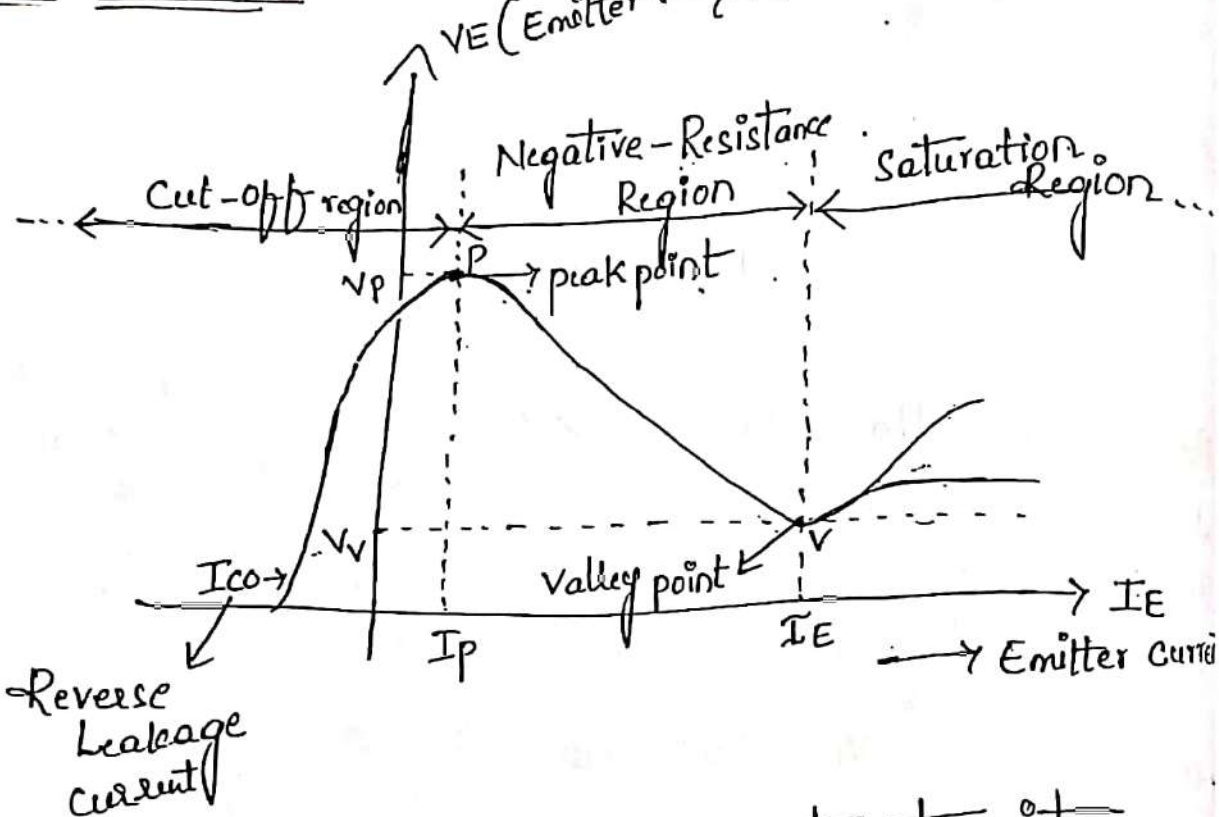

fig :— Characteristics of Uni-Junction transistor.

* Cut-off region :— The $V_E < V_p$ and the p-n junction is reverse biased. A small amount of leakage current I_{EO} flows through the device which is reverse saturation cur

* Negative resistance region :—

When $V_E = V_p$ the p-N junction becomes forward biased and I_E starts flowing. The V_E decreases, I_E increases. Hence the region is called negative resistance region.

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Saturation region :—

Increases in I_E further valley point current I_V drives the device in the saturation region. The voltage corresponding to valley point is called "valley point voltage". At the valley point, the resistance is changes from negative to positive and after the point V. current I_V increases the voltage also increases.

Advantages :—

It is low cost device
It has Excellent characteristics
It is a low-power absorbing device under normal operating conditions.
A negative resistance characteristics
Very low value of triggering current

Disadvantages :—

The main disadvantage of UJT is its inability to provide appropriate amplification.

Applications :—

* UJT is used to generate Sawtooth waveforms
* used in relaxation Oscillator
* used in Speed Control
* Switching Device
* Triggering Device for Triac's, SCR's
* for phase Control
* also used in Timing control.

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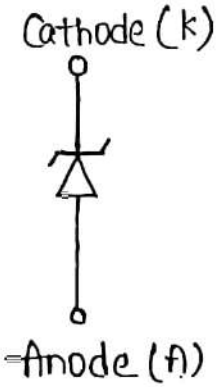
ener Diode :-

- Introduction
- Symbol
- Biasing Conditions
- V-I characteristics
- Advantages and Disadvantages
- Applications.

Introduction :- The zener diode is a silicon p-n junction semiductor device, which is generally operated in its reverse ikdown region. The zener diodes are fabricated with precise ikdown voltages, by controlling the doping level during the facturing. The zener diodes have breakdown voltage range 3V to 200V. In 1934, a physicist Carl zener investiga the breakdown phenomenon in the p-n junction diode

Symbol :-



Biasing Conditions :-

There are two types of Biasing Conditions in the ner diode :- 1. forward Bias
2. Reverse Bias.

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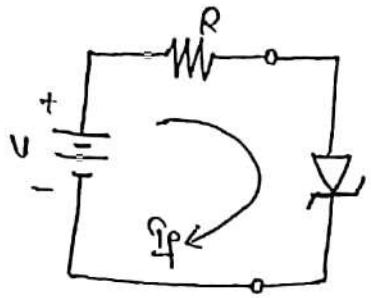
Forward Bias:-

In the forward Biased condition, the normal rec
liode and the zener diode operate in similar way.



R → Current Limiting Resistor

Reverse Bias:-

The zener diode is designed to be operated in the r
iased condition. The reverse biased condition, the diode co
:verse saturation current till the reverse voltage applied
ss than the reverse breakdown voltage. When the reverse
oltage exceeds reverse breakdown voltage, the current thro
I changes drastically but the voltage across it remains
lmost constant. Such a breakdown region is a normal oper
egion for a zener diode. The normal operating regions fo
rectifier diode and a zener diode are shown in the fi
55 (a) and (b).

The breakdown characteristics for a zener diode is signifi
antly important, as it is an operating region for the di
Then the reverse voltage applied to the zener diode is
ncreased, initially the current through it is very small, of
the order of few μA or less. This is the reverse leakage

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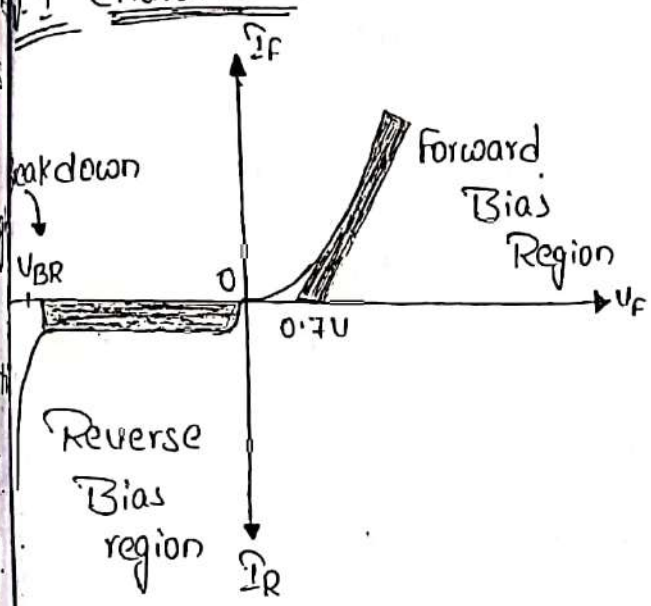
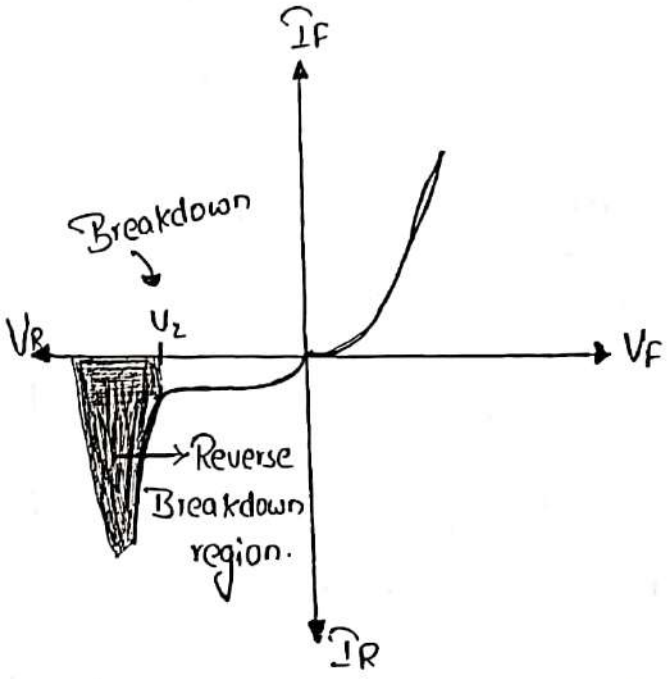
of the diode, denoted by I_D. At a certain reverse current through zener diode increases rapidly. The change from a low value to large value of current is very sharp and well defined. Such a sharp change in the reverse characteristics is called **Knee (or) Zener Knee** of the curve. At this knee, breakdown is said to occur in the device. The reverse voltage at which the breakdown occurs is called as **breakdown voltage**, denoted as V_z.

V-I Characteristics:-



(a) Operating regions shown shaded for Normal diode.



(b) Operating regions shown Shaded for zener diode.

Advantages of Zener Diode:-

The zener diode shunt is very economic as it is of low cost

It has a very simple circuit

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5. It requires only two or three components.
6. It provides a better regulation over a wider range of load currents and input voltages.
7. It provide higher current capability.

Disadvantages of Zener diode:-

- It has poor efficiency for heavy loads because a considerable amount of power is wasted in zener resistance (R_s) and series resistor in comparison with load power.
- The Dc output voltage slightly changes due to zener resistance.
- Changes in load current produce changes in zener current. Consequently the output voltage also changes.
- The internal impedance of the circuit is high.
- The voltage regulation is poor.
- The output voltage is not adjustable because it has $V_o = V_z$
- It cannot be used for large load current

Zener Diode Applications:-

Zener diodes are used in voltage stabilizers (or) shunt regulator.

- Used in Surge suppression circuitry for device protection
- Used in Over voltage protection circuits.
- clipping and clamping circuits
- Used in Switching units.

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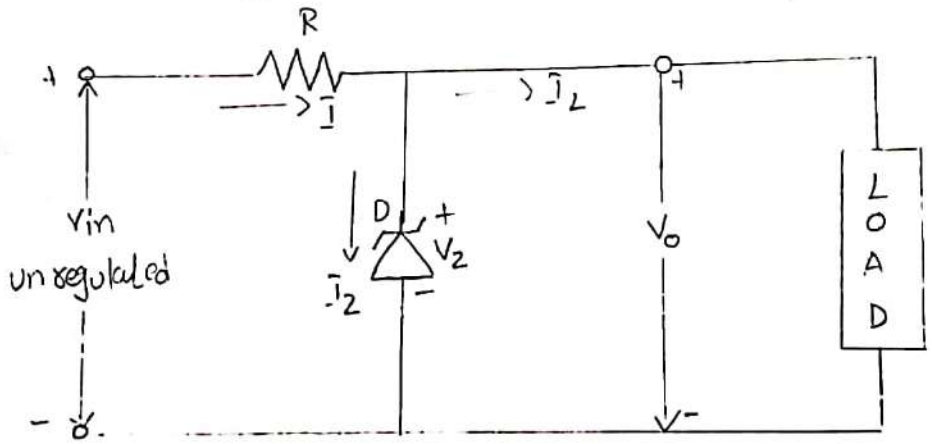
Zener Diode as a Shunt Regulator / voltage Regulator :

=> A regulator is a device whose input is pulsating d.c i.e rectifier output and its output is pure constant d.c voltage.

=> It almost eliminates all the ripples. it also regulates the output voltages to a constant value irrespective of the changes in the output or load.

=> The simplest shunt voltage regulator circuit uses a zener diode, to regulate the load voltage.

=> The Fig. 1.43.1 shows the arrangement of zener diode in a regulator circuit.



=> The zener diode has a characteristics that as long as the current through it is between I_{zmin} and I_{zmax} the voltage across it is constant equal to zener voltage V_z.

=> As zener diode is connected in shunt with the load resistance, the output voltage is equal to the zener voltage.

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=> The value of R can be obtained mathematically as,

$$R = \frac{V_{in} - V_Z}{I} \quad \text{i.e} \quad I = \frac{V_{in} - V_Z}{R}$$

=> while the relation between the various currents is given by $I = I_Z + I_L$

Regulation with varying input voltage :-

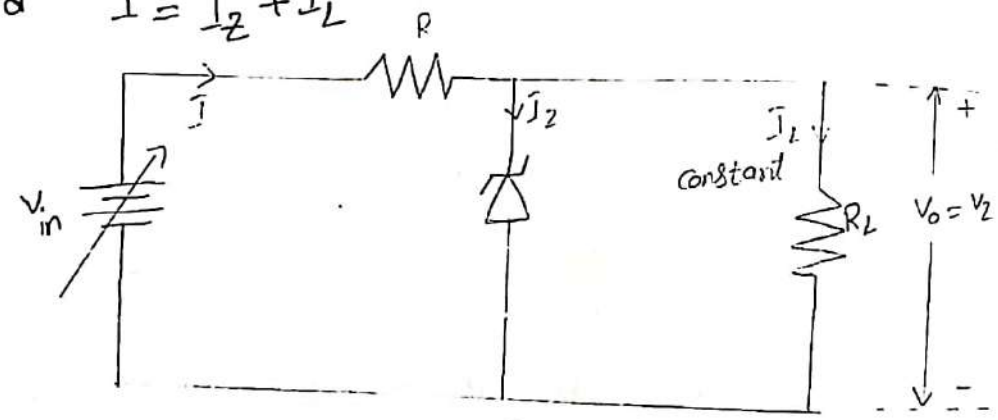
=> The Fig shows a zener regulator under varying input voltage condition.

=> it can be seen that the output is

$V_o = V_Z$ is constant

$$I_L = \frac{V_o}{R_L} = \frac{V_Z}{R_L} = \text{constant}$$

AND $I = I_Z + I_L$



Varying input condition

=> Now if 'V_{in}' increases, then the total current 'I' increases. But I_L is constant as V_Z is constant. Hence the current I_Z increases to keep I_L constant.

=> But as long as I_Z is between I_{Zmin} and I_{Zmax} and V_Z i.e. output voltage V_o is constant

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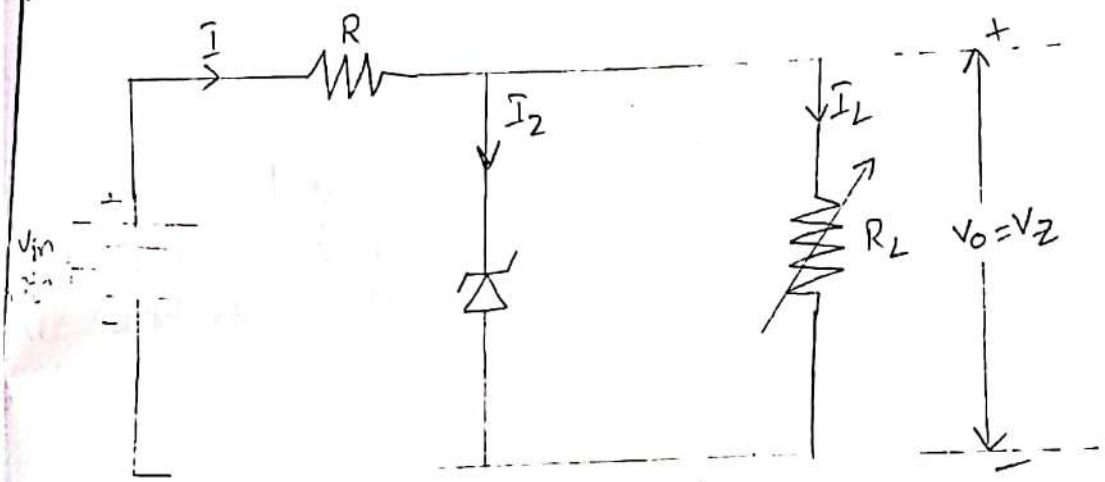
=> thus the changes in input voltage get compensated and output is maintained constant.

=> Similarly if V_{in} decreases, then current 'I' decreases. But to keep I_L constant, I_Z decreases. As long as I_Z is between I_{Zmax} and I_{Zmin} the output voltage remains constant.

Regulation with varying load :-

=> The Fig shows a zener regulator under varying load condition and constant input voltage.



varying load condition

=> The input voltage is constant while the load resistance 'R_L' is variable.

=> As V_{in} is constant and $V_o = V_Z$ is constant, then for constant 'R' the current 'I' is constant

$$I = \frac{V_{in} - V_Z}{R} \quad \text{constant} = I_L + I_Z$$

=> Now if 'R_L' decreases so I_L increases, to keep 'I' constant I_Z decreases. But as long as it is

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between I_z min and I_{zmax} output voltage V_o ca
constant.

=> Similarly if R_L increases so I_L decreases, to
I constant I_z increases. But as long as it
between I_{zmin} and I_{zmax} output voltage V_o
be constant.

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Zener Diode applications :-

- Zener diodes are used in voltage stabilizers (or) shunt regulator.
- used in Surge Suppression Circuitry for device protection
- used in over voltage protection circuits.
- Zener diodes are used in clipping and clamping circuits Especially peak clippers.
- They are used as Reference Elements
- Used in Switching applications.

Voltage Regulator :-

The load voltage equals breakdown voltage Vz of the diode. The Series resistor limits the Current through the diode and drops the Excess voltage when the diode is conducting.

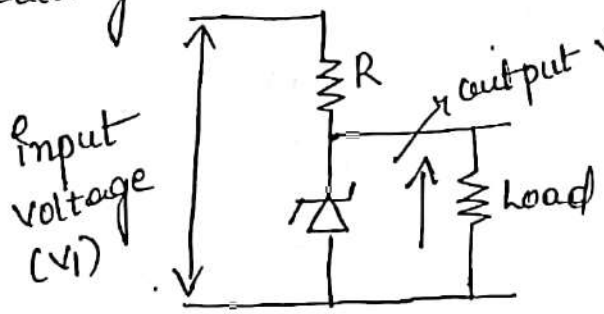

fig: Zener diode shunt regulator.

Zener diode in overvoltage protection:

If the input voltage increases to a value higher than the Zener breakdown voltage, Current flows through the diode and Create a voltage drop across the resistor; this triggers the SCR and creates a short circuit to the ground. The short circuit opens up the fuse and disconnects the load from the supply.

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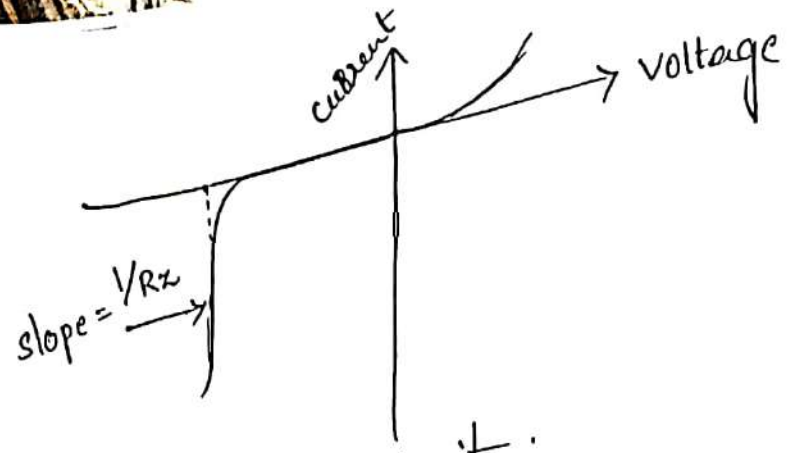

fig: SCR Overvoltage circuit.

Zener diode clipping circuits :—

Zener diodes are used to modify or shape AC waveform clipping circuits. The clipping circuit limits clips off parts of one or both of the half cycles of AC waveform to shape the waveform or provide protect

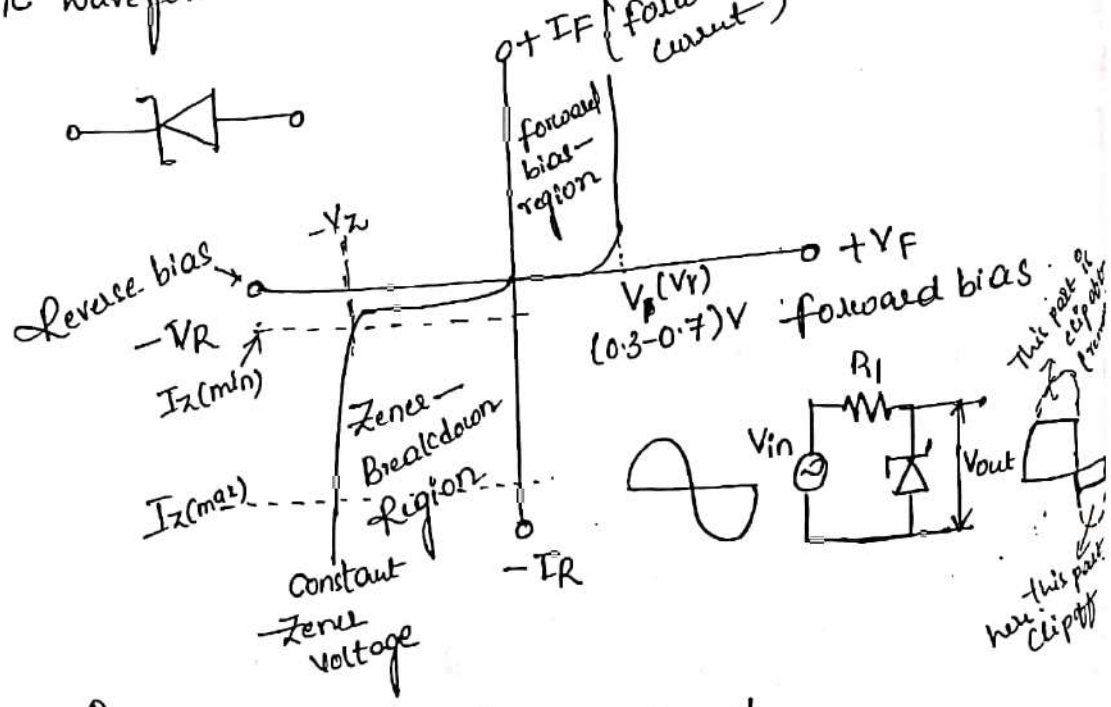

fig: Zener diode clipping circuits.

Other applications are waveform clippers, voltage shifter, over voltage op-amp gain control limiter, meter protection,

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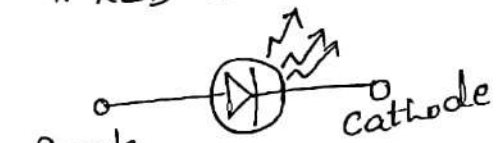
(Light Emitting Diode)

P:-
- Meaning of LED
- Symbol of LED
- construction of LED
- Working principle (Operation also)
- characteristics (output characteristics)
- Advantages and Disadvantages
- Applications

eaning of LED :- A Diode which Emits light when forward Biased is called LED

* LED is abreviated as "Light-Emitting Diode".

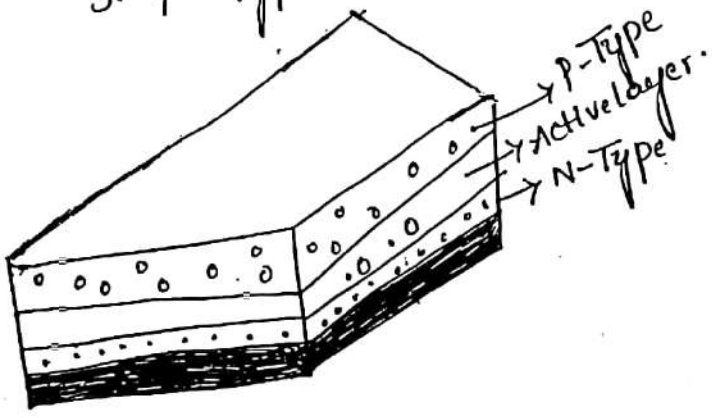
ymbol :-

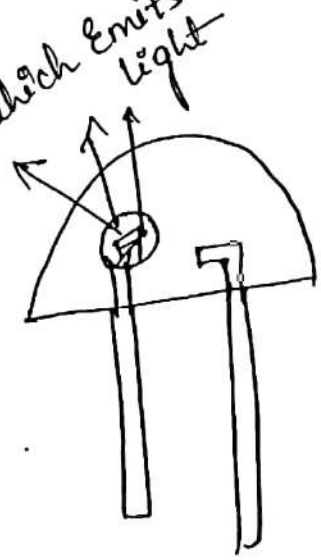


onstruction :-

In LED three Semiconductors layers on the Substrate re used as shown

1. N-Type
2. Active region - Responsible for Emission of light
3. P-Type





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In LED Emits light all the way around the layered structure. This layered structure is placed in a reflective cup so that the light gets reflected from the desired Exit direction.

Working principle :-

* The LED Works on the principle of "Electroluminescence"
* When the p-N junction is forward biased, the electrons in n-region Cross the junction and recombine with Holes in n-region.
* practically when LED is forward biased, the holes from p-region and electrons from n-region Enter into active region between p and n regions.
* In the active region recombination of Electrons and holes takes place and the Energy is released in the form of a light.
* The Energy released depends on the forbidden gap-Energy which determines the wavelength and Colour of the Emitted light.
* "Electroluminescense" is an "Electrical phenomenon in which a material Emits light in responce to the passage of an Electric current".

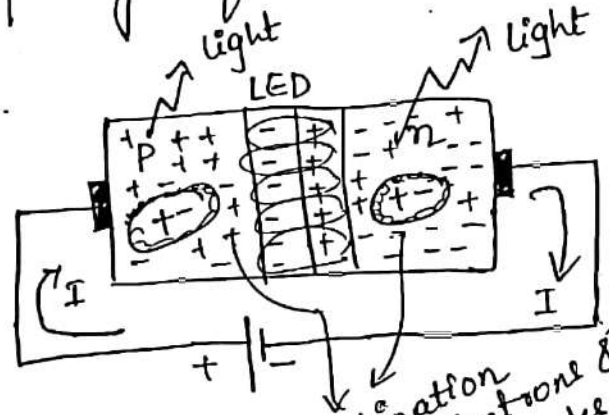

Fig :- forward-biased LED.

Recombination of electrons & holes → during recombination It Emits light

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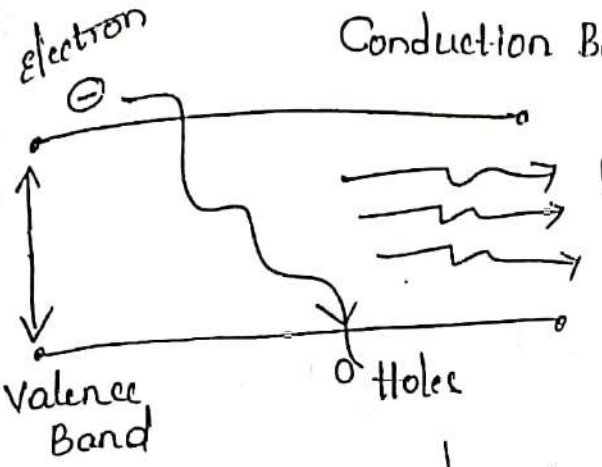

Planck's constant

$E = hf$

$E = h \cdot \frac{c}{\lambda}$

$E \propto \frac{1}{\lambda}$

C = speed of light.

λ = wavelength.

fig :- Process of Electroluminescence.

Materials of LED's

Materials	Sym. Indication	Colour
allium Arsenide →	GaAs →	Infrared
allium phosphide →	GaP →	Red (or) Green
allium Arsenic phosphide →	GaAsP →	Red (or) yellow.

ut characteristics :-

The amount of power output translated into light directly proportional to the forward current I_f.

lore forward current I_f, the greater the output light

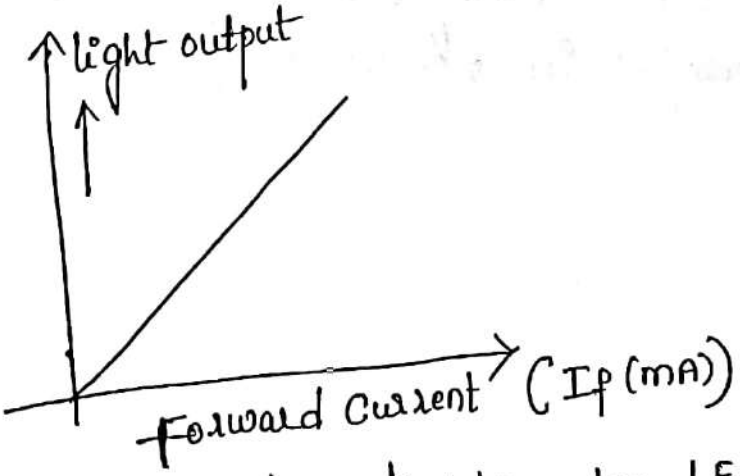

fig :- Output Characteristics for LED

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dvantages :..

LED's are Small in Size

The LED displays operated under different ambient lighting Conditions.

LED's are fast operating devices (ON/OFF in 1μs)

The LED's are light in weight

The LED's are available in various colours

The LED's have long life

LED's are cheap.

isadvantages :—

* It requires frequent replacement of battay in low power battay operated devices

Luminous Efficiency of LED is Low (1.5 lum/watt)

The characteristics are affected by Temperature.

Need large power for Opeation Compared to normal P-N junction diode.

Applications :—

All kinds of visual displays i.e Seven Segment displays such as Watches and calculators.

In the optical devices.

ON-OFF indicators in various types of electronic circuits.

Some LED's radiates Infrared light which is invisible such LED's useful in remote Control and burglar alarm.

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Manufacturing materials of LED :-

ing | Ga As (Gallium Arsenide) — Infraed
Al Ga As (Aluminium Gallium Arsenide) — red.
Ga As, Ga P (Gallium phasphide) — red.

(Al Ga As)
(Ga P)
Al Ga In P) } — Orange

Ga As P
Al Ga In P
Ga P } — yellow

Green -
Ga In P
Al Ga In P } — Green.

Zn S
Zinc selenide) } — Blue
In Ga N
Indium Gallium Nitrade.

In Ga N — Violate

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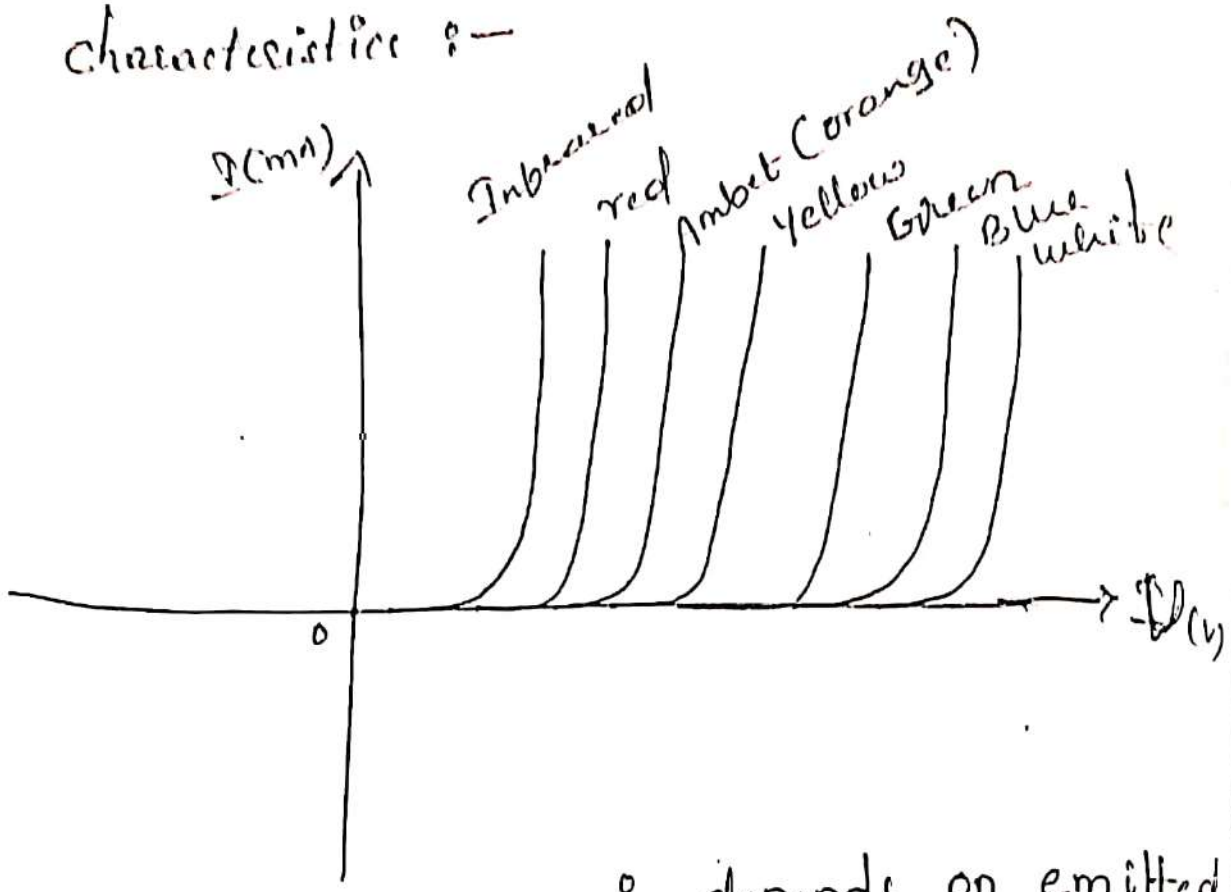
* Characteristics :—



* In LED, Cut-in voltage is depends on emitted Colour of light i.e 1.5V to 3.5V (forward voltage drop).

* Maximum Current is 30mA, if it is more than 30mA, LED get damage.

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Liquid Crystal Display [LCD]

- Introduction
- Arrangement of mods
- Types of LCD
- Advantages
- DISAdvantages
- Applications

Introduction:

The liquid crystal are one of the most fascinating material system in nature, having properties of liquid as well as of a solid crystal. The terms liquid crystal refers to the fact that these compounds have crystalline arrangement of molecules, yet they flow like a liquid. liquid crystal display do not emit or generate light, but rather alter externally generated illumination. Their ability to modulate light when electrical signal is applied has made them very useful in flat panel display technology

→ The different Arrangement of these rod like molecules lead to three main categories of liquid crystals

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→ smetic
→ Nematic
→ cholesteric

Smetic :-

In this structure the rod like molecules are arranged in layers, and within each layer there is orientational order over a long range. Thus, in a given layer, the rods are all oriented in the same direction. Also, in the smetic liquid crystals the molecules of different layers are ordered as shown in figure. Thus, both orientation order and positional order is present in the smetic crystals.

Nematic :-

In the Nematic structure the positional order between layer of molecules is lost, the orientation order is maintained.

cholesteric :-

In these crystals the rod like molecules in each layer are oriented in a different angle within each layer orientation order is maintained in each layer. The cholesteric liquid crystal is related to the nematic crystal, with the difference being the twist of the molecules as one goes from one layer to another.

There are

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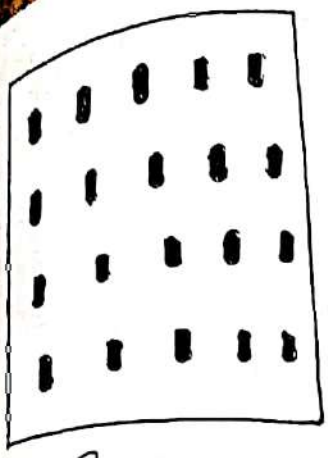
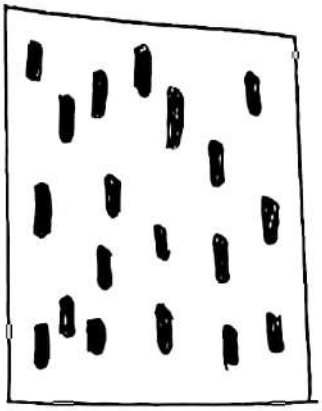
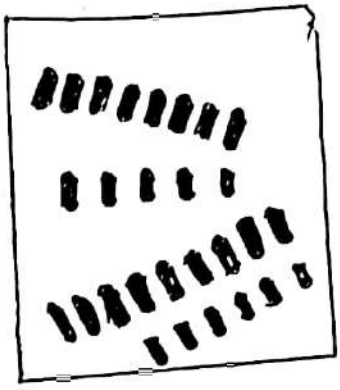


(a) Smetic



(b) Nematic



(c) Cholestric

there are two types of liquid crystal displays according the theory of operation:

1. Dynamic scattering LCD
2. Field Effect LCD

Dynamic scattering LCDS :-

It shows the construction of a typical liquid crystal ell. It consists of a layer of liquid crystal material andwiched between glass sheets with transparent metal ilm Electrodes. usually, an optically thin (about 50 nm) ayer of Indium Tin oxide (ITO) on each surface acts s an Electrode to allow a voltage to be held across the ell. The aligning treatment is then applied on the top f ITO.

when the cell is not activated, the liquid crystal transparent. when it is activated the molecular rbulence causes the light to be scattered in all rections so that the activated areas appear bright. his phenomenon is known as <u>dynamic scattering</u>.

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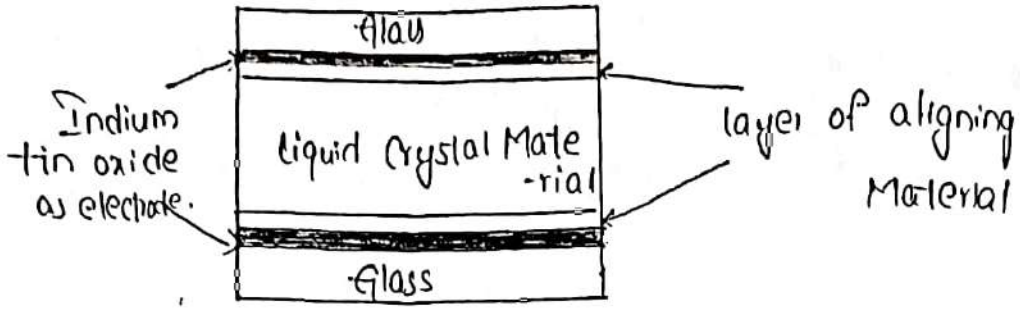
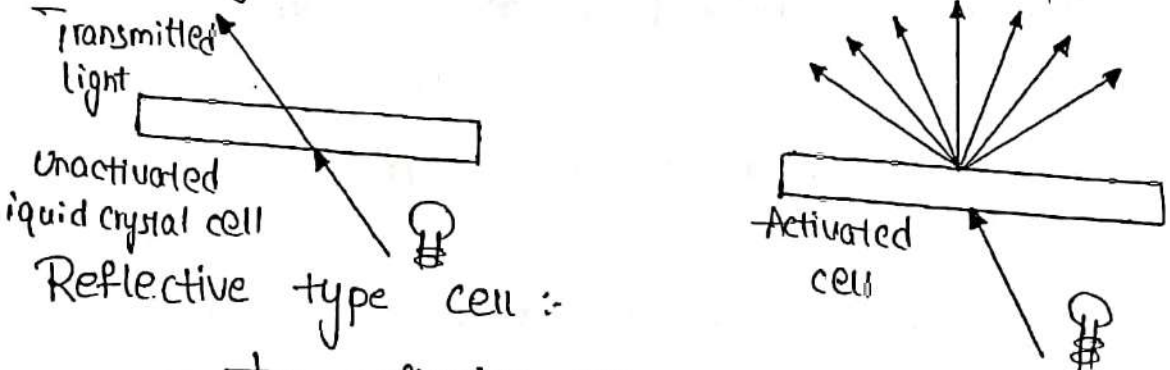
With both glass sheets transparent, the cell is known as a transmittive type cell.



When only one glass plate sheet is transparent and other has a reflective coating, the cell is termed reflective type.

Transmittive Type cell :-

When not activated, cell will simply transmit area of glass Edge lighting through the cell in straight lines. In this light condition the cell will not appear bright. When the cell in the is activated the incident light scatters and cell appears through quite bright.



Reflective type cell :-

The reflective type cell operates from light incident on its front surface. When it is not activated, light is reflected in the usual way from the mirror surface. and the cell does not

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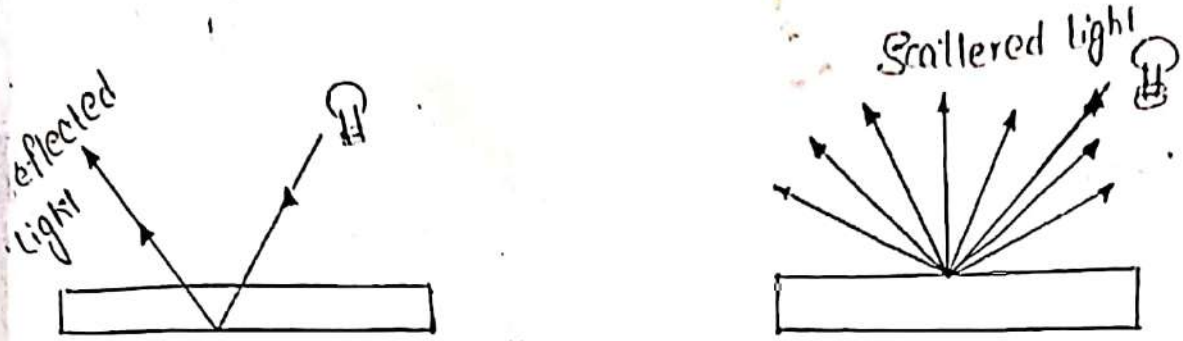
scattering occurs and cell appears bright.



Unactivated liquid crystal cell — Activated cell

Field Effect LCD :

It shows the field effect liquid crystal cell. It consist of two glass plates, a liquid crystal fluid, polarizers and transparent conductors. The liquid crystal fluid is sandwiched between two glass plates. Each glass plate is associated with light polarizer. The light polarizers are placed at right angle to each other. In the absence of electrical excitation, the light coming through the front polarizer is rotated through 90° in the fluid and passed through the rear polarizer. It is then reflected to the viewer by the back mirror as shown in figure.

On the Application of electrostatic field, the liquid crystal fluid molecules get aligned and therefore light through the molecules is not rotated by 90° & it is absorbed by the rear polarizer as shown in figure. This causes the appearance of dark light on a light background.

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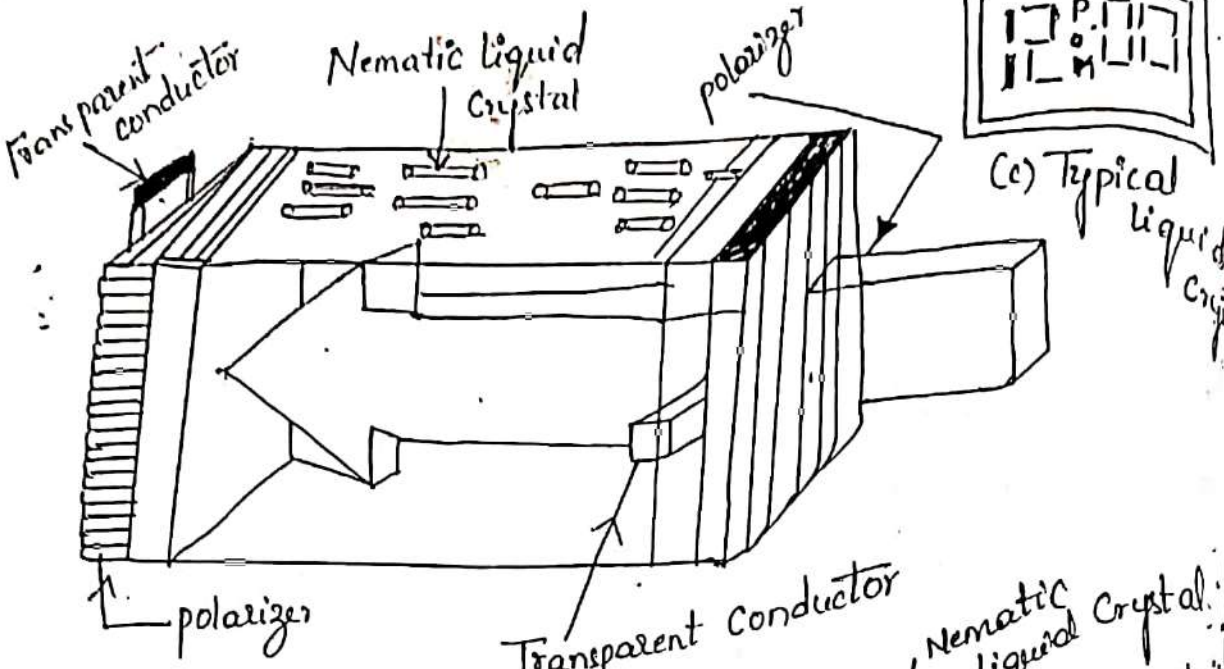

(c) Typical liquid Cr

(b) field Effect cell OFF State

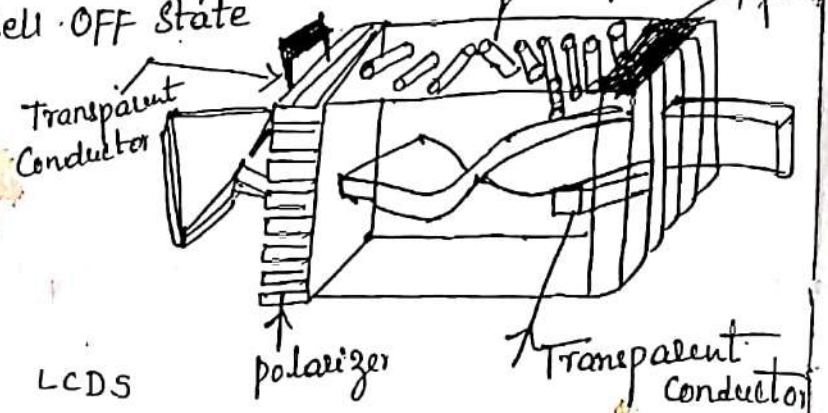

fig: field Effect cell "O State"

Advantages of LCDS

1. less power consumption
2. low cost
3. uniform brightness with good contrast
4. low operating voltage and current

DisAdvantages of LCDS

1. poor reliability
2. limited Temperature range
3. Poor visibility in low ambient temperature
4. Slow speed
5. Requires an ac drive

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Applications :—

- LCD's are used in Display Screen in calculations
- Digital Cameras
- TVs
- Computer monitor
- Digital wrist watches
- Mobile Screens
- Video players etc.

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2(A). RECTIFIERS

Concept of Rectifiers :—

- What is Rectifier
- What is the need of Rectifier
- Block diagram of Rectifier & characteristics
- Types of Rectifiers (Different types - circuits, operation, wave-form)
- Derivations of characteristics of Rectifiers
- Comparison of Rectifiers
- Applications, Advantages, Disadvantages of all types of Rectifiers.

1 Rectifiers :—

Definition :— A Rectifier is a device which Converts a.c voltage to pulsating d.c voltage, using one or more p-n junction diodes.

(or)

Rectifier is a device which Converts an Bi-directional a.c signal into uni-directional d.c signal.

2. Need of Rectifiers :— Rectifiers are the power electronic Circuits which Converts AC power (which is available from the power sockets in home) in to Dc power (which is available from batteries). The advantage of Dc power over AC power is it (Dc) can be stored in batteries where as AC power can't be stored. So every portable electronic device requires a battery to run it. So batteries in turn requires Dc power to charge them. So in order to charge the batteries in your portable electronic devices like mobile phones, laptops, etc (The ones with battery in it). Rectifiers are used to Convert bidirectional a.c to uni-directional d.c.

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Characteristics of Rectifiers :—

The important points to be studied while analyzing the various rectifier circuits are,

a). Waveform of the load current

b). Regulation of the output voltage (study the effect of change in load current on the load voltage)

c). Rectifier Efficiency (How efficiently the rectifier circuit converts a.c into d.c

d). peak value of current in the rectifier circuit (maximum value of current – decides rating of rectifiers)

e). peak value of voltage across the rectifier element in the reverse direction (PIV)

f). Ripple factor (amount of A.C component in output of rectifier)

Block diagram of Rectifier :—

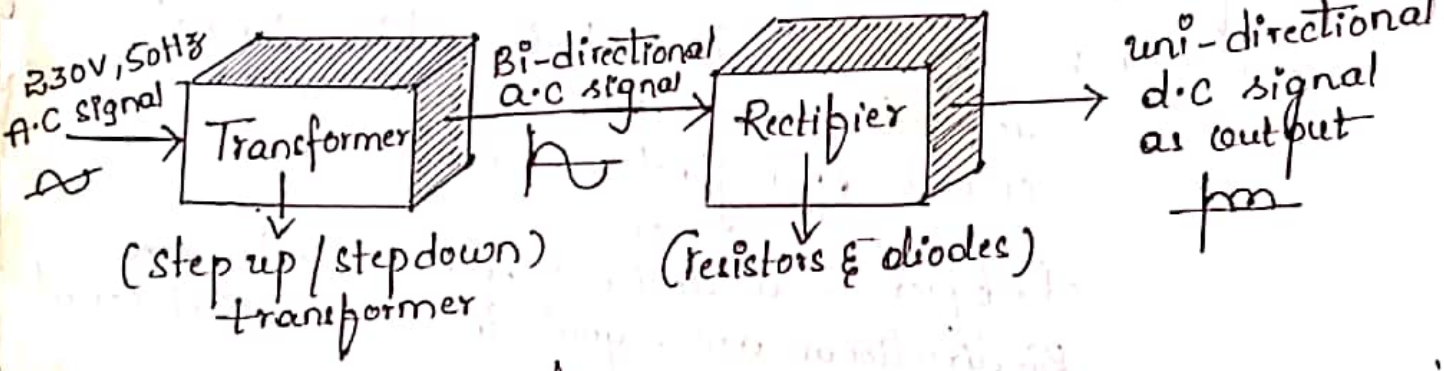

fig: Rectifier Block-diagram

Rectifiers are used for rectification of a.c signal (voltage) (correction of errors) and converts into d.c. The above figure shows block diagram of Rectifier. In this first block is "Transformer". Transformer is used to bring the level of a.c voltage, if we want to increase the level of a.c voltage we use "step-up-transformer". If we decrease the level of a.c voltage we use "step-down transformer". AC signal (voltage 230V, 50Hz for India) is applied to the Transformer

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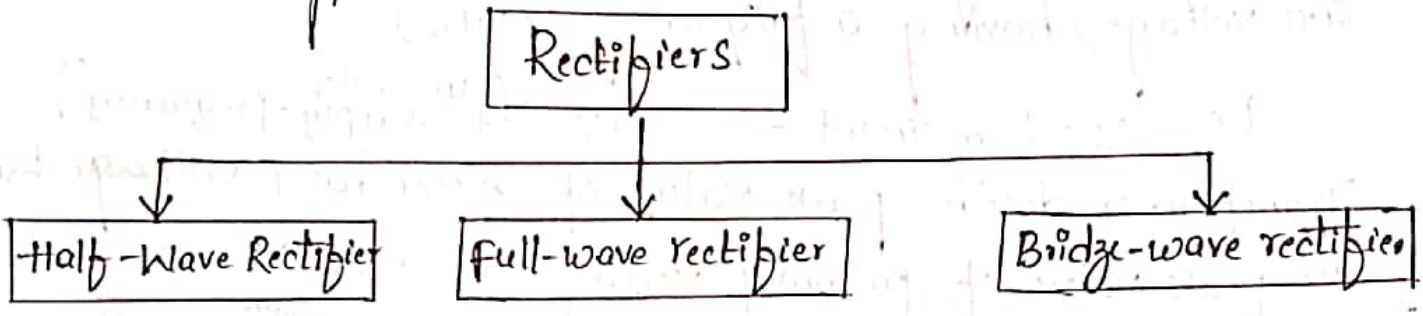
The output of transformer is given to the input of the Rectifier block. Rectifier is used for "Rectification" (i.e process of correcting Error of a.c for converting a.c into d.c). In rectifiers we are using resistors and diodes. It converts an a.c signal into "pulsating d.c / uni-directional d.c".

Types of Rectifiers :—

Using one or more diodes, rectifiers are classified into 3 types. Those are



1. Half-wave rectifier :—

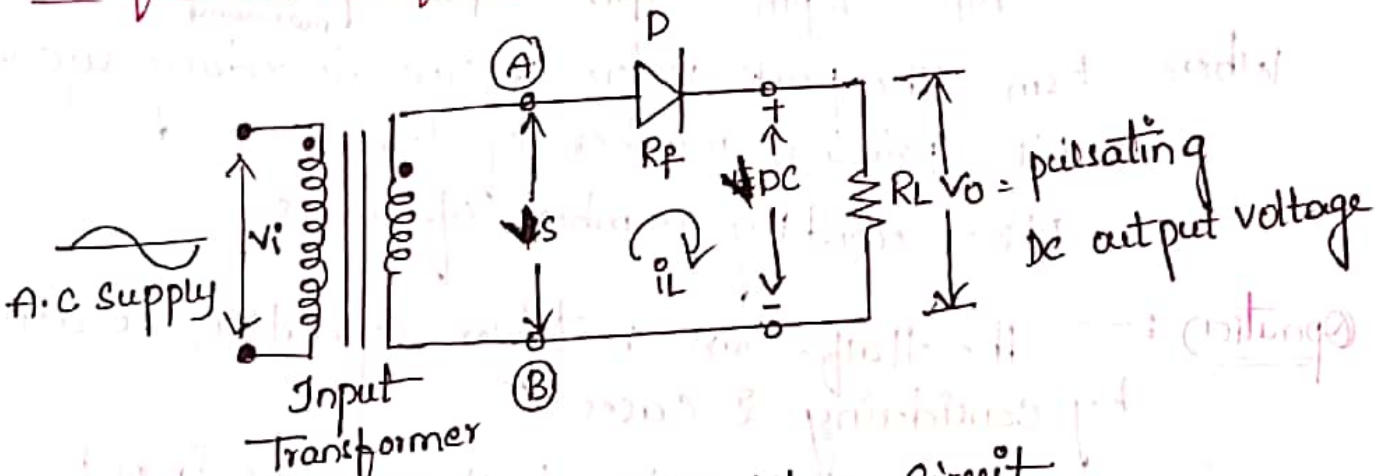


fig: Half-wave rectifier Circuit

* In Half wave rectifier, rectifying element conducts only positive half cycle of input a.c supply.
* The negative half cycles of a.c supply are eliminated from the output.

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* This rectifier circuit consists of resistive load, rectifying Element i.e p-n junction diode, and the source of a.c or voltage, all are connected in Series.
* Usually the rectifier circuits are operated from ac main supply
* To obtain the desired d.c, the a.c voltage is applied to rectifier circuit using suitable step-up or step-down transformer, mostly a step-down one, with necessary turns ratio.
* The input voltage (230V) of half-wave rectifier is a Sinusoidal a.c voltage, having a frequency (50Hz).

i.e $e_s = E_{sm} \sin \omega t \longrightarrow (1)$ ($\omega = 2\pi f$, f = supply frequency)

Transformer decides peak value of Secondary voltage E_{sm} the peak value of primary voltage is E_{pm}

$$\therefore \frac{N_2}{N_1} = \frac{E_{sm}}{E_{pm}} = \frac{V_{sm}}{V_{pm}} \Rightarrow \frac{\text{Secondary maximum Voltage}}{\text{primary maximum Voltage}}$$

Where E_{sm} = The peak value of the Secondary a.c volta
N_1 = primary number of turns
N_2 = Secondary number of turns

Operation :— The Half-wave rectifier Operation is done by considering 2 cases

(i) By applying positive half cycle as input
(ii) By applying negative half cycle as output

i.e during positive half cycle — Diode acts as forward bias
and during negative half cycle — Diode acts as Reverse-bias

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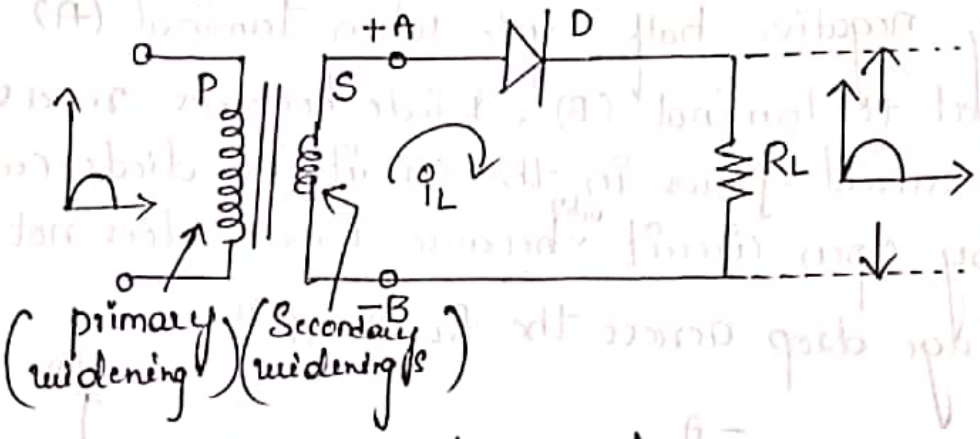
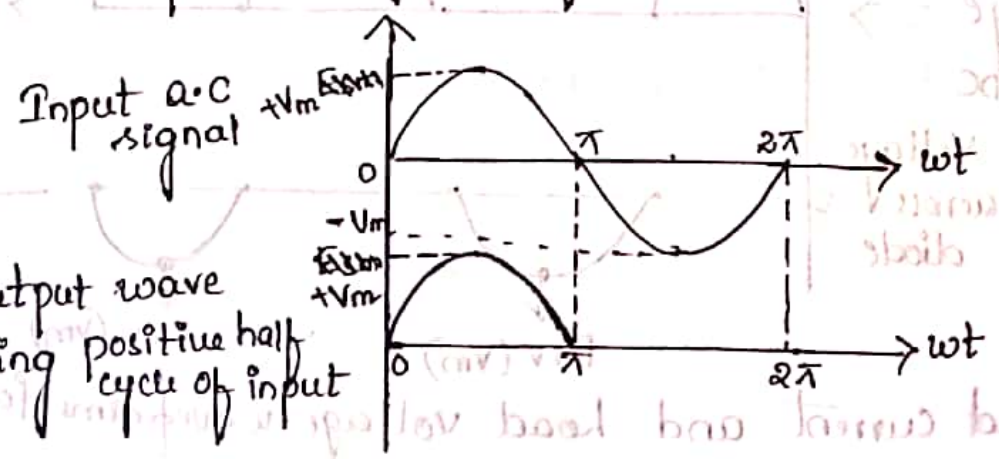
Case (i) :- During positive half cycle



(a) Diode forward biased

* During positive half cycle of secondary a.c voltage, terminal (A) becomes positive with respect to terminal (B).
* The diode is forward biased and the current flows in the circuit in the clockwise direction as shown in fig (a).
* The current will flow for almost full positive half cycle This current is also flowing through load resistance R_L denoted as i_L, the load current.
* The Diode can be replaced by a short circuit the current flows through the circuit obtained at load resistor
* So, the half-wave rectifier is a rectifier circuit, conducts only half of the wave of applied input signal. So it is called "half-wave rectifier".
* The output waveform of rectifier (half-wave) is shown below:



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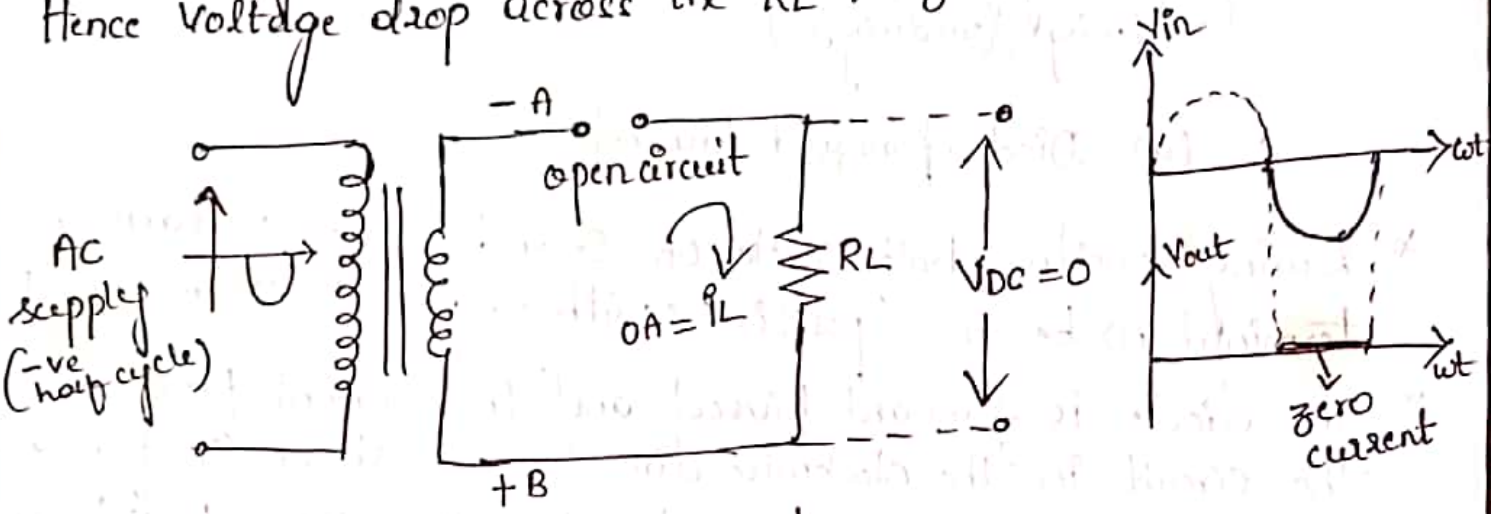
Case (2) :- During negative half-cycle as a input

During negative half-cycle when teminal (A) is negative with respect to teminal (B). Diode becomes reverse biased. Hence no current flows in the circuit i.e diode can be replaced by open circuit ~~x~~ why because Diode does not conduct Hence voltage drop across the R_L is zero



(b) Diode reverse biased

Output Waveform for Half-wave rectifier circuit :-

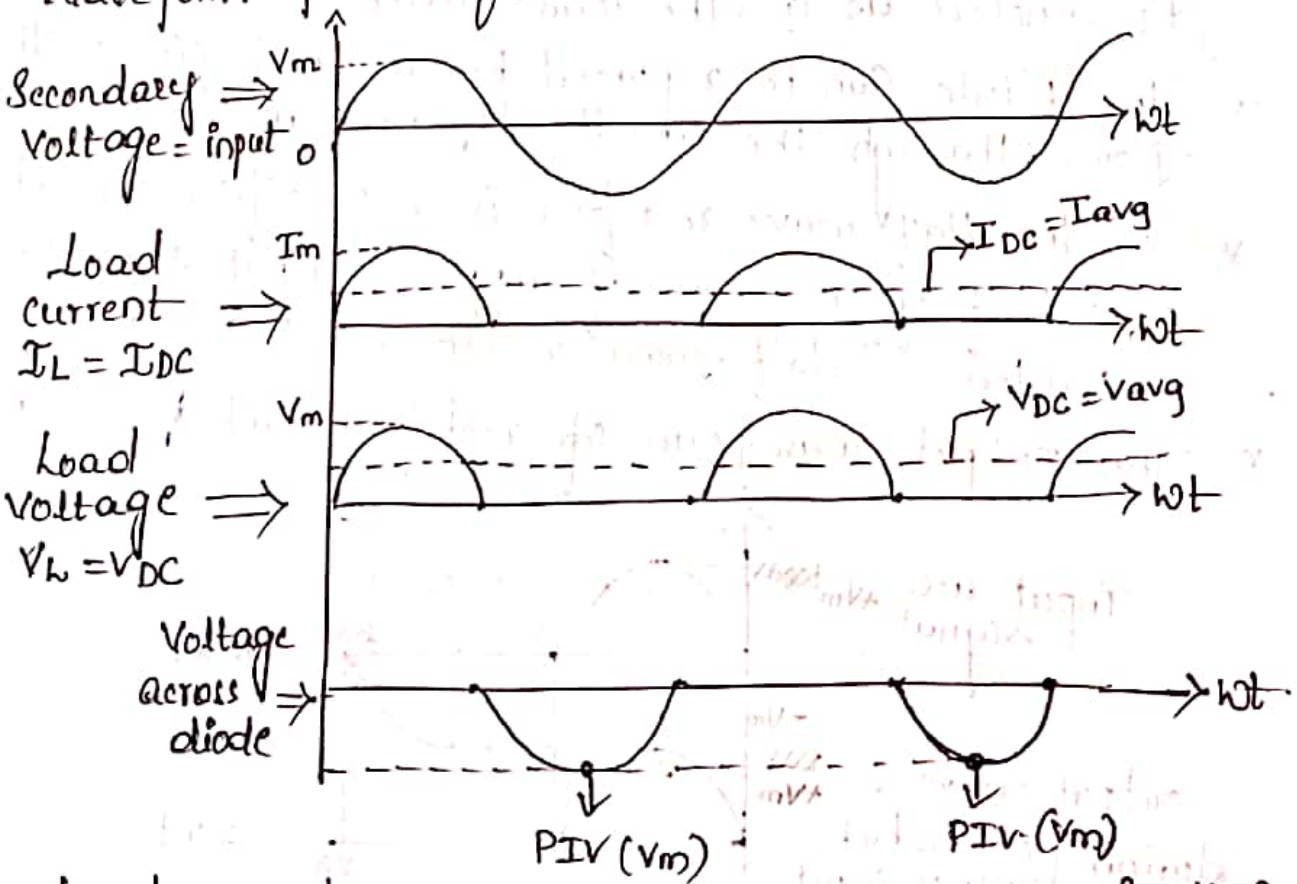


Fig :- Load current and Load voltage waveforms for HWR.

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The D.C waveform is expected to be a straight line but the half-wave rectifier gives output in the form of positive sinusoidal parts.

Hence, the output is called "pulsating D.C". It is discontinuous in nature. Hence it is necessary to calculate the average value of load current and average value of output voltage.

Derivations of characteristics of Half-wave rectifier :-

1. Average D.C Load current (I_{DC})
2. Average D.C Load voltage (V_{DC})
3. R.M.S Value of Load current (I_{RMS})
4. R.M.S Value of Load voltage (V_{RMS})
5. D.C power output (P_{DC})
6. A.C power input (P_{AC})
7. Rectifier Efficiency (η)
8. Ripple factor (γ)
9. Load current (I_L)
10. peak Inverse voltage (PIV)
11. Transformer utilization factor
12. Voltage Regulation (%R)

These are the Various Important Characteristics of Half-wave rectifier circuit. The derivations of these all are as follows.

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1. Average D.C Load Current :-

The Average (or) D.C Value of alternating current is obtained by "integration".

For finding the average value of an alternating wave-form we have to determine the area under the curve one Complete Cycle i.e from 0 to 2π and then dividing it by the base i.e 2π.

Mathematically, current wave-form can be described as,

$$i_L = I_m \sin\omega t \quad \text{for } 0 \le \omega t \le \pi$$
$$= 0 \quad \text{for } \pi \le \omega t \le 2\pi$$

where

I_m = peak value of load current

$$I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} i_L \, d(\omega t)$$

$$= \frac{1}{2\pi}\int_0^{2\pi} (I_m \sin\omega t)\, d\omega t$$

As no current flows during negative half cycle of a.c input voltage i.e between $\omega t = \pi$ to $\omega t = 2\pi$, we change the limits of integration.

$$\therefore I_{DC} = \frac{1}{2\pi}\int_0^{\pi} I_m \sin\omega t \, d\omega t + \frac{1}{2\pi}\int_{\pi}^{2\pi} I_m \sin\omega t \, d\omega t$$

$$= \frac{1}{2\pi}\int_0^{\pi} I_m \sin\omega t \cdot d\omega t$$

$$= \frac{1}{2\pi} I_m \left(\int_0^{\pi} \sin\omega t \cdot d\omega t\right)$$

$$= \frac{I_m}{2\pi}\left(-\cos\omega t\right)_0^{\pi} = \frac{-I_m}{2\pi}(\cos\pi - \cos 0)$$

$$= \frac{-I_m}{2\pi}(-1-1) = \frac{-I_m}{2\pi}(-2) = \frac{I_m}{\pi}$$

$$\therefore \boxed{I_{DC} = I_m/\pi}$$

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$$I_{DC} = \frac{I_m}{\pi} = \text{Average value}$$

Where $I_m = \frac{V_m}{R_f + R_s + R_L}$

Where R_s = Resistance of Secondary winding of transformer

R_f = forward resistance of diode

R_L = load Resistance

I_m = Maximum (or) peak value of current

V_m = Maximum (or) peak Value of voltage.

Note :- If R_s, R_f are given then we consider these values if these are not given then neglected while calculating I_m

i.e $I_m = \frac{V_m}{R_L}$ ($\because R_s, R_f << R_L$ – neglect R_s, R_f).

2). Average D.C Load voltage :-

It is the product of average (or) D.C load current and the load resistance R_L.

$$V_{DC} = I_{DC} \cdot R_L$$

$$= \frac{I_m}{\pi} \cdot R_L \quad \left(\because \text{where } I_{DC} = \frac{I_m}{\pi}\right)$$

$$V_{DC} = \frac{V_m}{\pi(R_f + R_s + R_L)} \cdot R_L \quad \left(\because I_m = \frac{V_m}{R_L + R_s + R_f}\right)$$

R_s, R_f are practically very small so neglect these.

$$V_{DC} = \frac{V_m}{R_L \cdot \pi} R_L = \frac{V_m}{\pi} \quad \therefore \boxed{V_{DC} = \frac{V_m}{\pi}}$$

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3. R·M·S Value of Load current (I_{RMS}) :-

The R·M·S means Squaring, finding mean and then finding Square root. Hence R·M·S value of load current can be obtained as,

$$I_{R\cdot M\cdot S} = \sqrt{\frac{1}{2\pi}\left(\int_0^{\pi}(I_m \sin\omega t)^2 d\omega t\right)}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2\omega t \cdot d(\omega t)} \qquad \left(\sin^2\omega t = \frac{1-\cos 2\omega t}{2}\right)$$

$$= I_m\sqrt{\frac{1}{2\pi}\int_0^{\pi}\left(\frac{1-\cos 2\omega t}{2} d\omega t\right)}$$

$$= I_m\sqrt{\left(\frac{\omega t}{2} - \frac{\sin 2\omega t}{2\times 2}\right)_0^{\pi}} \qquad (\text{as } \sin 2\pi = \sin(0) = 0)$$

$$= I_m\sqrt{\frac{1}{2\pi}\left(\frac{\pi}{2} - 0\right)}$$

$$= I_m\sqrt{\frac{1}{4}}$$

$$\boxed{I_{RMS} = \frac{I_m}{2}}$$

4. R·M·S Value of Load voltage :-

$$V_{R\cdot M\cdot S} = (I_{R\cdot M\cdot S})\, R_L$$

$$= \frac{I_m}{2}\cdot R_L \qquad \left(R_s, R_f \ll R_L \text{ neglect } R_s, R_f\right)$$

$$= \frac{V_m}{2(R_L + R_s + R_f)}\cdot R_L$$

$$= \frac{V_m}{2R_L}\cdot R_L = \frac{V_m}{2} \qquad \boxed{V_{RMS} = \frac{V_m}{2}}$$

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5. D.C power output (P_{DC}) :-

The D.C power output can be obtained as,

$$P_{DC} = V_{DC} \cdot I_{DC}$$

According to ohm's law ($\because V_{DC} = I_{DC} \cdot R_L$)

$$= (I_{DC} \cdot R_L) \cdot I_{DC}$$

$$P_{DC} = (I_{DC})^2 \cdot R_L$$

DC power output $= I_{DC}^2 \cdot R_L = \left(\frac{I_m}{\pi}\right)^2 R_L = \frac{I_m^2}{\pi^2} R_L$

$$P_{DC} = \frac{I_m^2}{\pi^2} R_L \quad \text{where } I_m = \frac{V_m}{R_L + R_s + R_f}$$

$$P_{DC} = \frac{V_m^2 \cdot R_L}{\pi^2 (R_f + R_s + R_L)^2}$$

$$P_{DC} = \frac{V_m^2 \cdot R_L}{\pi^2 \times R_L^2} = \frac{V_m^2}{\pi^2 \cdot R_L}$$

$$\left(P_{DC} = \left(\frac{V_m}{\pi}\right)^2 \left(\frac{1}{R_L}\right)\right)$$

6. A.C power input :-

The power input taken from the secondary of transformer is the power supplied to three resistances namely load-resistance R_L, the diode resistance R_f, winding resistance R_s. The a.c power is given by,

$$P_{AC} = I_{Rms}^2 [R_L + R_f + R_s]$$

but $I_{rms} = \frac{I_m}{2}$

$$\therefore \left(P_{AC} = \frac{I_m^2}{4} (R_L + R_f + R_s)\right)$$

($\because P_{AC} = I_{AC} \cdot V_{AC}$
$= I_{AC} (I_{AC} R)$

$P_{AC} = I_{AC}^2 \cdot R_L$

$\left(P_{AC} = I_{rms}^2 \cdot R_L\right)$

$(I_{AC} = I_{rms})$

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6. Rectifier Efficiency (η) :—

The rectifier efficiency is defined as the ratio of output d.c power to input a.c power

$$\eta = \frac{\text{D.C output power}}{\text{A.C input power}} = \frac{P_{DC}}{P_{AC}}$$

$$\eta = \frac{\left(I_m^2/\pi^2\right) \cdot R_L}{\frac{I_m^2}{4}(R_L + R_S + R_f)} = \frac{(4/\pi^2) R_L}{R_f + R_S + R_L}$$

$$\left(\eta = \frac{0.406}{1 + \left(\frac{R_f + R_S}{R_L}\right)}\right) \rightarrow$$ Efficiency is 0.406, this formula is used when R_f, R_s are given during calculation

If R_S, R_f are very small practically so neglect it then

$$\eta = \frac{(4/\pi^2) \cdot \cancel{R_L}}{\cancel{R_L} + \cancel{R_S}^{\to 0} + \cancel{R_f}^{\to 0}} = \frac{4}{\pi^2} = 0.406$$

$$\eta = 0.406$$

Percentage of efficiency ($\%\eta$) $= 0.406 \times 100$

$= 40.6\%$

$$(\%\eta = 40.6\%)$$

Thus, In HWR, maximum 40.6% a.c power gets converted to d.c power at the load. The remaining 60% of power is present interms of ripples in the output which is fluctuating Component (pulsating D.C).

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7. Ripple factor :-

It is seen that the output of half wave rectifier is not pure d.c but a pulsating d.c. The output contains pulsating components called "Ripples". The measure of such ripples present in the output is with the help of factor called "Ripple factor". it is denoted by γ (or) Γ (gama). It tells how smooth is the output.

* Smaller the ripple factor $\simeq$ closer to pure d.c

$$\text{Ripple factor } \gamma = \frac{\text{R.M.S value of a.c Component of output}}{\text{Average (or) D.C Component of output}}$$

Now, the output current is composed of a.c Component as well as d.c Component.

Let I_{ac} = r.m.s value of a.c Component present in output.

I_{DC} = D.C Component present in output

I_{RMS} = R.M.S Value of total output current

$$I_{RMS} = \sqrt{I_{ac}^2 + I_{DC}^2}$$

$$I_{ac} = \sqrt{I_{Rms}^2 - I_{DC}^2}$$

$$\therefore \text{Ripple factor} = \frac{I_{ac}}{I_{DC}}$$

$$\gamma = \frac{\sqrt{I_{rms}^2 - I_{DC}^2}}{I_{DC}}$$

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$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1}$$

This is general Expression for ripple factor and can be used for any rectifier circuit.

Similarly, ripple factor interms of voltage is same

i.e

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{DC}}\right)^2 - 1}$$

Now for a half-wave rectifier circuit,

$$I_{rms} = \frac{I_m}{2}, \quad I_{DC} = \frac{I_m}{\pi}$$

$$\gamma = \sqrt{\frac{\left(\frac{I_m}{2}\right)^2}{\left(\frac{I_m}{\pi}\right)^2} - 1} = \sqrt{\left(\frac{\pi^2}{4}\right) - 1} = \sqrt{1.4674} = 1.21$$

$$\gamma = 1.211$$

This indicates that the ripple contents in output are 1.21 times the d.c component i.e 121.1% of d.c component

Note:- The Ripple factor is minimised using filter circuit along with the rectifier.

9. peak inverse Voltage (PIV).

The PIV is the peak voltage across the diode in the reverse direction i.e when the diode is reverse biased. In half-wave rectifier, the load current is ideally zero. when the diode is reverse biased and hence the maximum value of the voltage that can exist across the diode is

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nothing but V_m. This is shown below

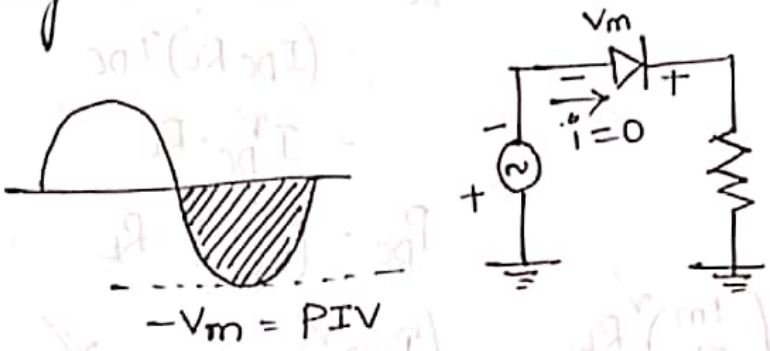

Fig: PIV rating of diode

PIV = Maxium value of secondary voltage = V_m

$\left(V_m = \pi V_{DC} \text{ (or) } \pi I_{DC}\right)$

Diode must be selected based on PIV rating and the circuit specifications.

10. Transformer utilization factor (T.U.F)

The factor which indicates how much is the utilization of the transformer in the circuit is called (T.U.F) Transformer utilization factor.

$$T.U.F = \frac{\text{D.c power delivered to the load}}{(\text{a.c power rating of the transformer})_{rated}}$$

Note :- While we are calculating a.c power rating it is necessary to consider r.m.s value of a.c voltage and current.

The A.C power rating of Transformer $= (V_{rms} \cdot I_{RMS})_{rated}$

Wher $(V_{rms})_{rated} = \frac{V_m}{\sqrt{2}}$ A.C power $= \frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{2}$

$(I_{rms})_{rated} = \frac{I_m}{2}$ $P_{AC} = \frac{V_m \cdot I_m}{2\sqrt{2}}$.

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D·C power delivered to load $P_{DC} = V_{DC} \cdot I_{DC}$

$= (I_{DC} R_L) I_{DC}$

$= I_{DC}^2 \cdot R_L$

$P_{DC} = \left(\frac{I_m}{\pi}\right)^2 \cdot R_L$

$$\therefore \text{TUF} = \frac{\left(\frac{I_m}{\pi}\right)^2 R_L}{\left(\frac{V_m I_m}{2\sqrt{2}}\right)} = \frac{\left(\frac{I_m}{\pi}\right)^2 R_L}{\left(\frac{I_m^2 R_L}{2\sqrt{2}}\right)} = \frac{I_m^2}{\pi^2} R_L \times \frac{2\sqrt{2}}{I_m^2 R_L}$$

$$= \frac{2\sqrt{2}}{\pi^2} = 0.287$$

$$\boxed{\text{T.U.F} = 0.287}$$

The value of TUF is low which shows that in half-wave circuit the transformer is not fully utilized.

11. Voltage Regulation :—

The secondary voltage should not change with respect to the load current. The voltage regulation is the factor which tells us about the change in the d·c output voltage as load changes from no load to full load condition

if $(V_{dc})_{NL}$ = D·C voltage on no load

$(V_{DC})_{FL}$ = D·C voltage on full load

$$\boxed{\text{Voltage Regulation} = \frac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}}}$$

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$$(V_{dc})_{NL} = \frac{V_m}{\pi}$$

$$(V_{dc})_{FL} = I_{DC} \cdot R_L = \frac{I_m}{\pi} \cdot R_L = \frac{V_m}{\pi(R_L + R_s + R_f)} \cdot R_L$$

$$\%R = \frac{\frac{V_m}{\pi} - \frac{V_m}{\pi} \cdot \frac{R_L}{R_L + R_s + R_f}}{\frac{V_m}{\pi} * \frac{R_L}{R_f + R_s + R_L}}$$

$$\%R = \frac{\frac{V_m}{\pi}\left(1 - \frac{R_L}{R_L + R_s + R_f}\right)}{\frac{V_m}{\pi} \times \frac{R_L}{R_L + R_s + R_f}} = \frac{1 - \frac{R_L}{R_L + R_s + R_f}}{\frac{R_L}{R_L + R_s + R_f}}$$

$$\%R = \frac{R_f + R_s}{R_L} \times 100$$

Neglecting winding resistance

$$\%R = \frac{R_f}{R_L} \times 100$$

Less the value of Voltage regulation, better is the performance of rectifier circuit.

Disadvantages of Half-wave rectifier circuit :—

* The ripple factor of HWR is 1.21 which is quite high.
* Rectification Efficiency is 40% – it indicates the HWR is quite inefficient.
* The circuit has low transformer utilization factor shows that transformer not fully utilized
* DC current is flowing through the secondary winding of the transformer which may cause dc saturation of the core of transformer.

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To minimize this transformer size have to be increased accordingly. This increases the cost.

Because of all these disadvantages, the half wave rectifier circuit is normally not used as a power rectifier circuit.

FULL WAVE RECTIFIER :—

The Full wave rectifier conducts during both positive and negative half-cycles of input a.c supply. In order to rectify both the half-cycles of a.c input, two diodes are used in this circuit. The diodes feed a common load R_L with the help of a Centre tap transformer. The a.c voltage is applied through a suitable power transformer with proper turns ratio.

The full wave rectifier circuit is as shown below. for the proper operation of the circuit, a Centre-tap-transformer is essential.

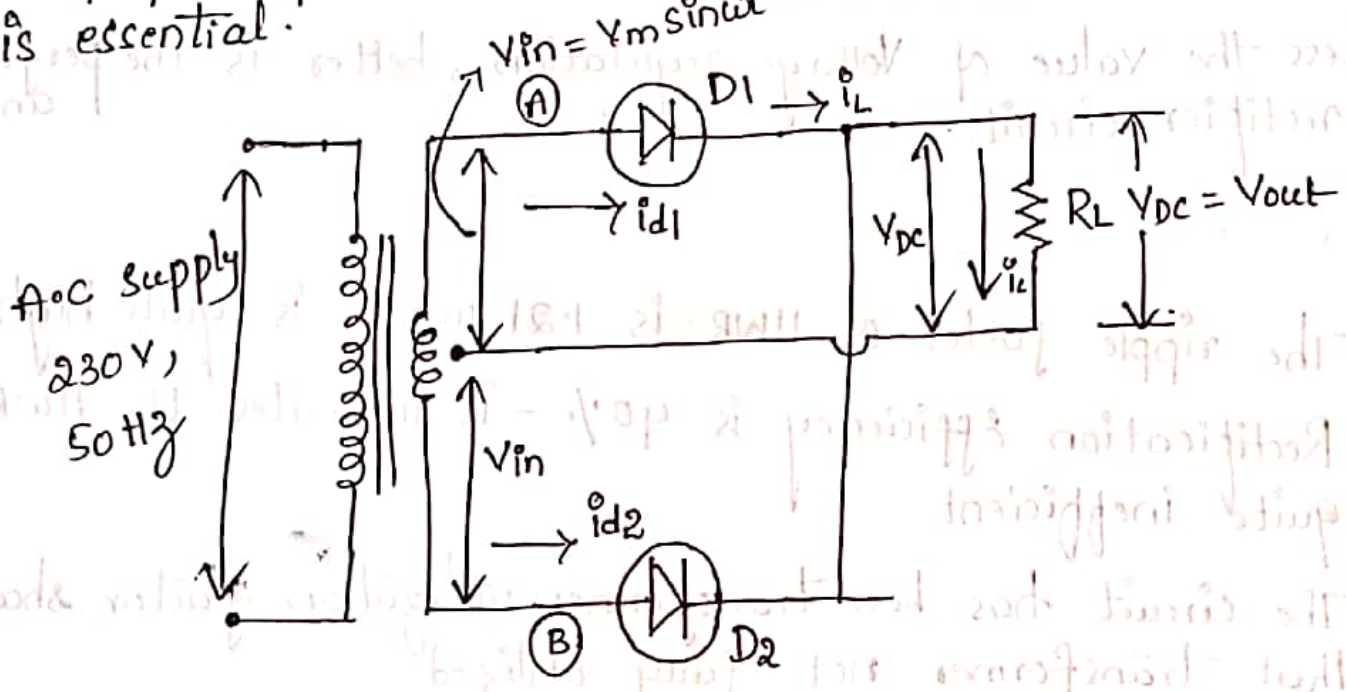

fig :- Full-wave rectifier

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The Diode D_2 supplies the load current $i_L = i_{d2}$. Now lower half of secondary winding carries the current but the upper half does not.

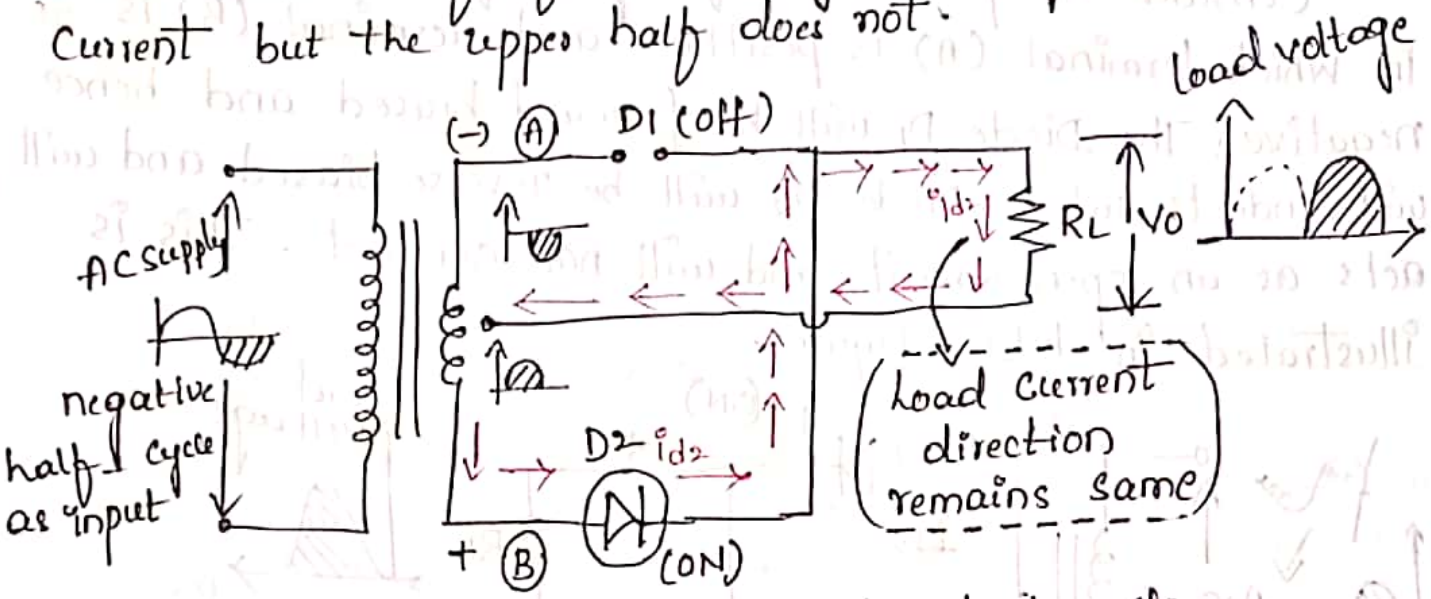

Fig :- Current flow during negative half cycle

∴ The load current flows in both the half-cycle of a.c voltage and in the same direction through the load-resistance. But the output load current/voltage is still pulsating d.c not pure d.c

characteristics of fullwave rectifier :—

1. Maximum load current
2. Average D.C load Current (I_{DC})
3. Average D.C load voltage (V_{DC})
4. R.M.S load Current (I_{rms})
5. R.M.S load voltage (V_{rms})
6. D.C power output (P_{DC})
7. A.C power input (P_{AC})
8. Rectifier Efficiency (η)
9. Ripple factor (γ)
10. load current
11. peak inverse voltage
12. TUF
13. voltage regulation.

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Operation :-

case 1:- Consider the positive half-cycle of a.c input voltage in which terminal (A) is positive and terminal (B) is negative. The Diode D_1 will be forward biased and hence will conduct, while Diode D_2 will be reverse biased and will acts as an open circuit and will not conduct. This is illustrated in below figure.

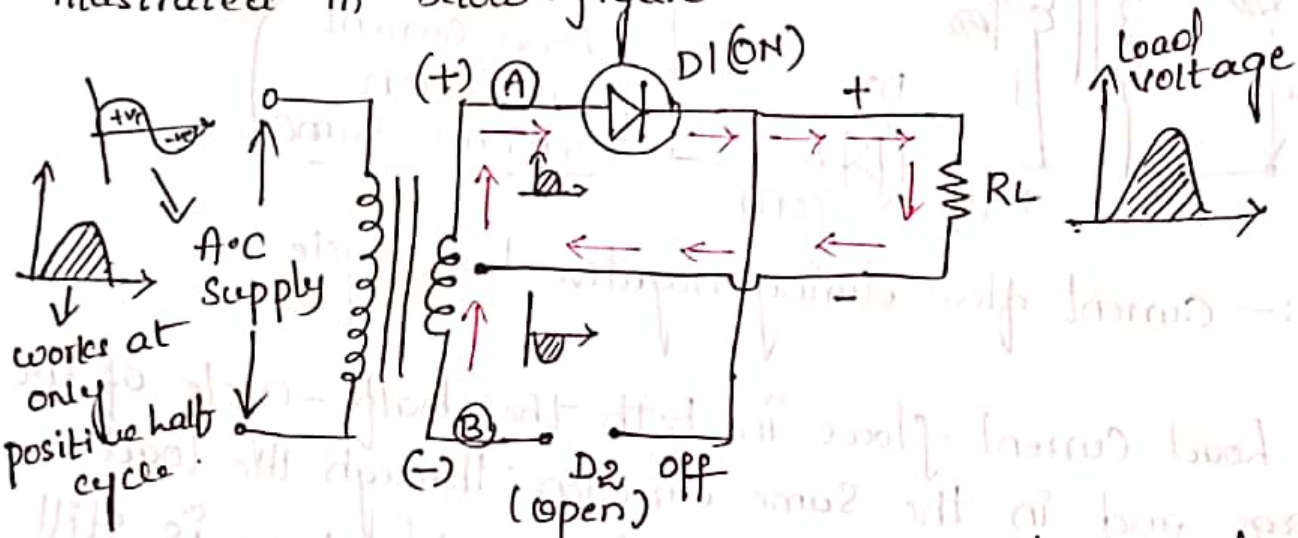

Fig :- Current flow during positive half cycle.

The Diode D_1 supplies the load current $i_L = i_{d1}$. This current is flowing through the upper half of Secondary winding while the lower half of secondary winding of the transformer carriers no current.

case 2 :- During negative half cycle

In the next half cycle of a.c voltage, polarity reverse and terminal (A) becomes negative, B becomes positive. The Diode D_2 conducts being forward biased. while D_1 does not conduct, it is reverse biased replaced by the open circuit.

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1. Maximum load Current :-

R_f = forward resistance of diodes

R_s = Winding resistance of each half of secondary

R_L = load resistance

V_{in} = Instantaneous a.c voltage across each half of secondary.

$V_{in} = V_m \sin\omega t$ → interms of voltage (maximum load voltage)

$I_{in} = I_m \sin\omega t$ → (Maximum load current - Im)

I_m = Maximum value of a.c input voltage across each half of secondary winding = $\frac{V_m}{R_s + R_f + R_L}$.

The Output Wave form of Full wave rectifier circuit.

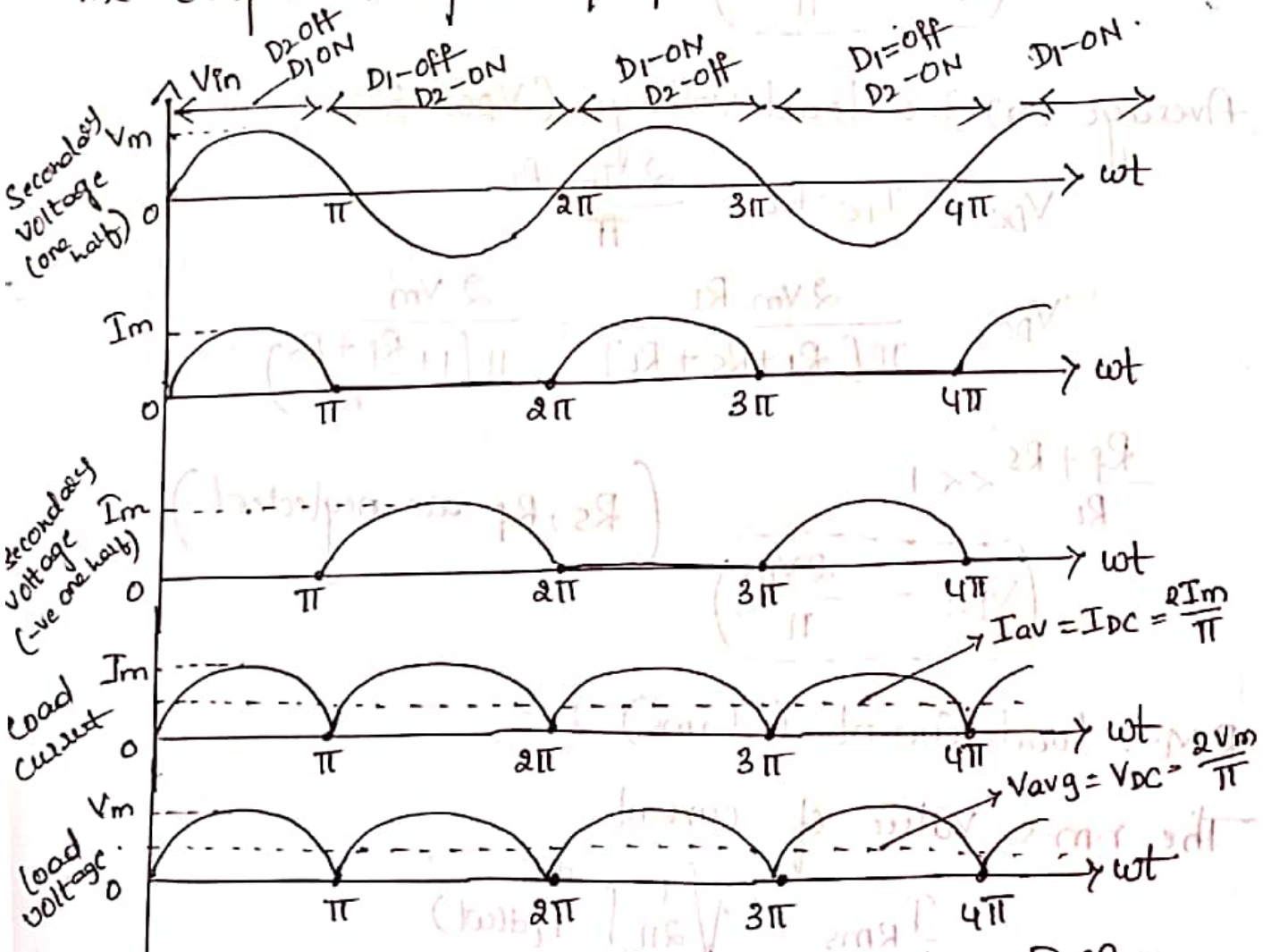

Fig:- load Current and load voltage for FWR.

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2. Average (or) DC Current :-

Consider one cycle of the load current i_L from 0 to π, to obtain the average value which is d.c value of load current

$$i_L = I_m \sin\omega t \quad -0 \le \omega t \le \pi$$

$$I_{avg} \text{ or } I_{DC} = \frac{1}{\pi}\int_0^{\pi} i_L \, d(\omega t) = \frac{1}{\pi}\int_0^{\pi} I_m \sin\omega t \cdot d\omega t$$

$$= \frac{I_m}{\pi}\left[(-\cos\omega t)_0^{\pi}\right)$$

$$= \frac{I_m}{\pi}\left(-\cos\pi - (-\cos 0)\right)$$

$$= \frac{I_m}{\pi}\left(+1-(-1)\right)$$

$$\boxed{I_{DC} = \frac{2I_m}{\pi}}$$

3. Average (or) D.C load voltage (V_{DC}) :-

$$V_{DC} = I_{DC} \cdot R_L = \frac{2I_m \cdot R_L}{\pi}$$

$$V_{DC} = \frac{2V_m \cdot R_L}{\pi\left[R_L + R_S + R_L\right]} = \frac{2V_m}{\pi\left(1 + \frac{R_f + R_S}{R_L}\right)}$$

$\frac{R_f + R_S}{R_L} << 1$ (R_S, R_f are neglected)

$$\boxed{V_{DC} = \frac{2V_m}{\pi}}$$

4. R.M.S load Current (I_{rms}) :-

The r.m.s value of current

$$I_{Rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_L^2 \, d(\omega t)}$$

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$$I_{R.M.S} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} (I_m \sin\omega t)^2 d(\omega t)}$$

$$= I_m \sqrt{\frac{1}{\pi}\int_0^{\pi} \left(\frac{1-\cos 2\omega t}{2}\right) d\omega t}$$

$$= I_m \sqrt{\frac{1}{2\pi}\left[(\omega t)_0^{\pi} - \left(\frac{\sin 2\omega t}{2}\right)_0^{\pi}\right]}$$

(as $\sin 2\pi = \sin(0) = 0$)

$$= I_m \sqrt{\frac{1}{2\pi}(\pi - 0)}$$

$$= I_m \sqrt{\frac{1}{2\pi}\pi} = \frac{I_m}{\sqrt{2}}$$

$$\boxed{I_{R.M.S} = \frac{I_m}{\sqrt{2}}}$$

5. R.M.S Value of load voltage Current :—

$$V_{R.M.S} = I_{R.M.S} \times R_L$$

$$= \frac{I_m}{\sqrt{2}} \times R_L$$

$$V_{R.M.S} = \frac{V_m}{\sqrt{2} \cdot R_L} \times R_L = \frac{I_m}{\sqrt{2}}$$

$$\boxed{V_{R.M.S} = \frac{V_m}{\sqrt{2}}}$$

6. D.C power output :— (P_{DC})

D.C power output = $V_{DC} \cdot I_{DC} = I_{DC}^2 \cdot R_L$

$$P_{DC} = I_{DC}^2 \cdot R_L = \left(\frac{2I_m}{\pi}\right)^2 R_L$$

$$P_{DC} = \frac{4}{\pi^2} I_m^2 R_L$$

Sub Value of I_m we get.

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$$\left(P_{DC} = \frac{4}{\pi^2} \frac{V_m^2}{(R_s + R_f + R_L)^2} \times R_L\right)$$

7). A.C power input ($P_{A.C}$) :—

$$P_{A.C} = I_{rms}^2 (R_s + R_f + R_L) = \left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f + R_s + R_L)$$

$$P_{A.C} = \frac{I_m^2 (R_f + R_s + R_L)}{2}$$

Sub value of I_m we get,

$$P_{AC} = \frac{V_m^2}{(R_f + R_s + R_L)^2} \times \frac{1}{2} \times (R_f + R_s + R_L)$$

$$P_{AC} = \frac{V_m^2}{2(R_f + R_s + R_L)}$$

8. Rectifier Efficiency :—

$$\eta = \frac{P_{DC\ output}}{P_{AC\ input}} = \frac{4/\pi^2 \cdot I_m^2 R_L}{\frac{I_m^2 (R_f + R_s + R_L)}{2}} = \frac{8 R_L}{\pi^2 (R_f + R_s + R_L)}$$

$$\eta = \frac{8 R_L}{\pi^2 (R_L)} = \frac{8}{\pi^2} = 0.812.$$

$$\%.\eta = 0.812 \times 100 = 81.2\ \%$$

$$\left(\%.\eta = 81.2\ \%\right)$$

Maximum theoretical Efficiency of FWR = 0.812
= 81.2 %.

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9). Ripple factor :-

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} \quad \left(\because I_{rms} = \frac{I_m}{\sqrt{2}},\ I_{DC} = \frac{2I_m}{\pi}\right)$$

$$= \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1} = 0.48$$

$$(\gamma = 48\%)$$

10). Load Current (i_L) :-

The Fourier Series for the load current is obtained by taking the sum of the series for the individual rectifier current. The two diodes conduct in alternate half cycles i.e current. Hence there is phase difference of π radians between two diodes current. Hence,

$$i_{d1} = I_m\left[\frac{1}{\pi} + \frac{1}{2}\sin\omega t - \frac{2}{3\pi}\cos 2\omega t - \frac{2}{15\pi}\cos 4\omega t \cdots\right]$$

i_{d2} = i_{d1} with ωt replaced by $(\omega t + \pi)$

$$i_{d2} = I_m\left[\frac{1}{\pi} + \frac{1}{2}\sin(\omega t+\pi) - \frac{2}{3\pi}\cos 2(\omega t+\pi) - \frac{2}{15\pi}\cos 4(\omega t+\pi) \cdots\right]$$

$$= I_m\left[\frac{1}{\pi} - \frac{1}{2}\sin\omega t - \frac{2}{3\pi}\cos(2\omega t + 2\pi) - \frac{2}{15\pi}\cos(4\omega t + 4\pi) + \cdots\right]$$

$$= I_m\left[\frac{1}{\pi} - \frac{1}{2}\sin\omega t - \frac{2}{3\pi}\cos 2\omega t - \frac{2}{15\pi}\cos 4\omega t \cdots\right]$$

Then the fourier Series for the load current is,

$$i_L = i_{d1} + i_{d2}$$

$$i_L = I_m\left[\underbrace{\frac{2}{\pi}}_{\text{d.c component}} \underbrace{- \frac{4}{3\pi}\cos 2\omega t - \frac{4}{15\pi}\cos 4\omega t \cdots}_{\text{a.c (or) ripples}}\right].$$

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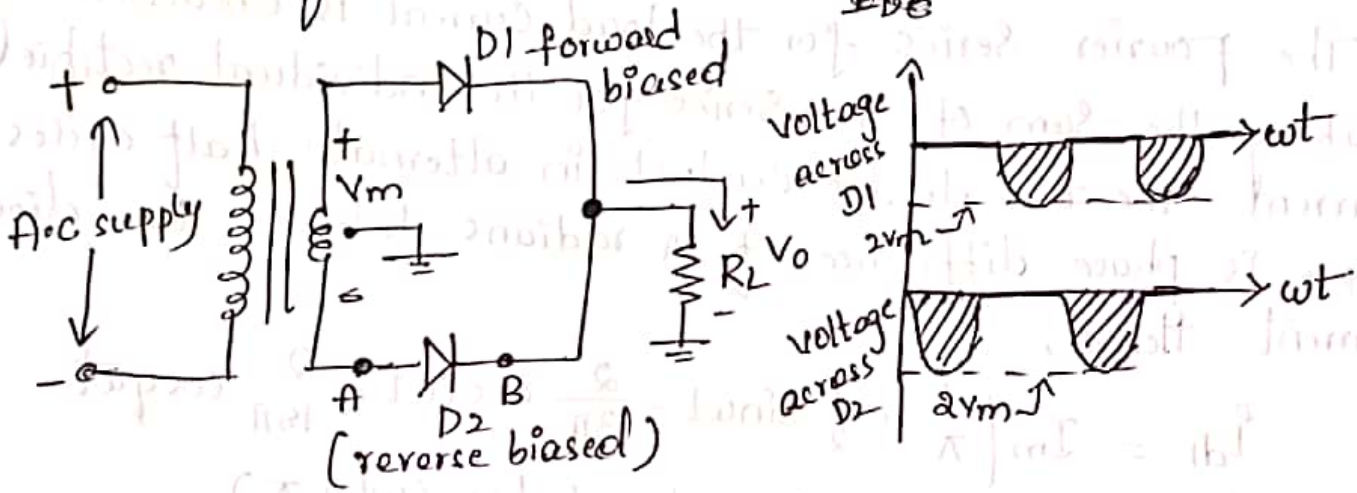
$$i_{secondary} = i_{d1} - i_{d2}$$

$$\therefore \quad i_{secondary} = I_m \sin\omega t \;//$$

11. Peak inverse voltage :-

the Maximum reverse voltage the diode can be withstand without damaging the junction of diode.

$$PIV \text{ of diode} = 2V_m = \frac{\pi V_{DC}}{\cancel{I_{DC}}} \text{ (or) } \pi I_{DC} \;//$$



$$\boxed{PIV = 2V_m}$$

if diode drop is considered to be 0.7V then

$$\boxed{PIV = 2V_m - 0.7}$$

12. Transformer utilization factor :- (T.U.F)

$$T.U.F = \frac{\text{D.C power to the load}}{\text{A.C power rating of secondary}}$$

$$= \frac{I_{DC}^2 \cdot R_L}{V_{rms} \cdot I_{rms}} = \frac{\left(\frac{2I_m}{\pi}\right)^2 R_L}{\frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}}$$

Neglecting forward & Secondary resistance R_f & R_s.

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$V_m = I_m R_L$

$$(TUF)_{sec} = \frac{4/\pi^2 \times I_m^2 R_L}{\frac{I_m^2 R_L}{2}} = \frac{8}{\pi^2} = 0.812$$

∴ The primary of the transformer is feeding two half wave rectifiers separately. These two half-wave rectifiers work independently of each other but feed a common load.

T·U·F for primary winding = 2 × T·U·F for secondary

$$= \frac{0.574 + 0.812}{2}$$

$$= 0.693$$

Average T·U·F for full-wave rectifier = 0.693

(T·U·F = 0.693)

13. Voltage Regulation :—

$$(V_{dc})_{NL} = \frac{2V_m}{\pi}, \quad (V_{dc})_{FL} = I_{DC} \cdot R_L$$

$$\%R = \frac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}} \times 100$$

$$= \frac{\frac{2V_m}{\pi} - I_{DC} R_L}{I_{DC} R_L} \times 100$$

$$\%R = \frac{2V_m/\pi - I_{DC} R_L}{I_{DC} R_L} \times 100$$

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$$I_m = \frac{V_m}{R_f + R_s + R_L}$$

$$V_m = I_m(R_f + R_s + R_L)$$

$$I_{DC} = \frac{2I_m}{\pi}$$

$$\% R = \frac{\frac{2I_m}{\pi}(R_f + R_s + R_L) - \frac{2I_m}{\pi} R_L}{\frac{2I_m}{\pi} \times R_L} \times 100$$

$$= \frac{R_f + R_s + R_L - R_L}{R_L} \times 100$$

$$\% R = \frac{R_f + R_s}{R_L} \times 100$$

Neglecting winding resistance R_s, the regulation can be expressed as,

$$\left(\% R = \frac{R_f}{R_L} \times 100\right)$$

Where R_f = Forward resistance of the diode.

Advantages of full wave rectifier :—

* The D.C load voltage and current are more than half-wave.
* No D.C current through transformer windings hence no possibility of saturation.
* TUF is better as transformer losses are less.
* Efficiency is higher
* large d.c power output
* The ripple factor is less.

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Disadvantages of Full wave rectifier :—

* The PIV rating of diode is higher
* Higher PIV dioder are larger in size and costlier.
* The cost of centre tap transformer is higher.

BRIDGE RECTIFIER :—

The Bridge rectifier Circuit are mainly used as,

a). The power rectifier circuit for Converting a·c power to d·c power.

b). A rectifying system in rectifier type a·c meters, such as a·c voltmeter, in which the a·c voltage under measurement in first converted into d·c and measured with conventional meter. In this system, the rectifying elements are either Copper oxide type or Selenium type.

The Basic Bridge rectifier circuit is shown below

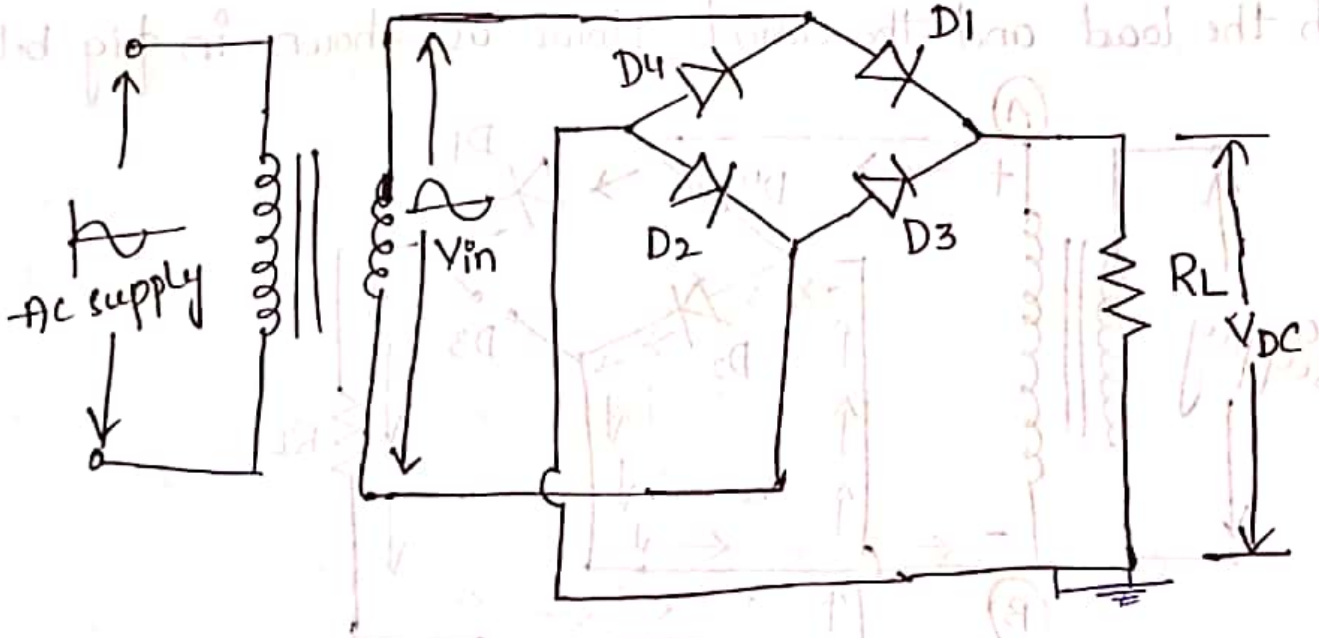

Fig:- Bridge rectifier Circuit.

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The bridge rectifier circuit is essentially a full-wave rectifier circuit, using 4 diodes forming the 4 arms of an electrical bridge. To one diagonal of the bridge the a.c voltage is applied through a transformer if necessary, and the rectified d.c voltage is taken from the other diagonal of the bridge.

The main advantage of the circuit is that it does not require a centre tap transformer on the secondary winding. Hence wherever possible a.c voltage can be directly applied to the bridge.

Operation :—

Consider the positive half cycle of ac input voltage The point A of secondary becomes positive. The diodes D_1 and D_2 will be forward biased, while D_3 and D_4 reverse biased. The two diodes D_1, D_2 conduct in series with the load and the current flows as shown in fig below.

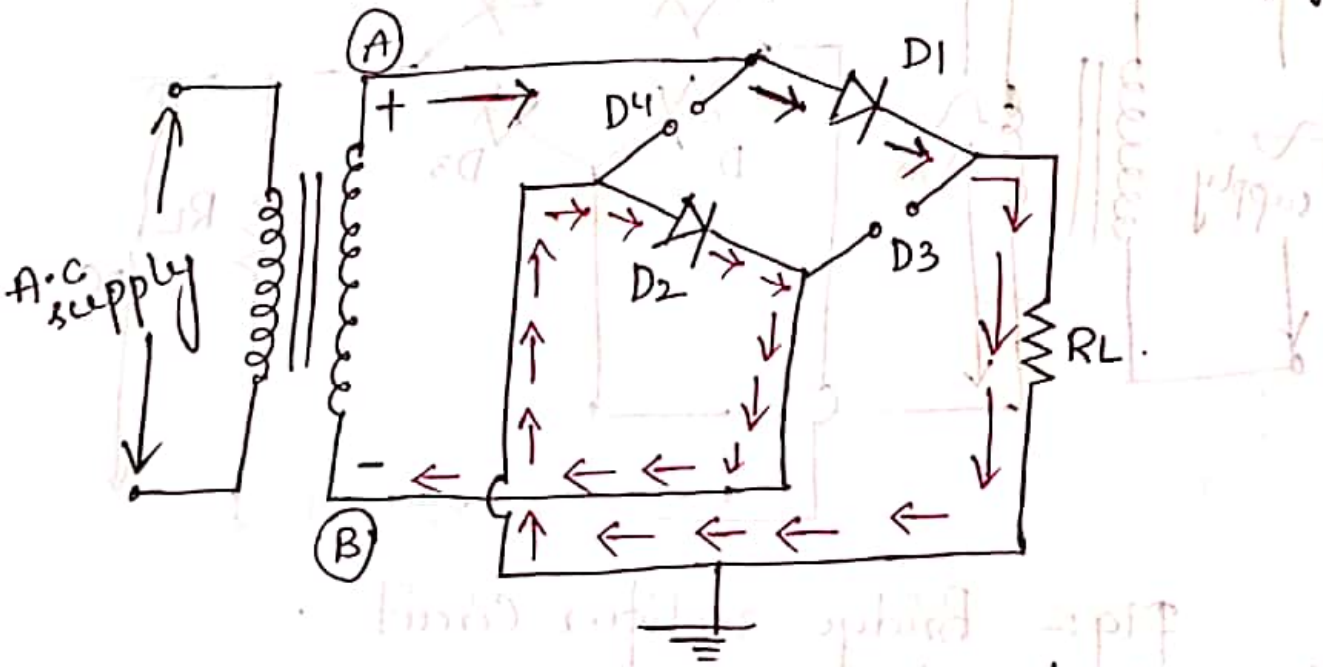

Fig: Current flow during positive half-cycle.

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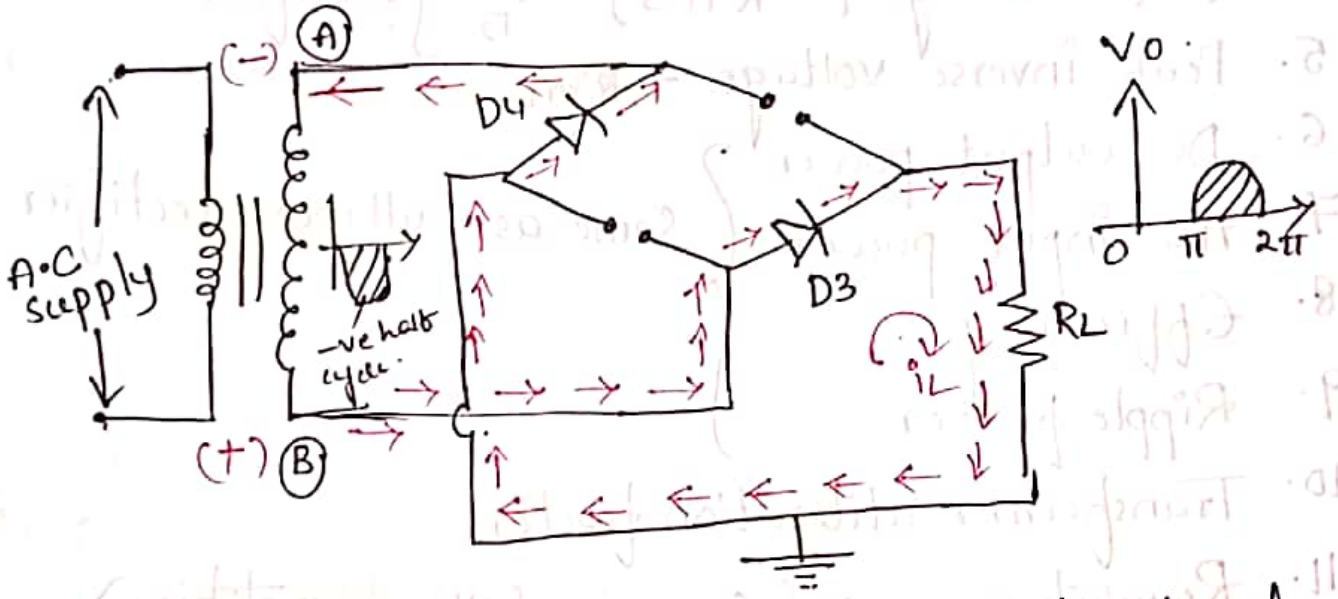
In the next half-cycle, when the polarity of a.c voltage reverses hence point B becomes positive diodes D_3 and D_4 are forward biased, while D_1 and D_2 reverse biased. Now the diodes D_3 and D_4 conduct is series with the load and the current flows as shown in below



It is seen that in both cycles of a.c the load current is flowing in the same direction hence, we get a full-wave rectified output.

The output waveforms of Bridge rectifier :—

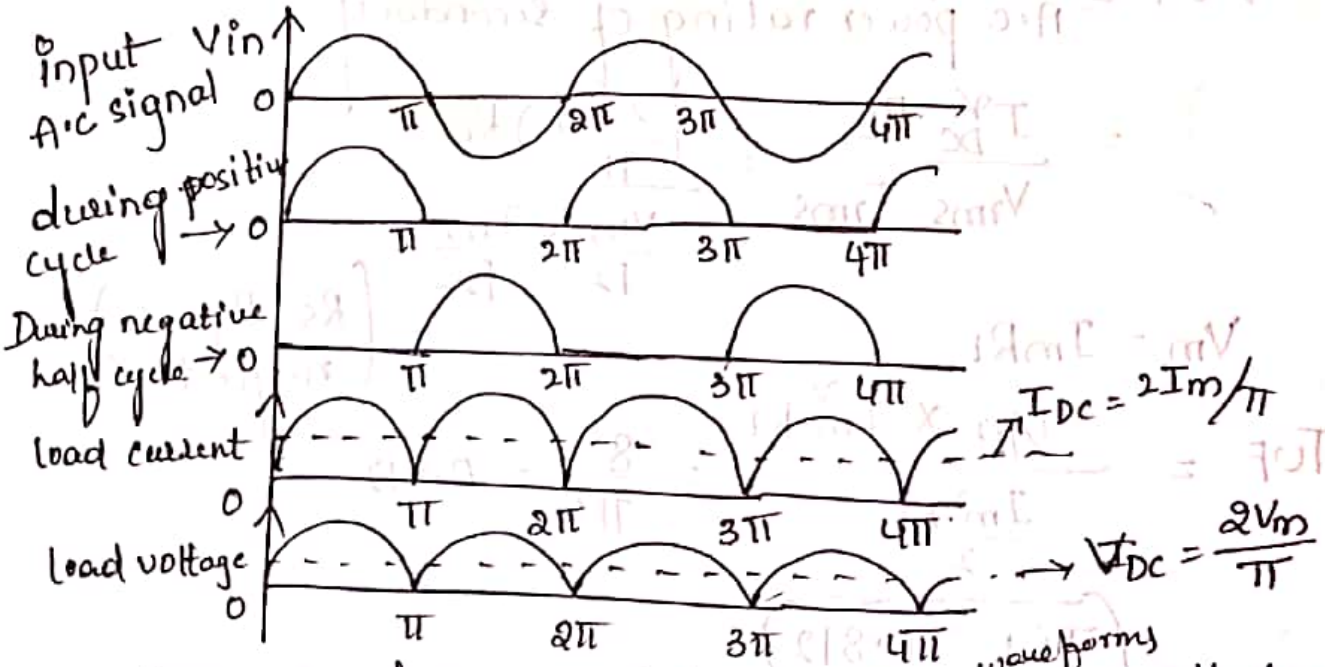


Fig:- Load current & load voltage waveforms for Bridge rectifier

Characteristics of Bridge rectifier :-

1. Average (or) DC current $-\frac{2I_m}{\pi}$ } Same as Full-wave rectifier
2. Average (or) DC voltage $-\frac{2V_m}{\pi}$ }
3. R.M.S current ($I_{R.M.S}$) $-\frac{V_m}{\sqrt{2}}$ } Same as full wave rectifier
4. R.M.S Voltage ($V_{R.M.S}$) $-\frac{V_m}{\sqrt{2}}$ }
5. Peak inverse voltage $- 2V_m$
6. DC output power } Same as Full wave rectifier.
7. AC input power
8. Efficiency
9. Ripple factor
10. Transformer utilization factor
11. Regulation $\longrightarrow$ (Same as full wave rectifier).
12. Forward resistance.

(10). Transformer utilization factor :-

$$T.U.F = \frac{\text{D.C power to the load}}{\text{A.C power rating of secondary}}.$$

$$= \frac{I_{DC}^2 \cdot R_L}{V_{rms} \cdot I_{rms}} = \frac{\left(\frac{2I_m}{\pi}\right)^2 R_L}{\frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}}$$

$(R_s = R_f = 0$ neglect$)$.

$V_m = I_m R_L$

$$TUF = \frac{4/\pi^2 \times I_m^2 R_L}{\frac{I_m^2 R_L}{2}} = \frac{8}{\pi^2} = 0.812$$

$(TUF = 0.812)$

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* DC current $I_{DC} = \frac{2I_m}{\pi}$
* DC voltage $V_{DC} = \frac{2V_m}{\pi}$
* R.M.S current $I_{R.M.S} = \frac{I_m}{\sqrt{2}}$
* R.M.S voltage $V_{R.m.s} = \frac{V_m}{\sqrt{2}}$
* Forward resistance is $R_f + R_f = 2R_f$
  (because at a time two diodes are conduct. so two forward resistance occur).
* $I_m = \frac{V_m}{R_s + 2R_f + R_L}$
* $P_{DC} = I_{DC}^2 R_L = \frac{4}{\pi^2} I_m^2 \cdot R_L$
* $P_{AC} = I_{RMS}^2 (R_s + 2R_f + R_L)$
  $= \frac{I_m^2 (2R_f + R_s + R_L)}{2}$
* Efficiency $\eta = \frac{8R_L}{\pi^2 (R_s + 2R_f + R_L)}$
  $\%\eta = 81.2\%$
* Ripple factor $\gamma = 0.48$.
* peak inverse voltage is V_m.

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Advantages of Bridge rectifier :-

* No centre tap transformer is required. Hence, whenever possible a.c voltage can directly be applied to the bridge.
* As two diodes conduct in Series in each half-cycle, inverse voltage appearing across diodes get shared. Hence the circuit can be used for high voltage applications. Such a peak reverse voltage appearing across diode is called peak inverse voltage rating (PIV) of diode.

Disadvantages :-

The only disadvantage of Bridge rectifier is the use of four diodes as compared to two diodes in normal full wave rectifier. This causes additional voltage drop as indicated by term $2R_f$ present in expression of I_m instead of R_f. This reduces the output voltage.

Applications :-

* Used as rectifier in power circuits to convert a.c to d.c
* In rectifier type meters, to convert a.c voltage to be measured to d.c
* In power supply circuits.

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Comparison of FWR with Bridge rectifier :—

Full-wave rectifier (FWR using two Diodes)	Bridge rectifier (FWR using 4 (four) diodes)
1. It uses centre tapped transformer.	1. It does not use centre tapped transformer.
2. One Diode conducts in each half cycle of input	2. Two diodes conduct in each half cycle of input
3. The voltage drop across the diode is due to R_f only	3. The voltage drop across the load diodes is due to $2R_f$
4. The output voltage is more	4. The output voltage is less
5. The transformer is less effectively used	5. The Transformer is used more Effectively.
6. T.U.F is 0.693	6. T.U.F is 0.812
7. PIV rating of the Diode is $2V_m$	7. The PIV rating of the diode is V_m.

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Comparison of Rectifier Circuits

S.NO	parameter	Half-wave rectifier	Full-wave rectifier	Bridge rectifier
1.	Number of Diodes	1	2	4
2.	Average D.C current (I_{DC})	$\frac{I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{2I_m}{\pi}$
3.	Average D.C voltage (V_{DC})	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$	$\frac{2V_m}{\pi}$
4.	R.M.S current	$\frac{I_m}{2}$	$\frac{I_m}{2}$	$\frac{I_m}{2}$
5.	R.M.S voltage	$\frac{V_m}{2}$	$\frac{V_m}{2}$	$\frac{V_m}{2}$
6.	Dc output power (P_{DC})	$\frac{I_m^2 R_L}{\pi^2}$	$\frac{4}{\pi^2} I_m^2 R_L$	$\frac{4}{\pi^2} I_m^2 R_L$
7.	A.C input power (P_{AC})	$\frac{I_m^2 (R_L + R_f + R_s)}{4}$	$\frac{I_m^2 (2R_f + R_s + R_L)}{2}$	$\frac{I_m^2 (2R_f + R_s + R_L)}{2}$
8.	Maximum rectifier efficiency (η)	40.6%	81.2%	81.2%
9.	Ripple factor (γ)	1.21	0.482	0.482
10.	Maximum load current (I_m).	$\frac{V_m}{R_s + R_f + R_L}$	$\frac{V_m}{R_s + R_f + R_L}$	$\frac{V_m}{R_s + 2R_f + R_L}$
11.	PIV	V_m	$2V_m$	V_m
12.	Ripple frequency	50Hz	100Hz	100Hz.
13.	T.U.F	0.287	0.693	0.812.

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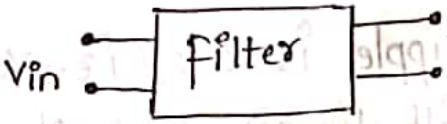
2(B) - FILTERS

Filter :- Filters are used to minimise the undesirable ac i.e ripples (unwanted particles). It is an electronic-circuit composed of capacitor-Inductor or Combination of both and connected between the rectifier and load to Convert pulsating d.c to pure d.c



Need of Filters :-

It is seen that the output of a half-wave or full wave rectifier circuits is not pure d.c but it contains ripples or undesired components. To minimize the ripple content in the output, filter circuits are used. These circuits are connected between the rectifier and load.

Block diagram of filter :-

Block diagram for filter is as shown below :-

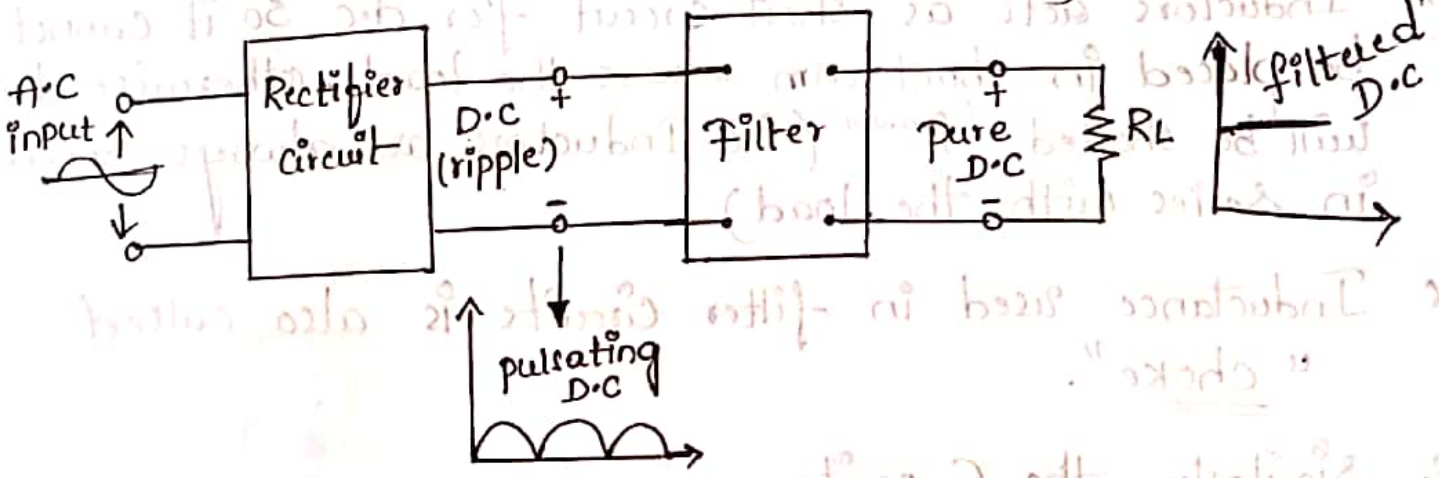


Fig :- power Supply using Rectifier and filter.

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An a.c input is applied to the rectifier. At the output of the rectifier, there will be d.c and ripple voltage present, which is the input to the filter. Ideally the output of the filter should be pure d.c. practically, the filter circuit will try to minimize the ripple at the output as far as possible.

Basically the ripple is a.c (i.e., varying with time) while D.C (i.e not varying with time) is constant. Hence in order to separate d.c from ripple, the filter circuit should use components which have widely different impedance for a.c and D.C. Two such components are

* Capacitors
* Inductors

* Ideally, Inductors acts as short circuit for d.c but it has large impedance for a.c
* Capacitors acts as short circuit for a.c but it has large impedance for d.c.
* Inductors acts as short circuit for d.c so it cannot be placed in shunt arm across the load, otherwise d.c will be shorted. (parallel) (i.e Inductors are always connected in series with the load).
* Inductance used in filter circuits is also called "choke".
* Similarly, the Capacitance is open for d.c i.e it blocks d.c; hence it cannot be connected in series with the load.

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Types of filter circuits :-

There are basically four types of filter circuits,

1. Capacitor filter (C-Filter)
2. Inductor filter / choke input filter (L-filter)
3. LC filter / L-section filter
4. CLC filter / π-section filter

Looking from the rectifier side, if the first element in the filter is Capacitor then it is called "Capacitor filter" while if the first element is an inductor, it is called "Inductor filter" (or) choke input filter. The Inductor filter is not use nowadays as inductors are bulky, expensive and Consume more power.

①. Capacitor filter :-

The block schematic of Capacitor input filter is shown below. Looking from the rectifier side the first element in filter is a "Capacitor".

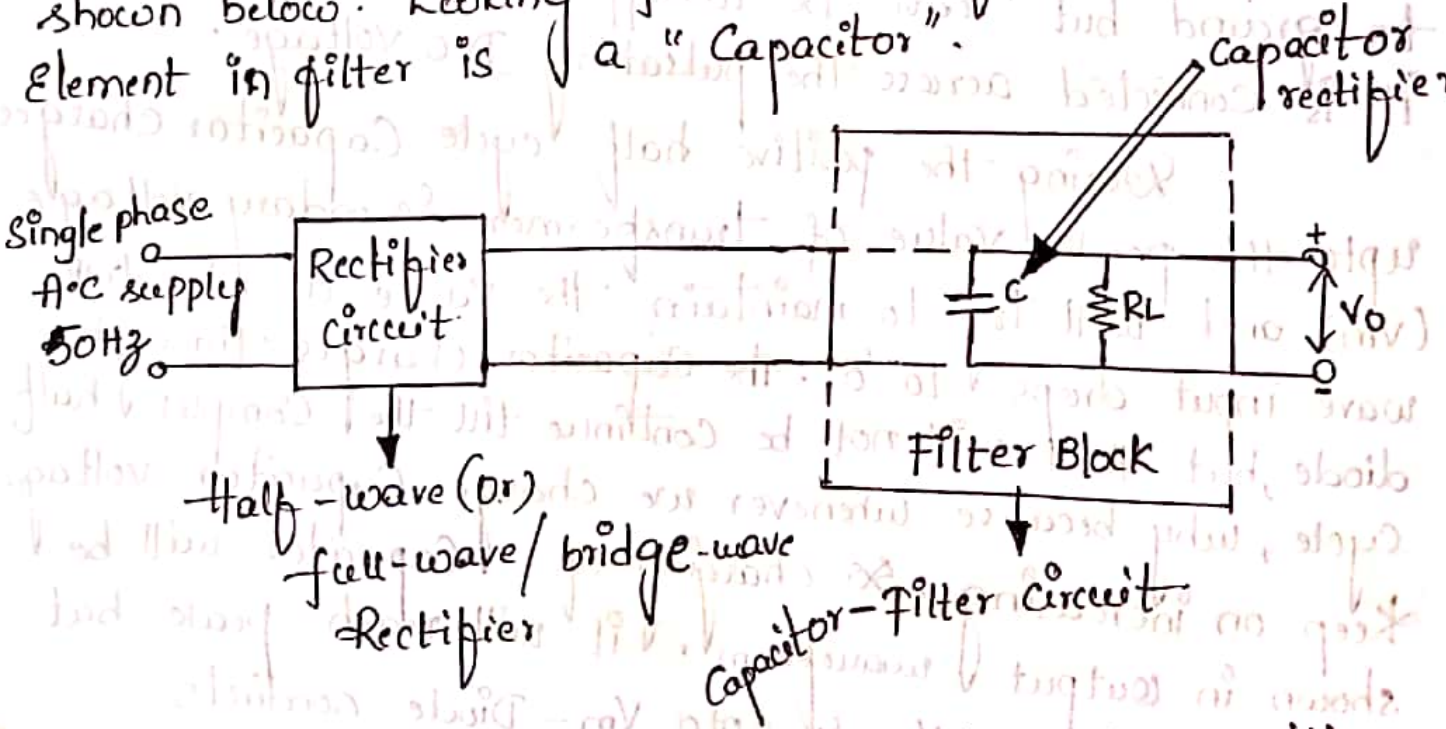

fig :- Block diagram for Capacitor filter with Connection of Rectifier output.

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The amount of ripple present in a full wave rectifier is 48%. This is not sufficient, further more reduction of ripple is required. To do this filters are used. One of the most "inexpensive" filter is "Capacitor filter". The capacitor filter can be directly connected to rectifier output.

The filter part of the circuit is as shown below:

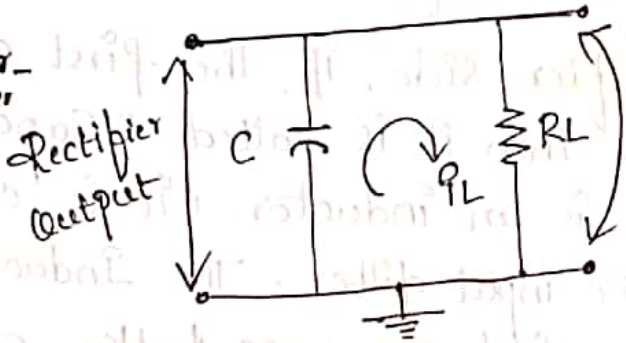

fig: Capacitor-filter

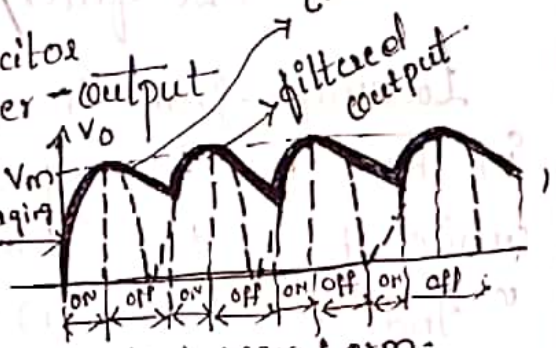

fig: output waveform.

Operation :-

The property of the Capacitor is that it allows A.C Components and it blocks D.C Component. The operation of Capacitor filter is to short the ripple to ground but leave DC to appear at the output when it is connected across the pulsating D.C voltage.

During the positive half cycle Capacitor charges upto the peak value of transformer Secondary voltage (Vm) and will try to maintain the value as the full wave input drops to '0'. The Capacitor charges through diode, but that will not be continue till the Complete half cycle, why because whenever we charge Capacitor voltage keep on increasing, so charging of Capacitor will be shown in output waveform. It will reach peak but not going to afta Vm so upto Vm - Diode conducts.

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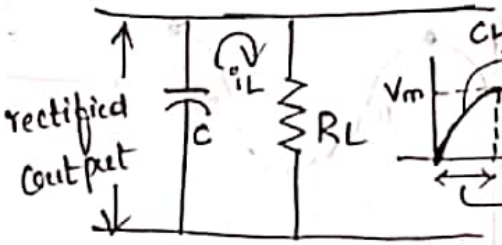
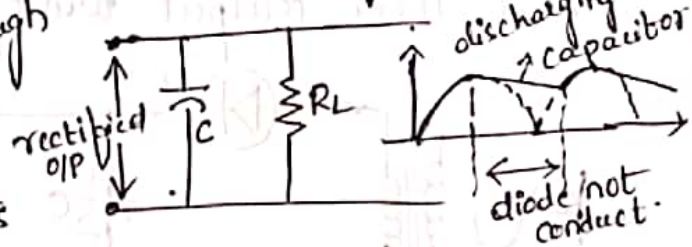
After the peak value, the capacitor discharges (diode is in Reverse-bias).



Charging - Capacitor



Discharging - Capacitor

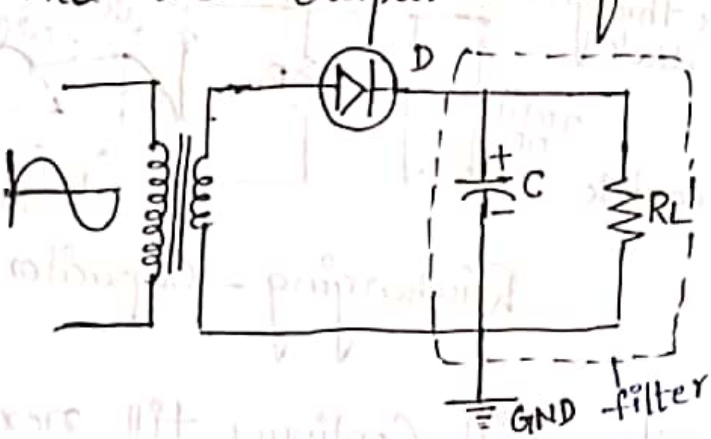
The discharging of capacitor will continues till next half cycle. The discharging time of capacitor is very high i.e., finally conclude that supply voltage is more than Capacitor voltage, the Capacitor charging through diode start to i.e in forward bias condition. if supply voltage is less than diode Capacitor voltage, the Capacitor starts to decreasing / Discharging current (or) voltage through diode i.e in reverse-bias condition.

(i) $V_{in} > V_\gamma$ (Charging) → Diode conducts, when applied input voltage is more than Capacitor voltage (or) diode voltage, the diode conducts. This voltage is called as "Cut-in-voltage".

(ii) $V_{in} < V_\gamma$ (Discharging) → when applied voltage is less than diode voltage, diode doesn't conduct - This voltage is called as "Cut-out-Voltage".

* The Ripple voltage waveform can be assumed as triangular from Cut-in-point to cut-out-point. Whatever charge the Capacitor acquires is equal to charge of capacitor has lost during non-conducting

filter circuit for Halfwave rectifier and full-wave rectifier and their output waveforms are shown below :



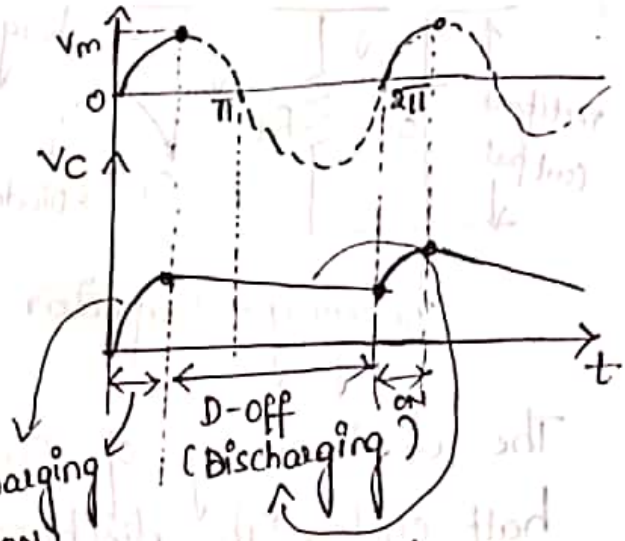
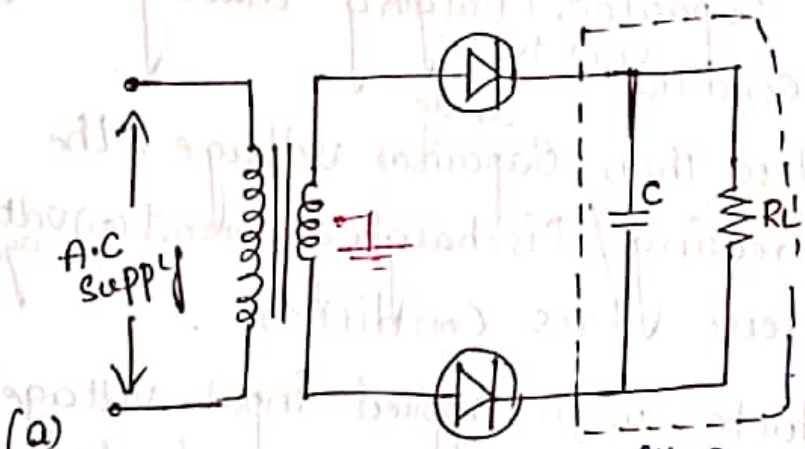
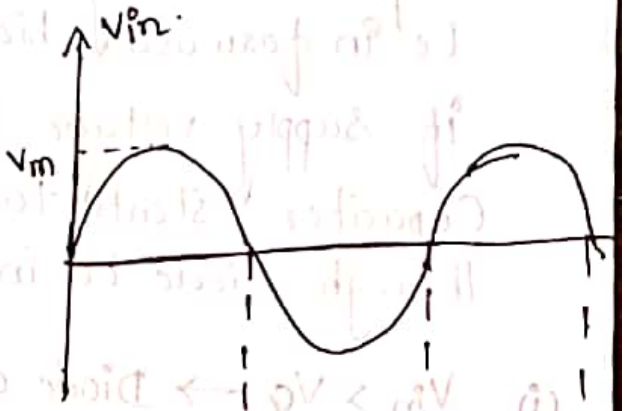


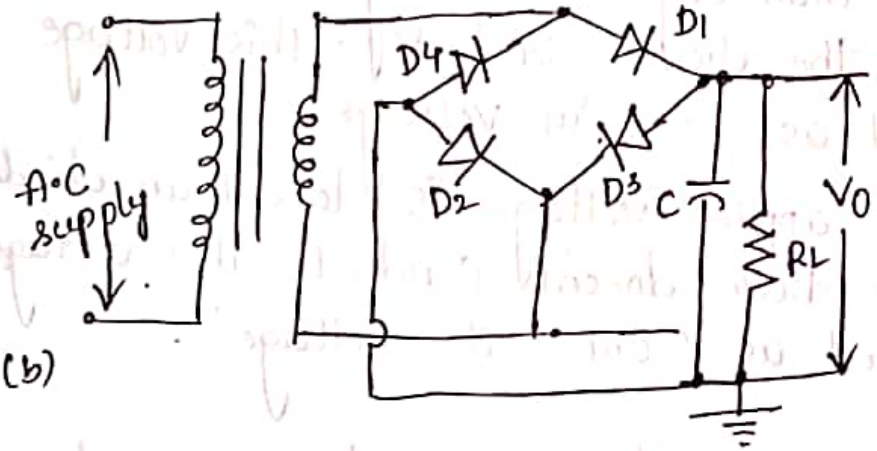
fig: Filter circuit for Half-wave rectifier

(Capacitor discharges during negative half cycle).



(a)





(b)

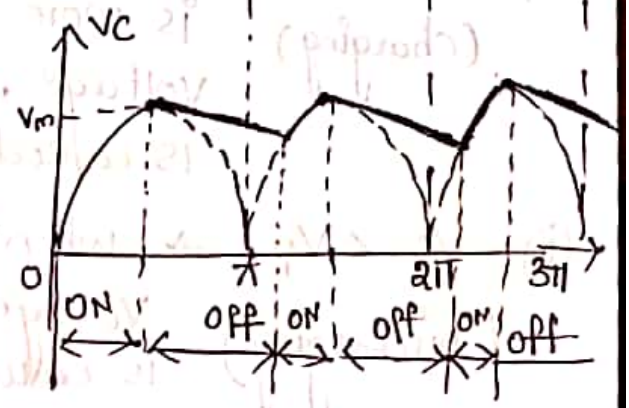


Fig: Filter circuits using full-wave rectifier
(a) Centre-tap transformer using filter-c
(b) Bridge rectifier using c-filter
and their Corresponding filter circuit waveform.

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Ripple factor :-

In Capacitor filter circuit, whatever the charge acquires by capacitor is equal to the charge of the capacitor has lost during the period of non-conducting.

i.e The charge aquires = $V_{rp-p} \times C$

The charge loss = $I_{dc} \times T_2$

$\therefore$ Acquired charge = charge lost

$$V_{rp-p} \times C = I_{dc} \times T_2$$

The value of capacitor is large and load resistance is also large. Then we have to assume that

T_2 = Half of the periodic time of waveform ($T_2 = \frac{T_1}{2}$)

$$T_2 = \frac{T_1}{2} = \frac{1}{2f}$$

Then the value of ripple voltage peak-to-peak is

$$V_{r,P-P} = \frac{I_{dc}}{2fc}$$

With the assumption made above, the ripple form will be triangular in nature and the value of R.M.S of the ripple is given by $V_{r,rms}$

$$V_{r,rms} = \frac{V_{r,P-P}}{2\sqrt{3}}$$

$$V_{r,rms} = \frac{I_{dc}}{2\sqrt{3} \times 2f_c} = \frac{I_{dc}}{4\sqrt{3} f_c} = \frac{V_{dc}}{4\sqrt{3} f_c R_L}$$

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for full-wave rectifier with filter :— $V_r = \frac{V_{dc}}{2fCR_L}$

$\therefore$ Ripple factor $\gamma = \frac{V_{r,rms}}{V_{dc}}$ $V_{r(rms)} = \frac{V_r}{2\sqrt{3}}$

$= \frac{V_{dc}}{V_{dc}\, 4\sqrt{3} fCR_L}$

The ripple may be decreased by increasing C or R_L (or) both with a resulting increase in dc o/p voltage.

if f = 50Hz, C = in μF, R_L = in Ω, $\gamma = \frac{2890}{CR_L}$ //.

for fullwave $\longrightarrow$ $\gamma = \frac{1}{4\sqrt{3} fCR_L}$ Where f_c = supply frequency (Hz)

R_L = load-resistance (Ω)

C = Capacitor (F). filter in F.

for Half-wave rectifier with filter :—

$V_r = \frac{V_{dc}}{fCR_L}$, $V_{r(rms)} = \frac{V_r}{2\sqrt{3}}$

Ripple factor = $\frac{V_{r(rms)}}{V_{dc}} = \frac{V_{r(rms)}}{2\sqrt{3} fCR_L \cdot V_{dc}} = \frac{1}{2\sqrt{3} fCR_L}$.

i.e $V_{r(rms)} = \frac{V_r}{2\sqrt{3}} = \frac{V_{dc}}{2\sqrt{3} fCR_L}$ $V_{r(rms)}$.

$\therefore \frac{V_{r(rms)}}{V_{dc}} = \frac{V_{dc}}{2\sqrt{3} \times fC \times R_L \times V_{dc}} = \frac{1}{2\sqrt{3} fCR_L}$.

$\gamma = \frac{1}{2\sqrt{3} fCR_L}$ $\longrightarrow$ for Half wave.

Where f = Supply frequency (Hz)

C = Capacitor filter in F

R_L = load resistance in Ω

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formulae :—

* DC output voltage $V_{DC} = V_m + I_{DC}\left[\frac{1}{4fC}\right]$ $\longrightarrow$ for full wave rectifier with C-filter.
* DC output voltage $V_{DC} = V_m - I_{DC}\left[\frac{1}{2fC}\right]$ $\longrightarrow$ for Half-wave with C-filter
* $V_{r(rms)}$ (rms voltage) = $\frac{I_{DC}}{4\sqrt{3} fC}$ volts. $\longrightarrow$ full wave filter
* $V_{r(rms)}$ (rms voltage) = $\frac{I_{DC}}{2\sqrt{3} fC}$ volts $\longrightarrow$ Half wave filter

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Advantages :- The advantages of C-filter are

1. Less number of components
2. Low ripple factor hence low ripple voltage
3. Suitable for high voltage at small load current

Disadvantages :- The Disadvantages of C-filter are

1. Ripple factor depends on load resistance
2. Not suitable for variable loads as ripple content increases as R_L decreases.
3. Regulation is poor.
4. Diodes are subjected to high surge currents hence must be selected accordingly.

Problems:

1). Calculate the value of Capacitance to use in Capacitor filter Connected to a full wave rectifier Operating at a standard aircraft power frequency of 400 Hz. If the ripple factor is 10% of a load of 500Ω

$$\Gamma = \frac{1}{4\sqrt{3} f C R_L}$$

$$\Gamma = 10\% = 10 \times \frac{1}{100} = 0.1$$

$$f = 400, \; R_L = 500\Omega$$

$$\Gamma = \frac{1}{4\sqrt{3} f C R_L} \Rightarrow C = \frac{1}{4\sqrt{3} f \Gamma R_L}$$

$$= \frac{1}{4\sqrt{3} \times 400 \times 0.1 \times 500}$$

$$= \frac{1}{1385600} = 7.21 \mu f.$$

$$\boxed{\Gamma = 7.21 \mu f}$$

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... - Idc = Vm - 0 = Vm

2. Calculate the value of Capacitance to use in a Capacitor filter connected to a full-wave rectifier operating at a standard aircraft power frequency of 400 Hz, if the ripple factor is 10% for a load of 500Ω.

&

2. A FWR voltage of 18V peak is applied across a 500μF filter Capacitor. Calculate the ripple and dc voltages if the load takes a current of 100 mA.

Given $V_m = 18V$

$C = 500\mu F$

$I_{dc} = 100\,mA$

$$V_{dc} = V_m - \frac{I_{dc}}{4fC} = 18 - \frac{100\times10^{-3}}{4\times50\times500\times10^{-6}} = 17V$$

$$V_{r,rms} = \frac{I_{dc}}{4\sqrt{3}fC} = \frac{100\times10^{-3}}{4\sqrt{3}\times50\times500\times10^{-6}} = 0.577\,V$$

$$\therefore \text{ripple factor } \gamma = \frac{V_{rms}}{V_{dc}} = \frac{0.577}{17}\times100 = 3.39\%$$

3. A Bridge rectifier with Capacitor filter is fed from 220V to 40V step down transformer. If average d.c current in load is 1A and Capacitor filter of 800μF. Calculate the load regulation and ripple factor. Assume power line frequency of 50Hz. Neglect diode forward resistance and d.c resistance of secondary of transformer?

$V_m(rms) = 40V \quad C = 800\mu F, \; f = 50Hz$

$I_{dc} = 1A$

$$\therefore V_m = \sqrt{2}\,V_{rms} = \sqrt{2}\times40 = 56.56\,V$$

$$V_{dc(FL)} = V_m - \frac{I_{dc}}{4fC} = 56.5685 - \frac{1}{4\times50\times800\times10^{-6}} = 50.31V$$

On no load $I_{dc} = 0$

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Hence $V_{dc(NL)} = V_m - \frac{I_{dc}}{4fC} = V_m - 0 = V_m = 56.56V$

$\therefore$ percentage of regulation $= \frac{V_{dc(NL)} - V_{dc(FL)}}{V_{dc(FL)}} \times 100$

$= \frac{56.56 - 50.3185}{50.3185} \times 100$

$= 12.42\%$

$R_L = \frac{V_{dc}}{I_{dc}} = \frac{50.31}{1} = 50.31\Omega$

$\gamma = \frac{1}{4\sqrt{3}fCR_L} = \frac{1}{4\sqrt{3} \times 50 \times 800 \times 10^{-6} \times 50.3185} = 0.0717$

i.e 7.17% of ripples present.

L - filter (Inductor filter) :-

In this type of filter an inductor (choke) is connected in series with the load. It is known that the inductor opposes change in the current. So the ripple which is change in the current is opposed by the inductor and it tries to smoothen the output.

The below circuit shows the inductor filter. when the output of the rectifier passes through an inductor, it blocks the ac component and allows only dc component to reach the load

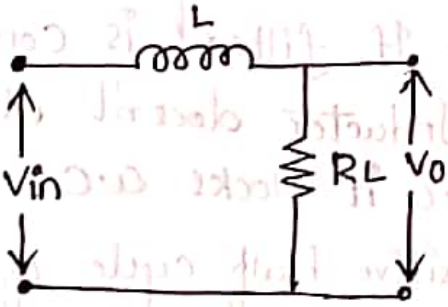

fig:- Inductor filter (or) choke filter

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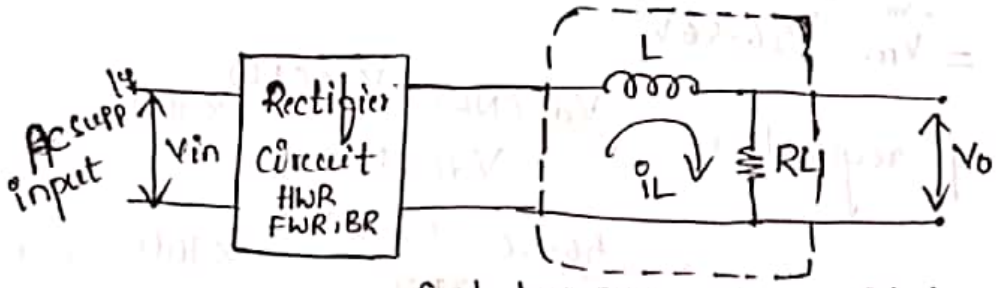

fig:- Inductor filter with Rectifier circuit.

The Rectified output is connected to the Inductor filter which is used to remove unwanted ripples in rectified output using Inductor. Inductor is used to blocks a.c (ripples) in the output of rectifier then pass remaining part of rectified o/p which is d.c content across load.

Inductor : It is used to allows d.c and blocks a.c

Let us Consider, Fullwave rectifier circuit with Inductor-filter.

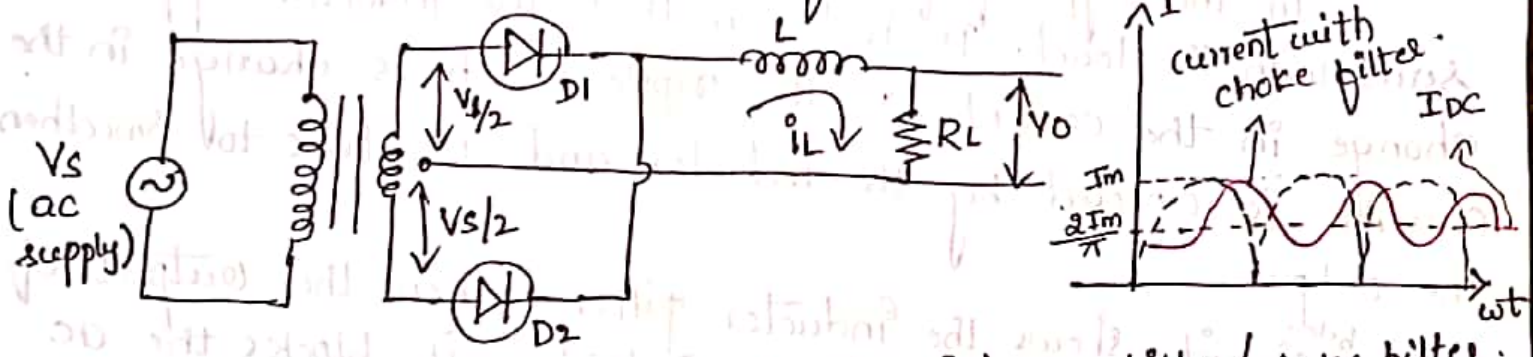

fig:- Full wave rectifier circuit with L-filter/choke filter.

The Output of full wave rectifier is Connected to the input of Inductor filter. If filter is connected what happening in the circuit is, the Inductor doesn't allow instantaneous Current, so it allows d.c it blocks a.c

Operation :— If the positive half cycle of the Secondary voltage of the transformer, the diode D_1 is forward biased. Hence the current flowing (flows) through D_1 and L, RL also.

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While in the negative half cycle, the diode D_1 is reverse biased, while Diode D_2 is forward biased. Hence the current flows through D_2, L and R_L. Hence we get the unidirectional current flowing through R_L. Due to inductor L, which opposes change in current, it tries to make the output smooth by opposing the ripple content in the output.

We know that,

The Fourier Series for the load current for full wave rectifier is

$$i_L = I_m \left[\frac{2}{\pi} - \frac{4}{3\pi} \cos 2\omega t - \frac{4}{15\pi} \cos 4\omega t \right]$$

Neglecting higher order harmonics we get,

$$i_L = I_m \left[\frac{2}{\pi} - \frac{4}{3\pi} \cos 2\omega t \right] \quad \left(\because \frac{4}{15\pi} \cos 4\omega t = 0 \right)$$

$$i_L = \frac{2I_m}{\pi} - \frac{4I_m}{3\pi} \cos 2\omega t \longrightarrow (1)$$

for full wave

$$I_{DC} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi \cdot R_L} \quad \left(\because I_m = \frac{V_m}{R_L} \right).$$

While the second harmonic Component represents a.c Component or ripple present and can be written as,

$$I_m = \frac{V_m}{Z} \text{ for a.c component}$$

$\tan\phi = \frac{2\omega L}{R_L}$ $\cos\phi = \frac{R}{Z}$

Where $Z = R_L + j2X_L = \sqrt{R_L^2 + 4\omega^2 L^2} \angle\phi$ (angle ϕ).

Where $\phi = \tan^{-1}\left(\frac{2\omega L}{R_L}\right)$ (X_L – inductive reactance – opposition that electronic components exhibit to the passage of AC

(Impedance (Z) – Resistance & Reactance Combined to form an impedance
– it is also used for opposition of flow of electric current
– which exhibits in AC circuit

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$$I_m = \frac{V_m}{\sqrt{R_L^2 + 4\omega^2 L^2}} \longrightarrow (2)$$

Hence, eq (1) can be modified as,

$$i_L = \frac{2V_m}{\pi R_L} - \frac{4V_m}{3\pi\sqrt{R_L^2 + 4\omega^2 L^2}} \cos(2\omega t - \phi) \longrightarrow (3)$$

The ripple present is the 2nd harmonic component having frequency '2ω'. Hence while calculations, the effective inductive reactance must be calculated at 2ω hence represented as $2X_L$ in the above equations of 'Z'

Ripple factor :—

Ripple factor is given by, (here using i_L - 2nd harmonic - maximum current is from (3) & $I_m = \frac{2V_m}{3\pi\sqrt{R_L^2 + 4\omega^2 L^2}}$ from (2))

$$\gamma = \frac{I_{r\,rms}}{I_{DC}} \qquad I_{r\,rms} = \frac{4V_m}{3\sqrt{2}\pi\sqrt{R_L^2 + 4\omega^2 L^2}}$$

Where $I_{r,rms} = \frac{I_m}{\sqrt{2}}$ of a.c component present in i_L

$$I_{DC} = \frac{2I_m}{\pi} = \frac{2V_m}{\pi \cdot R_L}$$

$$\therefore \text{Ripple factor} = \frac{\frac{4V_m}{3\sqrt{2}\pi\sqrt{R_L^2 + 4\omega^2 L^2}}}{\frac{2V_m}{\pi R_L}}$$

$$= \frac{\pi R_L}{2V_m} \times \frac{4V_m}{3\sqrt{2}\pi\sqrt{R_L^2 + 4\omega^2 L^2}}$$

$$= \frac{2R_L}{3\sqrt{2}\sqrt{R_L^2 + 4\omega^2 L^2}} = \frac{2}{3\sqrt{2}} \cdot \frac{R_L}{\sqrt{R_L^2\left(1 + \frac{4\omega^2 L^2}{R_L^2}\right)}}$$

$$= \frac{2}{3\sqrt{2}} \cdot \frac{R_L}{R_L\sqrt{1 + \frac{4\omega^2 L^2}{R_L^2}}}$$

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$$\therefore \text{Ripple factor} = \frac{2}{3\sqrt{2}} \cdot \frac{1}{\left(\sqrt{\frac{4\omega^2 L^2}{R_L^2} + 1}\right)}$$

Initially on on load condition $R_L \longrightarrow \infty$

hence, $\frac{4\omega^2 L^2}{R_L^2} \longrightarrow 0$.

$$\therefore \text{Ripple factor} = \frac{2}{3\sqrt{2}} = 0.472$$

This is very close to normal full wave rectifier without filtering.

But as load increases R_L decreases

hence $\frac{4\omega^2 L^2}{R_L^2} >> 1$ so neglecting 1 we get

$$\text{ripple factor} = \frac{2}{3\sqrt{2}} \cdot \frac{1}{\sqrt{\frac{4\omega^2 L^2}{R_L^2}}} = \frac{2}{3\sqrt{2}} \cdot \frac{1}{2\omega L} \times R_L$$

$$\Gamma = \frac{R_L}{3\sqrt{2} \cdot \omega L} //$$

So load changes, ripple changes which is inversely proportional to the value of the inductor.

Note :— Smaller the value of R_L, smaller the ripple hence the filter is suitable for low load resistances i.e for high load current applications. But as choke/inductor filters are not used now a days as inductors are bulky, costlier and more power consuming.

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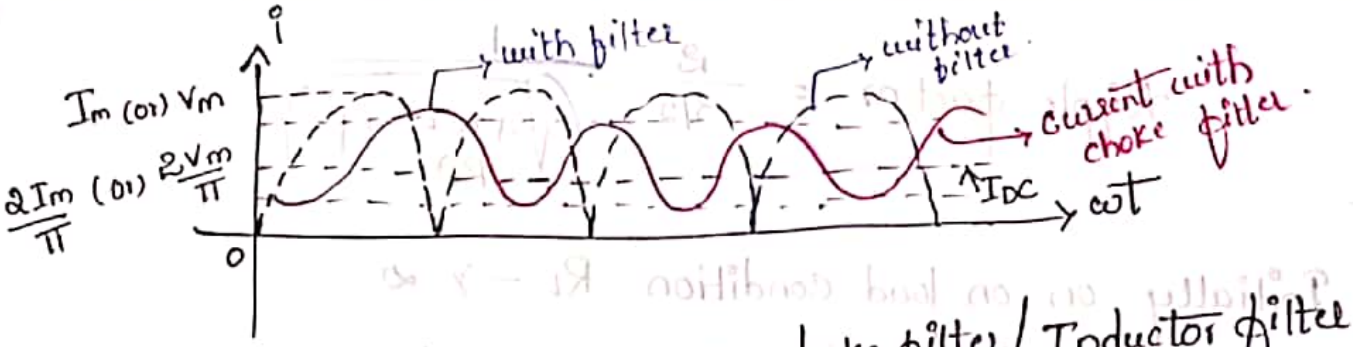
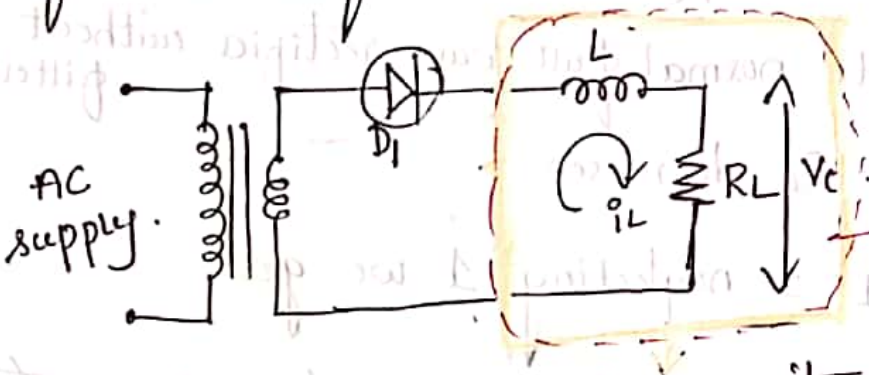


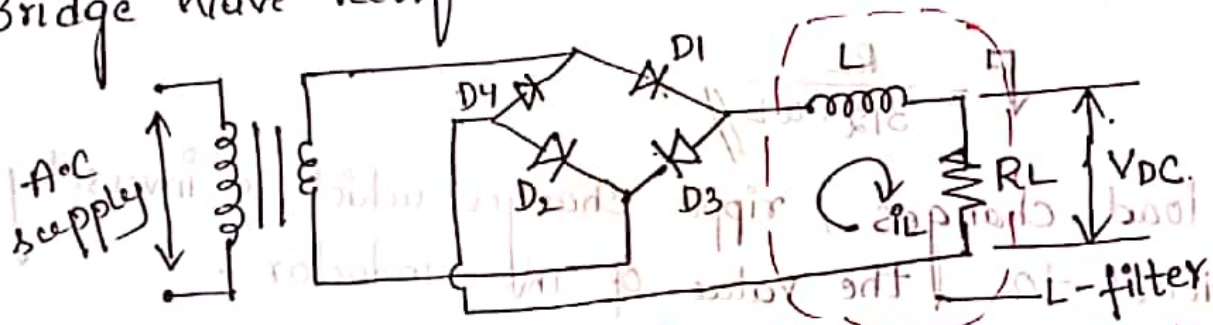
fig: Current waveform of choke filter / Inductor filter.

Half-wave rectifier circuit with Inductor filter :—



Inductor filter circuit

Bridge Wave rectifier Circuit with Inductor filter :—



Problem :— Calculate Value of inductance to use in the inductor filter connected to a full wave rectifier operating at 60Hz to provide a dc output with 4% ripple for a 100Ω load?

We know that (γ) ripple factor for Inductor-filter $= \frac{R_L}{3\sqrt{2}\omega L}$ → (1).

ripple content is 4% i.e $\frac{4}{100} = 0.04$; $R_L = 100\Omega$, $\omega = 2\pi f$, $f = 60Hz$, $L = ?$

$\therefore \gamma = \frac{R_L}{3\sqrt{2}\omega L}$ (from (1))

$0.04 = \frac{100}{3\sqrt{2} \times 2\pi \times 60 \times L} \Rightarrow L = \frac{0.0625}{0.04} = 1.5625$ H //

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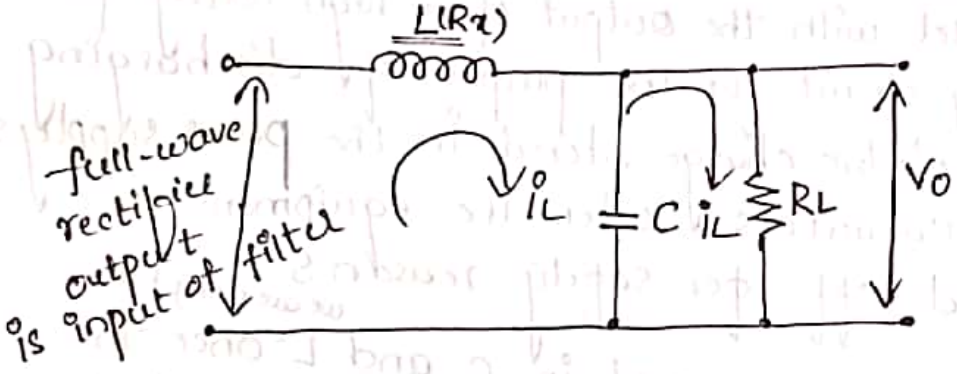
L- Section or LC filter :—

This is also called "choke input filter" as the first Element looking from the rectifier side is an "Inductance" (L). The d.c winding resistance of the choke is R_x. The circuit is also called "L-type filter" or LC filter. The circuit is shown in below



The basic requirement of this filter circuit is that the current through the choke (inductor) must be continuous and not interrupted. In LC filter, the inductor is connected series to load resistor and capacitor is parallely connected to the load resistor R_L.

* An Interrupted current through the choke may develop a large back e.m.f which may be in Excess of PIV rating of the diodes and/or maximum voltage rating of the Capacitor C. Thus this back e.m.f is harmful to the diodes and Capacitor. To eliminate the back e.m.f developed across the choke, the current through it must be maintained Continuous.

This is assured by connecting a bleeder resistance, R_B across the output terminals.

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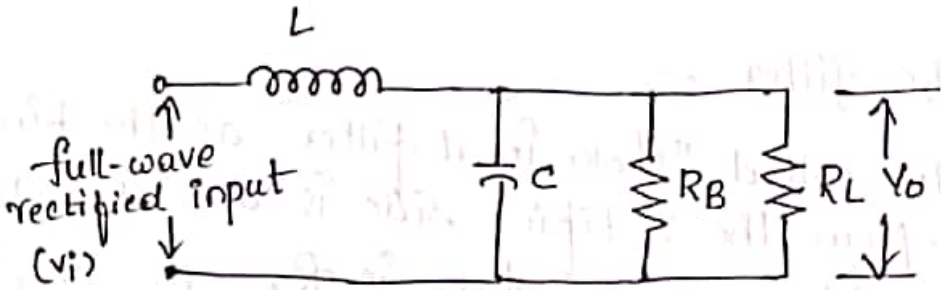


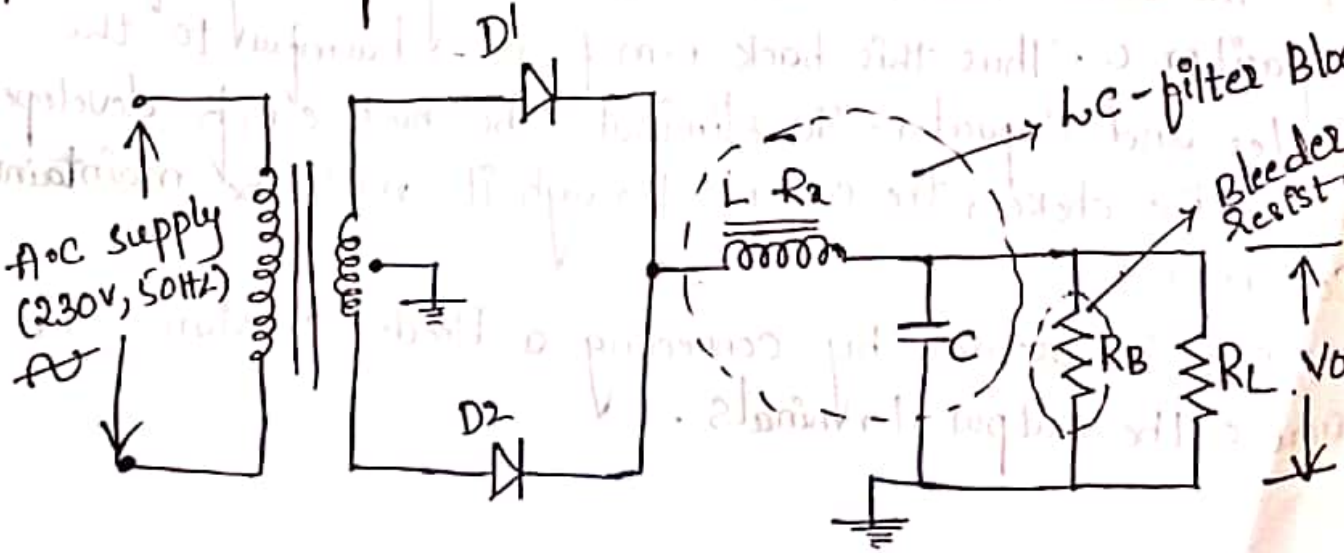
fig: Bleeder resistor connected as the LC filter output.

Bleeder resistor (RB): Bleeder resistor is a resistor connected in parallel with the output of a high voltage power supply circuit for the purpose of discharging the electric charge stored in the power supply's filter capacitors when the equipment is turned off, for safety reasons we are using RB

* To discharge the energy present in C and L* once the circuit is turned off. It prevents a electrical shock
* In case Bleeder resistor is not provided then L and C would be charged and upon contact would discharge through your body.

Hence, providing a resistor (Bleeder) causes the charged Energy to decay when circuit is turned off.

Full-Wave rectifier circuit with LC filter :-



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During positive half cycle of applied sine wave, the diode D_1 conducts (replaced by short circuit) the current flows through the diode, this current having undesirable components these can be applied input of LC filter. Here L (inductor) is connected in series with load resistance, it allows d.c and rejects a.c, the rejected a.c components are shunted to ground and allows d.c passes through R_L, the d.c voltage across load resistance obtained. The capacitor is connected parallel to load resistance R_L it allows a.c which is shunted to ground rejects d.c. The rejected d.c passes through circuit and taken the d.c voltage across the load resistance R_L. The same process will be done during negative half cycles which is reverse.

Ripple factor :—

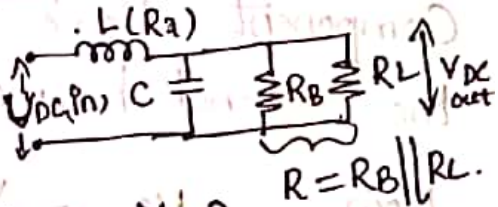
filter elements L and C are having reasonably large values

The Reactance X_L of the inductance L at 2w

i.e $X_L = 2\omega L$

The Reactance X_C of the Capacitance C at 2w as

i.e $X_C = \frac{1}{2\omega C}$



$\therefore \quad X_L >> X_C$ (X_L much larger than X_C).

Let R be the equivalent resistance of Bleeder resistance R_B and the load resistance R_L connected in parallel

Then, $$R = R_B \| R_L = \frac{R_B \cdot R_L}{R_B + R_L}$$

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Using Fourier Series,

The input voltage V_{in} can be written as

$$V_{in} = V_{sm}\left[\frac{2}{\pi} - \frac{4}{3\pi}\cos 2\omega t - \frac{4}{15\pi}\cos 4\omega t \cdots\right]$$

where V_{sm} = Maximum Value of half secondary voltage of the transformer.

The 1st term in $V_{in} \rightarrow \frac{2}{\pi} V_{sm}$ indicates d.c output voltage of the rectifier, remaining terms "ripple".

The amplitude of the lowest ripple Component, is Second harmonic Component of the frequency is, $\frac{4}{3\pi}$

amplitude of the fourth harmonic component is, $\frac{4}{15\pi}$

i.e amplitude of 4th Harmonic = $\frac{1}{5^{th}}$ (or) 20% of amplitude of second harmonic component.

The remaining higher Components will have still less amplitudes Compared to amplitude of Second harmonic Component. Hence all harmonics are neglected, except the second harmonic.

Now $V_{in} = V_{sm}\left[\frac{2}{\pi} - \frac{4}{3\pi}\cos 2\omega t\right]$

$V_{im} = \frac{2V_m}{2}$

$V_{2sm} = \frac{4V_m}{3\pi}$

DC current = $I_{DC} = \frac{\frac{2}{\pi} V_{sm}}{\pi(R_x + R)}$ $\left(R = R_B \| R_L\right)$

V_{DC} (DC voltage across load) = $V_{DC} = I_{DC} \cdot R$

$= \frac{2}{\pi}\frac{V_{sm}}{R_x + R} \times R$

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$$V_{DC} = \frac{2}{\pi}\frac{V_{sm}\cdot R}{R\left(1+\frac{R_2}{R}\right)} = \frac{2}{\pi}\frac{V_{sm}}{1+\frac{R_2}{R}}$$

$$V_{DC} = \frac{2}{\pi}\frac{V_{sm}}{1+\frac{R_2}{R}\to 0} \quad R_2 << R \text{ neglect it.}$$

$$V_{DC(cot)} = \frac{2V_{sm}}{\pi} \simeq V_{DC(in)}$$

∴ Thus the choke input filter circuit gives approximately constant d.c voltage across the load

⇒ The impedance Z_2 of filter circuit for 2nd harmonic component at 2ω will be

$$Z_2 = (R_2) + j(2\omega L) + \left[\frac{1}{j2\omega C} \| R\right]$$

$\frac{1}{2\omega C} << R$, $2\omega L >> R_2$

then $Z_2 = R_2 \to 0 + j2\omega L + \left(\frac{1}{j2\omega C} \| R\right) \to 0$

$$Z_2 = j2\omega L \qquad |Z_2| = \sqrt{(2\omega L)^2}$$

Hence $|Z_2| = (2\omega L) = 2\omega L$

2nd Harmonic Component of the current in the filter circuit

$I_{2m} = \frac{V_{2m}}{Z_2}$ $\quad V_{2m} = \frac{4}{3\pi} V_{sm}$

$$I_{2m} = \frac{\frac{4}{3\pi} V_{sm}}{Z_2} = \frac{\frac{4}{3\pi} V_{sm}}{2\omega L}$$

2nd Harmonic voltage across the load is

$$V_{2m} = I_{2m} \times \left(\frac{1}{2\omega C} \| R\right) \qquad \frac{1}{2\omega C} << R.$$

$$= I_{2m} \times \frac{1}{2\omega C}$$

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$$V_{2m} = I_{2m} \times \frac{1}{2\omega C}$$

$$= \frac{\frac{4}{3\pi} V_{sm}}{2\omega L} \times \frac{1}{2\omega C}$$

$$= \frac{4}{3\pi} \frac{V_{sm}}{4\omega^2 LC}$$

$$V_{2m} = \frac{V_{sm}}{3\pi\omega^2 LC}$$

$$\therefore V_{2(rms)} = \frac{V_{2m}}{\sqrt{2}} = \frac{V_{sm}}{3\sqrt{2}\pi\omega^2 LC}$$

Hence Ripple factor is given by

$$\text{Ripple factor} = \frac{V_{2rms}}{V_{DC}}$$

$$= \frac{\frac{V_{sm}}{3\sqrt{2}\pi\omega^2 LC}}{\frac{2}{\pi}\frac{V_{sm}}{1+\frac{R_2}{R}}} = \frac{V_{sm}}{3\sqrt{2}\pi\omega^2 LC} \times \frac{\pi\left(1+\frac{R_2}{R}\right)}{2V_{sm}}$$

$$= \frac{1}{6\sqrt{2}\omega^2 LC}$$

$$= \frac{1}{6\sqrt{2}\omega^2 LC} \times \left(1+\frac{R_2}{R}\right)$$

$$\left(\text{J}^{\text{H}} = \frac{1}{6\sqrt{2}\omega^2 LC}\right) \quad (R_2/R << 1)$$

neglect $\frac{R_2}{R}$.

Hence, the ripple factor for choke-input filter does not depends upon the load resistance unlike the Capacitor input filter.

This filter circuit is having better load regulation Compared to that of Capacitor input filter in which case the d.c voltage depends upon the D.C load Current.

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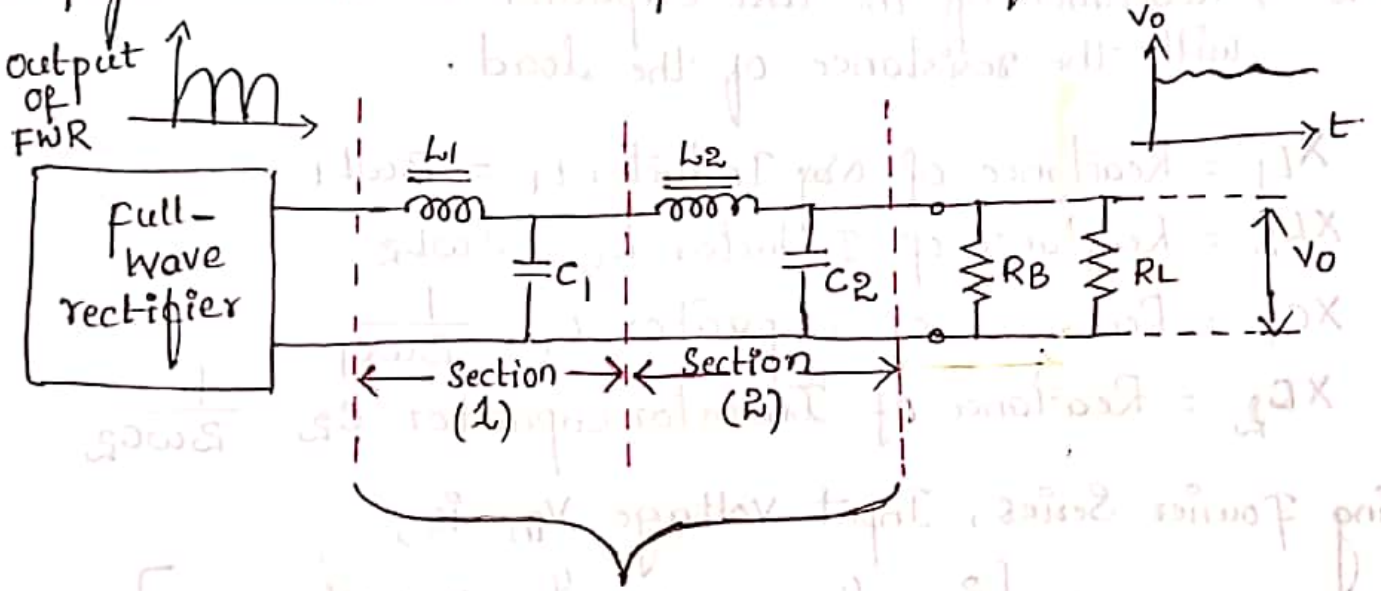
Multiple L- Section filter :-

The Number of L-section i.e LC circuits can be Connected One after another to obtain multiple L-section filter. It gives Excellent filtering and Smooth d.c output voltage.

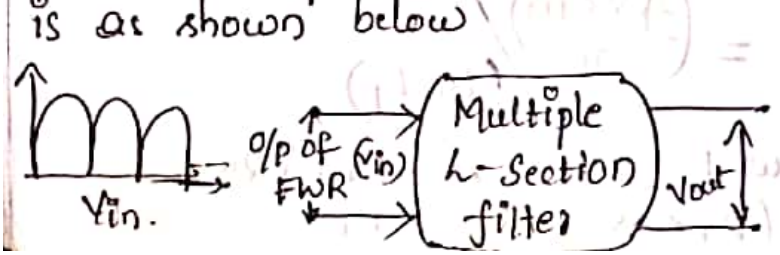
The figure below shows multiple L-section filter

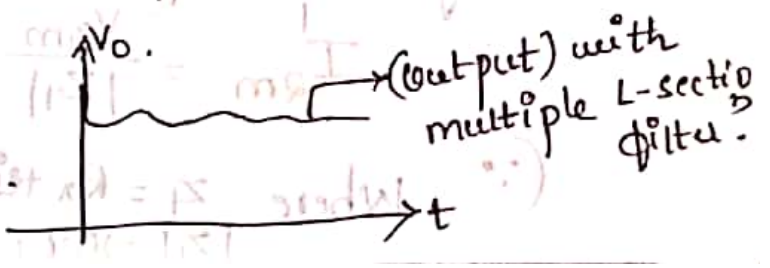


Multiple L- Sections

Fig:- Multiple L-section filter

The above figure shows the multiple L-section filter. In this multiple number of LC-filters are interlinked by wires. Here two LC filters are connected at the output of full wave rectifier. By connecting more number of filters the output of rectifier is filtered Efficiently and gives the Smooth D.C output voltage, as shown in above figure. at the output of LC filter. The output wave form of filter is as shown below





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Ripple factor :-

The following assumptions are made in the analysis of multiple L-section (LC) filter.

*1 → Reactances of all the inductors are much greater than the reactances of the capacitors

*2 → Reactance of the last capacitor is small compared with the resistance of the load.

X_{L_1} = Reactance of Inductor $L_1 = 2\omega L_1$

X_{L_2} = Reactance of Inductor $L_2 = 2\omega L_2$

X_{C_1} = Reactance of Capacitor $C_1 = \frac{1}{2\omega C_1}$

X_{C_2} = Reactance of ~~Inductor~~ Capacitor $C_2 = \frac{1}{2\omega C_2}$

Using Fourier Series, Input voltage V_{in} is,

$$V_{in} = V_{sm}\left[\frac{2}{\pi} - \frac{4}{3\pi}\cos 2\omega t - \frac{4}{15\pi}\cos 4\omega t ----\right]$$

$$V_{in} = \frac{2V_{sm}}{\pi} - \frac{4V_{sm}}{3\pi}\cos 2\omega t \quad \left[\begin{matrix}\text{neglecting Higher} \\ \text{order harmonics}\end{matrix}\right].$$

1st terms indicates d.c output voltage → $\frac{2V_{sm}}{\pi}$

2nd term (i.e 2nd Harmonic) indicates for a.c Component

↳ $\frac{4V_{sm}}{3\pi}\cos 2\omega t$, Where $\frac{4V_{sm}}{3\pi} = V_m = V_{2m}$ = Second harmonic maximum value.

∴ The second harmonic current component flowing through the capacitor C_1 is

$$I'_{2m} = \frac{V_{2m}}{|Z_1|} = \left(\frac{4V_{sm}}{3\pi}\right) \Big/ (2\omega L_1)$$

(∵ Where $Z_1 = R_2 + j2\omega L_1 = R_2 + j2X_L = R_2 + j2\omega L$

$|Z_1| = 2\omega L_1$ ($R_2 << X_L$ – neglect R_2))

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R.m.s value of current

$$I'_{2(rms)} = \frac{I'_{2m}}{\sqrt{2}} = \frac{4}{3\pi} \times \frac{1}{\sqrt{2}} \times \frac{V_{sm}}{\omega L_1}$$

$$I'_{2(rms)} = \frac{4}{3\pi} \times \frac{1}{\sqrt{2}} \times \frac{V_{sm}}{X_{L1}}$$

$$I'_{2(rms)} = \frac{4^2}{3\pi} \times \frac{1}{\sqrt{2}} \times \frac{\pi \cdot V_{DC}}{2 X_{L1}} \quad \left(V_{DC} = \frac{2V_m}{\pi} = \frac{2V_{sm}}{\pi} \right)$$

$$\therefore V_{sm} = \frac{\pi \cdot V_{DC}}{2}$$

$$= \frac{2\pi V_{DC}}{3\pi\sqrt{2} X_{L1}}$$

$$= \frac{\sqrt{2} \times \sqrt{2}\,\pi V_{DC}}{3\pi\sqrt{2} X_{L1}}$$

$$\boxed{I'_{2(rms)} = \frac{\sqrt{2}}{3} \frac{V_{DC}}{X_{L1}}} \longrightarrow (1)$$

Where $I'_{2(rms)}$ = first section of LC filter – rms current

case 2:- If for Second section of LC filter having rms current is just $I_{2(rms)}$ not $I'_{2(rms)}$.

$\therefore I_{2(rms)}$ = Second section LC filter – rms current.

In this case neglecting reactance of the last capacitor (C_2) Consider C_1 only then

$$I_{2(rms)} = \frac{\text{Voltage across } C_1}{X_{L2}}$$

$$= \frac{(I'_{2(rms)}) X_{C1}}{X_{L2}}$$

$$\boxed{I_{2(rms)} = \frac{\frac{\sqrt{2}}{3} \frac{V_{DC}}{X_{L1}} * (X_{C1})}{X_{L2}}} \longrightarrow (2)$$

Here Where * → indicates multiplication

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Case (3)

Ripple voltage across the load is the voltage across Capacitor C_2,

$$V_r(r.m.s) = I_2(r.m.s) * [X_{C2})$$

$$= \frac{I_2'(rms)\, X_{C1}}{X_{L2}} * X_{C2}$$

$$= \frac{\sqrt{2}}{3} * \frac{V_{DC}\, X_{C1}}{X_{L2}} * \frac{X_{C2}}{X_{L1}}$$

$$V_{r(rms)} = \frac{\sqrt{2}}{3} * \frac{V_{DC}\, X_{C1} X_{C2}}{X_{L1} X_{L2}} \longrightarrow (3)$$

$\therefore$ Ripple factor $\gamma = \frac{V_r(r.m.s)}{V_{DC}}$

Substitute (3) in γ then we get

$$\gamma = \left(\frac{\sqrt{2}}{3} \frac{V_{DC}\, X_{C1} X_{C2}}{X_{L1} X_{L2}}\right) \Big/ (V_{DC})$$

$$\gamma = \frac{\sqrt{2}}{3} \frac{X_{C1}}{X_{L1}} \frac{X_{C2}}{X_{L2}} \longrightarrow (4)$$

where X_{C1} – Reactance of C_1 capacitor $= \frac{1}{2\omega C_1}$

X_{C2} – Reactance of C_2 capacitor $= \frac{1}{2\omega C_2}$

X_{L1} – Reactance of L_1 inductor $= 2\omega L_1$

X_{L2} – Reactance of L_2 inductor $= 2\omega L_2$

then Sub $X_{C1}, X_{C2}, X_{L1}, X_{L2}$ in (4) we get

$$\gamma = \frac{\sqrt{2}}{3} \cdot \frac{1/2\omega C_1}{2\omega L_1} \times \frac{1/2\omega C_2}{2\omega L_2} = \frac{\sqrt{2}}{3} \cdot \frac{1}{2\omega C_1} \times \frac{1}{2\omega L_1} \times \frac{1}{2\omega C_2} \times \frac{1}{2\omega L_2}$$

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$$\Gamma = \frac{\sqrt{2}}{3}\,\frac{1}{16\omega^4 L_1 L_2 C_1 C_2}$$

for multiple π-section filter having n similar sections with $L_1 = L_2 = \ldots L_n$ and $C_1 = C_2 = \ldots C_n$ then the Ripple factor is given by

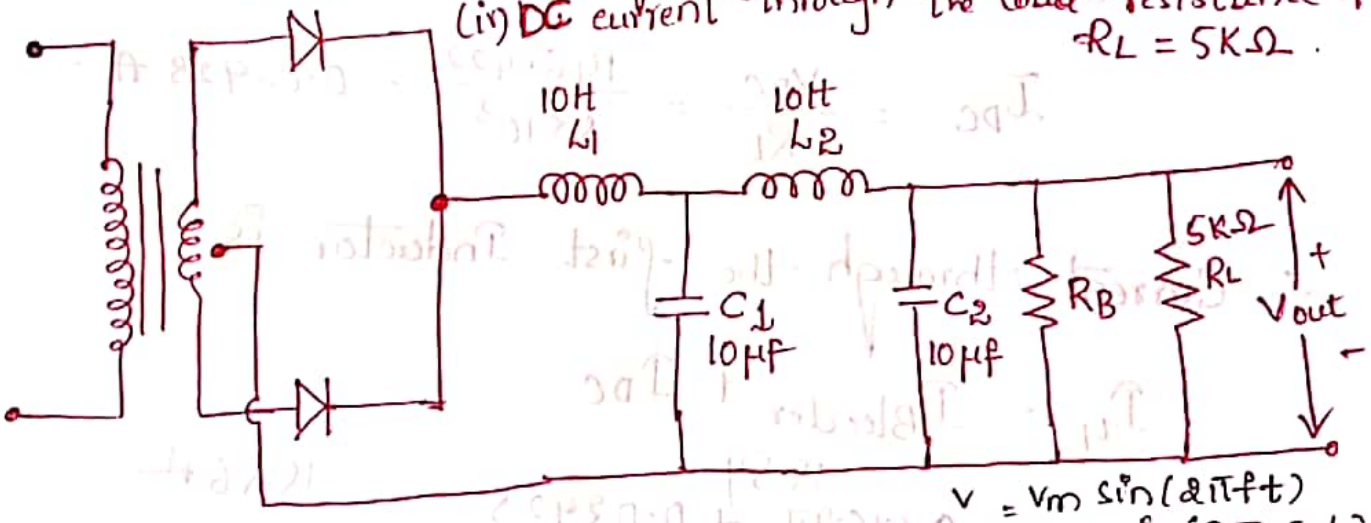
$$\sqrt{\Gamma} = \frac{\sqrt{2}}{3}\,\frac{1}{(4\omega^2 LC)^n}$$

* The value of critical inductance is $L_{critical} = \frac{R_L}{3\omega}$
* The value of Bleeder resistance is $R_B \leq 3\omega L$

Problems :—

1. For a rectifier circuit shown below, the voltage $v = 230\sin$ $V = 230\sin(2\pi \times 50t)$ V.

Calculate : (i) Ripple factor
(ii) Suitable Bleeder resistance
(iii) Current through the first inductor with R_B in the circuit.
(iv) DC current through the load resistance if $R_L = 5K\Omega$.



$v = V_m \sin(2\pi f t)$
$V = 230\sin(2\pi \times 50t)$

Sol: Given that $L_1 = L_2 = 10H$, $f = 50Hz$
$C_1 = C_2 = 10\,\mu f$, $R_L = 5K\Omega$, $V_m = 230V$.

(i) Ripple factor

for two section LC filter, $n = 2$ hence

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$$\Gamma \text{ (or) } Y = \frac{\sqrt{2}}{3} \times \frac{1}{(4\omega^2 LC)^2}$$

$$= \frac{\sqrt{2}}{3} \times \frac{1}{(4 \times (2\pi \times 50)^2 \times 10 \times 10 \times 10^{-6})^2}$$

$$\boxed{Y = 3.0246 \times 10^{-4}}$$

(ii) $R_B \leq 3\omega L \leq 3 \times 2\pi \times 50 \times 10 \leq 9.42\ K\Omega$

$\therefore \boxed{R_B = 9\Omega} \approx 9.4\Omega$

(iii)(iv) $V_{DC} = \frac{2V_m}{\pi}$

$V_m = 230\ V$

$\therefore V_{DC} = \frac{2 \times 230}{\pi} = 146.422V \Rightarrow \boxed{V_{DC} = 146.422\ V}$

(iii) (iv) At with Bleeder resistor, the current through the first inductor is

$I_{Bleeder} = \frac{V_{DC}}{R_B} = \frac{146.422}{9.4 \times 10^3} = 0.016A$ ~~15.54~~

$I_{DC} = \frac{V_{DC}}{R_L} = \frac{146.422}{5 \times 10^3} = 0.02928\ A$

$\therefore$ Current through the first Inductor is

$I_L = I_{Bleeder} + I_{DC}$

$= 0.01627 + 0.02928 = 15.56\ A$

$I_L = 0.04555\ A$ (or) $45\ mA$

$\boxed{I_L = 0.045\ A}$ //.

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CLC filter (or) π - filter :—

* This is a Capacitor input filter followed by a L-Section.
* The Ripple Rejection Capability of π filter is very good.
* The CLC filter circuit is as shown below :

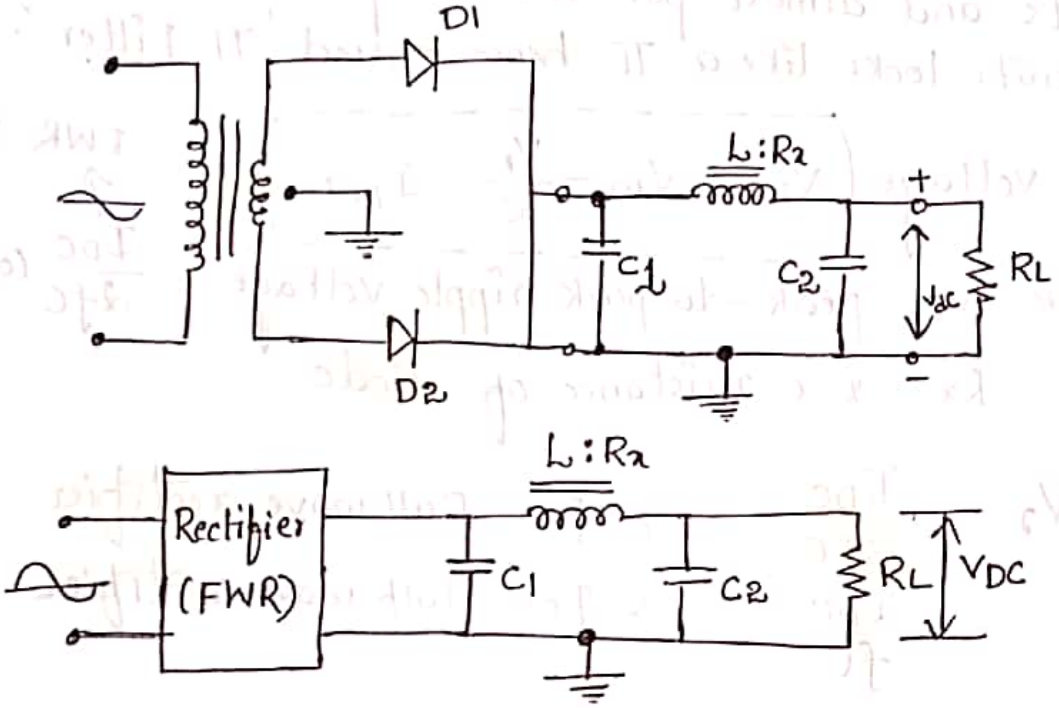

Fig : π Type filter

It Consists of an Inductance L with a d.c winding resistance as R_2 and two Capacitors C_1 and C_2. The filter circuit is fed from full wave rectifier. Two Capacitors are selected equal. This Circuit is basically a Capacitor input filter since the first element looking from the rectifier side is a "Capacitor".

Operation :—

The Rectifier Output is given to the Capacitor C_1. This Capacitor offers very low reactance to the a.c Component but blocks d.c Component. Hence Capacitor C_1 bypasses most of the a.c Component.

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The d·c Component then reaches to the choke L. The choke L offers very high reactance to a·c Component and low reactance to d·c Component. so it blocks a·c Component and does not allow it to reach to load while it allows d·c Component to pass through it. The Capacitor C_2 now allows to pass remaining a·c components and almost pure d·c Component reaches to the load. The circuits looks like a π hence called "π filter".

The output voltage $\left(V_{DC} = V_m - \frac{V_r}{2} - I_{DC}R_s\right)$ FWR ↑ HWR ↓

where V_r = peak-to peak ripple voltage $= \frac{I_{DC}}{2fC}$ (or) $\frac{I_{DC}}{fC}$

R_s = D·C resistance of diode

$\therefore$ $V_r = \frac{I_{DC}}{2fC}$ ⟶ for full wave rectifier

$= \frac{I_{DC}}{fC}$ ⟶ for Half wave rectifier

Ripple factor :—

With a full wave rectifier, the peak to peak value of the ripple voltage at the output of Capacitor input filter C_1 is given by,

Now $V_{r(p-p)} = \frac{I_{DC}}{2fC_1}$ (for full wave).

$V_{r(p-p)} = \frac{I_{DC}}{2 \times \frac{\omega}{2\pi} \times C_1}$ $\left(\because \omega = 2\pi f,\ f = \frac{\omega}{2\pi}\right)$

$$\left(V_{r(p-p)} = \frac{\pi I_{DC}}{\omega C_1}\right) \longrightarrow (1)$$

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The r.m.s value of the second harmonic ripple voltage is given by,

$$V_{r(ac)(r.m.s)} = \frac{V_{r(P-P)}}{\pi.\sqrt{2}} \longrightarrow (2)$$

Sub (1) in (2)

$$V_{r(r.m.s)} = \frac{\pi I_{DC}}{\omega C_1 (\pi\sqrt{2})} = \frac{I_{DC}}{\sqrt{2} \times \omega C_1}$$

$$= \frac{2 I_{DC}}{2\sqrt{2} \times \omega C_1}$$

$$= \frac{\sqrt{2}\sqrt{2} I_{DC}}{\sqrt{2} * 2\omega C_1} \quad \left(\frac{1}{2\omega C_1} = X_{C_1}\right)$$

$$= \sqrt{2} I_{DC} \cdot X_{C_1}$$

$$\therefore V_{r(rms)} = \sqrt{2} I_{DC} \cdot X_{C_1} \longrightarrow (3)$$

This is the ripple voltage at the input of LC_2 filter following the Capacitor C_1.

Using voltage division rule.

here ($*$ = Multiplier)

$$V'_{r(r.m.s)} = \frac{V_{r(r.m.s)} * X_{C_2}}{X_L - X_{C_2}}$$

$$V'_{r(r.m.s)} = \frac{V_{r(r.m.s)} X_{C_2}}{\left[\frac{X_L}{X_{C_2}} - 1\right] X_{C_2}} = \frac{V_{r(rms)}}{\left(\frac{X_L}{X_{C_2}} - 1\right)} \longrightarrow (4)$$

Note :- The Reactances must be Calculated at Second harmonic frequency 2ω

Now, $$\frac{X_L}{X_{C_2}} = \frac{2\omega L}{\left(\frac{1}{2\omega C_2}\right)} = 4\omega^2 LC_2$$

$4\omega^2 LC_2 >> 1$ hence 1 can be neglected

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$$V_r'(r\cdot m\cdot s) = \frac{V_r(r\cdot m\cdot s)}{4\omega^2 L C_2} = \frac{1}{(2\omega C_2)(2\omega L)} \cdot V_r(r\cdot ms)$$

$$V_r'(rms) = \frac{X_{C2}}{X_L} V_r(rms) \quad \left(\because X_{C2} = \frac{1}{2\omega C_2},\ X_L = 2\omega L\right)$$

$$\therefore V_r'(r\cdot m\cdot s) = \frac{X_{C2}}{X_L} V_r(rms) \longrightarrow (5)$$

Using equation (3) in (5)

$$V_r'(r\cdot m\cdot s) = \frac{X_{C2}}{X_L} * \sqrt{2}\, I_{DC} X_{C1}$$

Where $I_{DC} = \frac{V_{DC}}{R_L}$

$$V_r'(rms) = \frac{X_{C2}}{X_L} X_{C1} * \frac{V_{DC}}{R_L} * \sqrt{2}$$

$$V_r'(rms) = \sqrt{2}\, \frac{X_{C2}}{X_L} \cdot \frac{X_{C1}}{R_L} \cdot V_{DC} \longrightarrow (6)$$

$\therefore$ Ripple factor $= \dfrac{V_r'(rms)}{V_{dc}} \longrightarrow (7)$

Sub (6) in (7) we get

$$= \left(\sqrt{2} \cdot \frac{X_{C2}}{X_L} \cdot \frac{X_{C1}}{R_L} \cdot V_{dc}\right) / V_{dc}$$

$$\boxed{\gamma = \sqrt{2} \cdot \frac{X_{C2}}{X_L} \cdot \frac{X_{C1}}{R_L}}$$

We know $X_{C1} = \frac{1}{2\omega C_1}$ $\quad X_{L1} = 2\omega L_1$

$X_{C2} = \frac{1}{2\omega C_2}$ $\quad X_{L2} = 2\omega L_2$.

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Substitute $X_{C_1}, X_{C_2}, X_{L_1}, X_{C_2}$ in ripple factor

$$\text{Ripple factor } (\gamma) = \frac{\sqrt{2}\left(\frac{1}{2\omega C_1}\right)\left(\frac{1}{2\omega C_2}\right)}{(2\omega L) R_1}$$

$$\boxed{\gamma = \frac{\sqrt{2}}{8\omega^3 L C_1 C_2 R_L}}$$

* Since this π filter employs three filtering elements, the ripple is reduced to the great extent.

Eg:- If C_1, C_2 are expressed in microfarads and frequency f is assumed to be 50 Hz then we get

$$\gamma = \frac{\sqrt{2}}{8(2\pi \times f)^3 \times (C_1 \times 10^{-6})(C_2 \times 10^{-6} \times L \times R_L)}$$

$$= \frac{\sqrt{2}}{8(2\pi \times 50)^3 \times (C_1 \times 10^{-6} \times C_2 \times 10^{-6} \times L \times R_L)}$$

$$\boxed{\gamma = \frac{5700}{L C_1 C_2 R_L}}$$

this is formula for ripple factor when C_1, C_2 are in μf (microfarads), L in henries (H) and R_L in ohms.

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Multiple π Section filter :—

To obtain almost pure d.c to the load, more π sections may be used one after another. Such a filter using more than one π sections is called "Multiple π-section filter". The figure below shows multiple π-section filter.

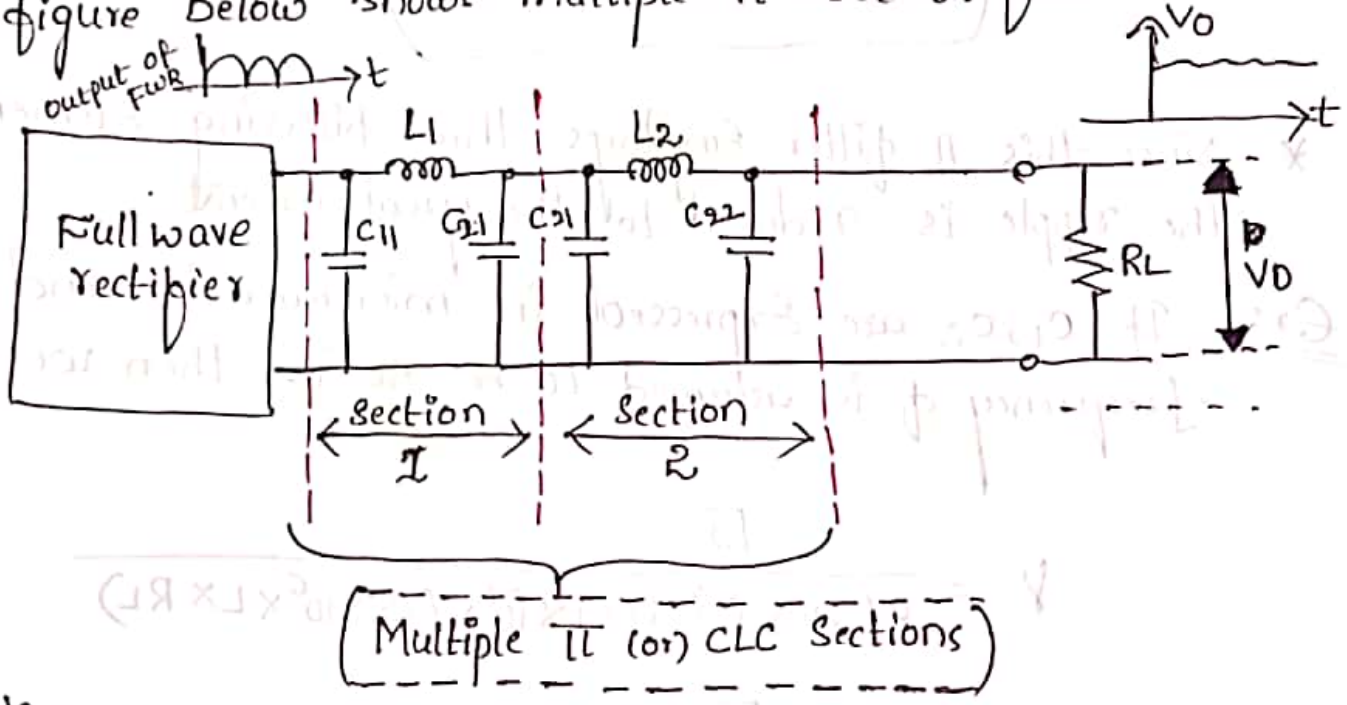

fig :- Multiple π-section filter.

The Ripple factor for multiple π section filter is given by

$$\gamma = \sqrt{2}\,\frac{X_{C11}}{R_L}\cdot\frac{X_{C21}}{X_{L1}}\cdot\frac{X_{C22}}{X_{L2}}\cdots\cdots$$

This expression can be extended to include n-number of such π-sections.

Where X_{C11} = Reactance of capacitor C_{11}

X_{C12} = Reactance of capacitor C_{12}

X_{C22} = Reactance of capacitor C_{22}

X_{C21} = Reactance of capacitor C_{21}

X_{L1} & X_{L2} – Reactance of inductor L_1 & L_2, R_L = load resistor.

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Advantages of π filter :—

The various advantages of π filter are,

1. For a same total value of L and C, the ripple factor of π filter is much smaller than multiple LC section filter.
2. Higher D.C output voltage at high load currents can be achieved.
3. The output is very much smoother.

Disadvantages :—

1. Voltage regulation is poor. Eventhough we are using CLC some small fluctuations are present at output waveform.
2. Higher values of PIV rating for the diode.

Problems :—

1. Calculate the ripple factor for a π-type filter, employing 10 H choke and two equal capacitors 16 μf each and fed from a full-wave rectifier and 50 Hz mains. The load resistance is 4 KΩ

Given values are : $C_1 = C_2 = 16\mu F$, $L = 10H$, $R_L = 4K\Omega = 4000\Omega$

$f = 50$ Hz

Ripple factor $$\gamma = \frac{\sqrt{2}}{8\omega^3 L C_1 C_2 R_L} = \frac{\sqrt{2}}{8(2\pi f)^3 L C_1 C_2 R_L}$$

$$= \frac{\sqrt{2}}{8(2\pi\times 50)^3 \times 16\times 10^{-6}\times 16\times 10^{-6}\times 10\times 4000} = 5.56\times 10^{-4}$$

Thus ripple is 0.055% which shows that with π filter the output is almost pure d.c.

Here we are also using another formula $\gamma = \frac{5700}{L C_1 C_2 R_L}$ but condition is C_1, C_2 must be in μf, L in henries, R_L in Ω's

$\therefore \gamma = \frac{5700}{10\times 16\times 16\times 4000} = 5.56\times 10^{-4}$ = which is same as above.

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(2). Design a CLC or π – Section filter for $V_{dc} = 10V$, $I_L = 200mA$ and $\gamma = 2\%$.

$$R_L = \frac{V_{dc}}{I_L} = \frac{10}{200 \times 10^{-3}} = 50\Omega$$

$$\gamma = \frac{5700}{LC_1C_2 \times 50} = \frac{114}{LC_1C_2} \quad \left(\gamma = 2\% = \frac{2}{100} = 0.02\right)$$

$$0.02 = \frac{114}{LC_1C_2}$$

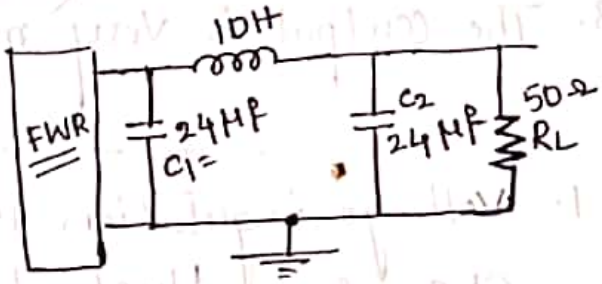
if we assume $L = 10H$, $C_1 = C_2 = C$ then

$$0.02 = \frac{114}{10 \times C^2} = \frac{11.4}{C^2}$$

$$C^2 = 570$$

$$C = \sqrt{570} \simeq 24\,\mu F$$

$\boxed{C = 24\,\mu f}$



(3) A FWR single phase employs a π section filter Consisting of two 4 μ·f Capacitances and a 20H choke. The transformer voltage to the centre tap is 300 V rms. The load current is 500 mA. Calculate the d.c output voltage and the ripple voltage. The resistance of the choke is 200Ω

$C_1 = C_2 = 4\,\mu f$, $L = 20H$, $V_{rms} = 300V$

$I_C = 500\,mA$, $R_2 = 200\Omega$,

Maximum value of Secondary voltage $V_{sm} = V_m = \sqrt{2} \times V_{rms}$

$= \sqrt{2} \times 300 = 424.2V$

Load resistance $R_L = \frac{V_{dc}}{I_{dc}} = 270\Omega$

(2) Ripple voltage $V_r = \frac{I_{dc}}{2fC} = \frac{500 \times 10^{-3}}{2 \times 50 \times 4 \times 10^{-6}} = 1.25\,mV$ (Assume $f = 50Hz$)

(1) DC output voltage $= V_{s(max)} - \frac{V_r}{2} - I_{dc}R_2$

$= 424.2 - \frac{1.25 \times 10^{-3}}{2} - (500 \times 10^{-3} \times 200)$

$= 324.19V$

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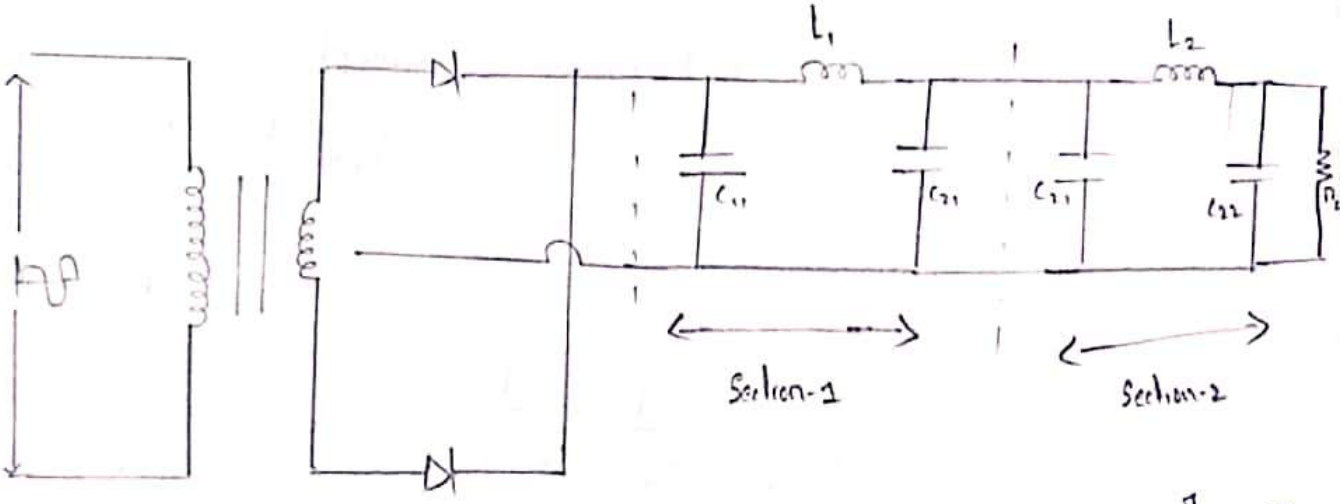
π Section / c.l.c filter / capacitor-input / c-filter followed by L-section



⇒ To obtain a pure dc more π sections may be used one after the another such a filter called as multiple π section filter

$$\text{Ripple factor } (\gamma) = \frac{\sqrt{2} \times C_{11} \times C_{21} \times C_{22}}{R_L \times 4 \times L_2}$$

For full wave rectifier with capacitor discharge

$$Q_{discharge} = Q_{charge}$$

$$I_{dc}\, I_2 = C_1 . V_{P-P}$$

$$V_{P-P} = \frac{I_{dc} \cdot T_2}{C_1} \quad (T_2 = T/2)$$

$$V_{P-P} = \frac{I_{dc}}{2fC_1} \rightarrow (1) \qquad T = \frac{1}{2f}$$

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$$v(t) = V_{dc} - \frac{V_{rp-p}}{\pi}\left(\sin(2\omega t) - \frac{\sin(4\omega t)}{2} + \cdots\right)$$

R.m.s value of Second harmonic component

$$V'_{rms} = \frac{V_m}{\sqrt{2}} = \frac{V_{rp-p}}{\pi\sqrt{2}}$$

$$= \frac{I_{dc}}{2\sqrt{2}fC_1\pi}$$

$$= \frac{2I_{dc}}{4\sqrt{2}fC_1\pi}$$

$$V'_{rms} = \sqrt{2}\, I_{dc} X_{C_1} \rightarrow (2)$$

$$X_{C_1} = \frac{1}{\omega C_1} = \frac{1}{2\omega C_1} = \frac{1}{2(2\pi f)C_1}$$

From voltage division rule:

$$V_{rms} = V'_{rms} \cdot \frac{X_{C_2}}{X_L + X_{C_2}} \qquad X_L >> X_{C_2}$$

$$= V'_{rms} \times \frac{X_{C_2}}{X_L}$$ Sub (2)

$$= \sqrt{2}\, I_{dc} \frac{X_{C_1} X_{C_2}}{X_L}$$

$$= \sqrt{2} \times \frac{V_{dc}}{R_L} \times \frac{X_{C_1} X_{C_2}}{X_L}$$

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Ripple factor (γ) = $\frac{V_{rms}}{V_{dc}}$

$$= \frac{\sqrt{2}\, V_{dc} X_{C_1} X_{C_2}}{R_L \times X_L}$$

$$= \frac{\sqrt{2}\, X_{C_1} X_{C_2}}{R_L X_L}$$

$X_{C_1} = \frac{1}{2\omega C_1}$ · $X_{C_2} = \frac{1}{2\omega C_2}$ $X_L = 2\omega L$

$$= \sqrt{2} \times \frac{1}{2\omega C_1} \times \frac{1}{2\omega C_2} \times \frac{1}{2\omega L} \times \frac{1}{R_L}$$

$$\gamma = \frac{\sqrt{2}}{8\omega^3 L C_1 C_2 R_L}$$

For π π Section $\gamma = \frac{\sqrt{2}\, X_{C_{11}} \cdot X_{C_{21}} \cdot X_{C_{22}} -- X_{C_{nn}}}{R_L X_{L_1} X_{L_2} ---- X_{L_n}}$

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COMPARISON OF FILTERS :

Parameter	Capacitor / C Filter	Choke input /L filter	LC filter	π / (CLC) type filter
Place of filter	Across the load	In series with the load	Across the load	Across the load
Useful in	Reducing ripple in load voltage	Reducing ripple in load current	Reducing ripple in load current	Reducing ripple in load voltage
Lowest ripple in the load voltage	No load or light loads	Heavy loads	All loads	No load or light loads
Suitable for	Light load applications	Heavy load applications	Light as well as heavy loads	All loads
Surge current through diodes	Very high and must be controlled	Low and need not to be controlled	Low and need not to be controlled	Low
Expression for ripple factor	RF= $1/4\sqrt{3}fCR$ Ripple-factor - γ	RF=$R/3\sqrt{2}\omega L$ γ =	RF=$R/6\sqrt{2}\omega^2LC$ γ =	RF=$1/2\sqrt{3}/(\omega^2LC_1C_2R_L)$
Size of filter	Small and compact	Bulky	Bulky	Bulky
Cost	Lowest	Moderate	Higher	Highest
Voltage regulation	Poor	Moderate	Good	Very good
Applications	Cell charger, small eliminators	High current dc power supplies	Dc power supplies	Dc power supplies

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TRANSISTOR CHARACTERISTICS

INTRODUCTION:

* Transistors are Solid-state devices used for amplifying Controlling and generating electrical Signals. They are used widely in electronic equipments such as pocket Calculators, Radios and also in Communication Satellites.

* In 1947, John Bardeen, Walter Brattin were the first to invent the "transistor" by adding another junction to a p-n junction diode which Could control the flow of majority Charge Carriers. Later in 1951 William Shockley made the modern version i.e., junction transistor. It is one of the greatest inventions of the 20th Century.

* The following are the advantages of transistors.

1. Low operating Voltage.
2. Higher efficiency.
3. Small Size.
4. Does not Require any filament power.

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TRANSISTOR:

Definition:- A transistor is a semiconductor device that Regulates Current or Voltage flow used to Switch or amplify the electronic Signals.

* Transistor is nothing but Transfer of Resistance. As it transfers the resistance from one Region to other Regions

* Transistor is a three terminal device, they are

1. Emitter
2. Base
3. Collector.

* TRANS-IS TOR
  - TRANS → transfer property
  - IS TOR → means resistance property offered to the junctions.

EMITTER:

* The terminal of the transistor which supplies or emits the charge carriers is called "Emitter" terminal.
* It is Heavily doped and moderate in size.
* It is always in forward bias with respect to base in order to supply charge carriers.
* Because of heavy doping it can supply large amount of charge carriers.

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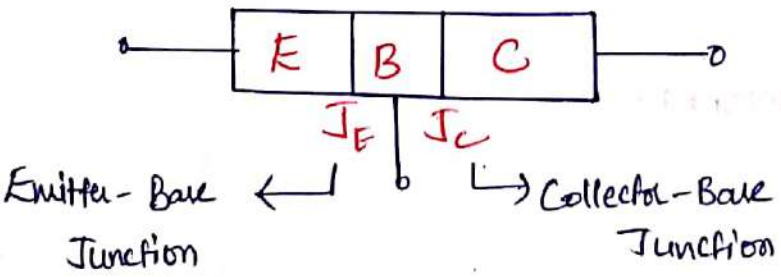
BASE:

* The terminal which lies in between Emitter and Collector is called Base terminal of the transistor.
* It is lightly doped and very thin in size.
* The charge carriers emitted by the emitter passes through the base.
* To reduce the recombination of charge carriers it is lightly doped.

COLLECTOR:

* The terminal which collects the emitted charge carriers by the Emitter is called "Collector" terminal.
* It is moderately doped and large in size.
* Emitter and collector are same type materials.
* The collected charge carriers generates heat, to dissipate this heat to the surroundings this region is made large.



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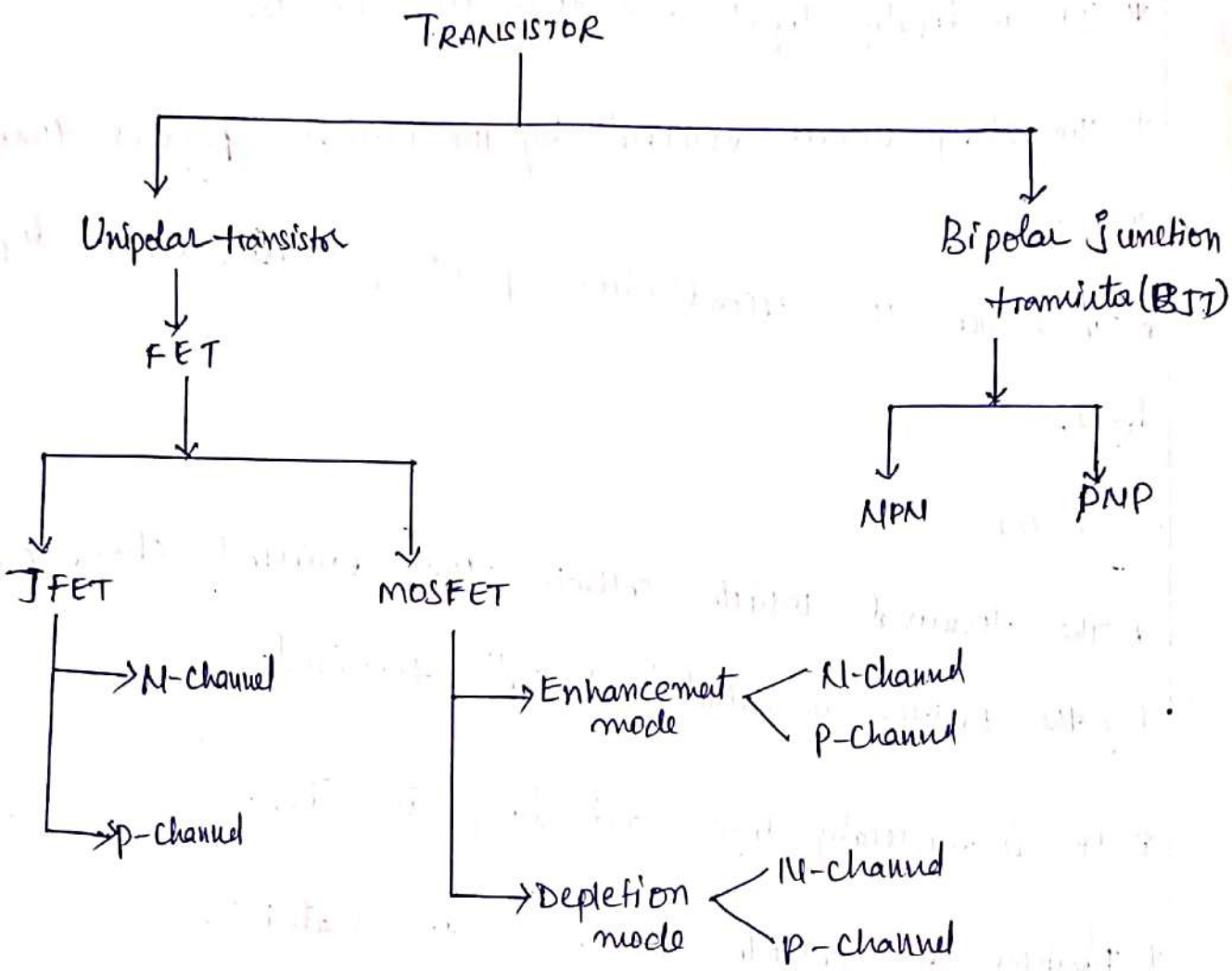
TYPES OF TRANSISTORS:

* Transistors are classified based on construction and usage of charge carriers.



UNIPOLAR TRANSISTOR:

* In unipolar transistor current conduction is due to only majority charge carriers.

Eg: FET's i.e., JFET's, MOSFET's..

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BIPOLAR JUNCTION TRANSISTOR:

* In Bipolar junction transistor (BJT's) current conduction is due to both majority and minority charge carriers.

* BJT is a current-controlled device because its output characteristics depends on the are determined by the input current.

Definition: A Bipolar junction transistor is a three terminal semiconductor device consisting of two P-N junctions which is able to amplify or magnify a signal.

* BJT is analogous to the vaccum triode and is comparitively small in size. It is used in amplifier and oscillator circuits and as a switch in digital circuits.

* Based on the construction it is classified into two types
  1. N-P-N Transistor.
  2. P-N-P Transistor.

NPN Transistor:

Definition: A thin layer of P-type material is sandwiched between two layers of N-type material then it is called as a NPN transistor.

* It is made up of Silicon or germanium crystal.

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SYMBOL:

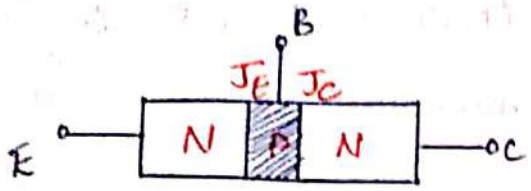

FIG: NPN transistor

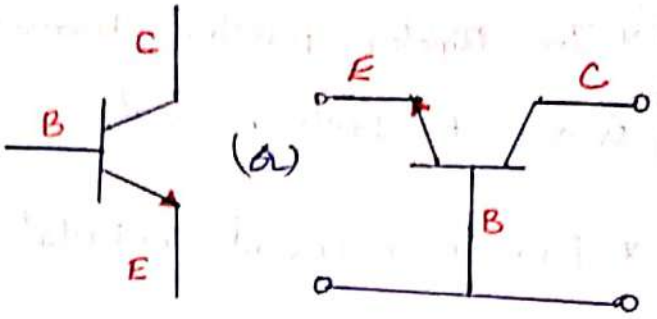

FIG: SYMBOL OF NPN TRANSISTOR.

* The arrow in the symbol indicates the direction of current flow when the Emitter-Base junction is forward biased.

PNP TRANSISTOR:

Definition: A thin layer of N-type material is sandwiched between two layers of P-type material then such type of transistor is called PNP transistor.

SYMBOL:

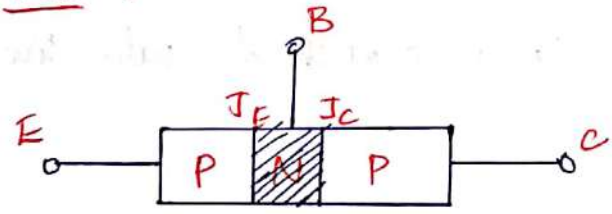

FIG: PNP TRANSISTOR

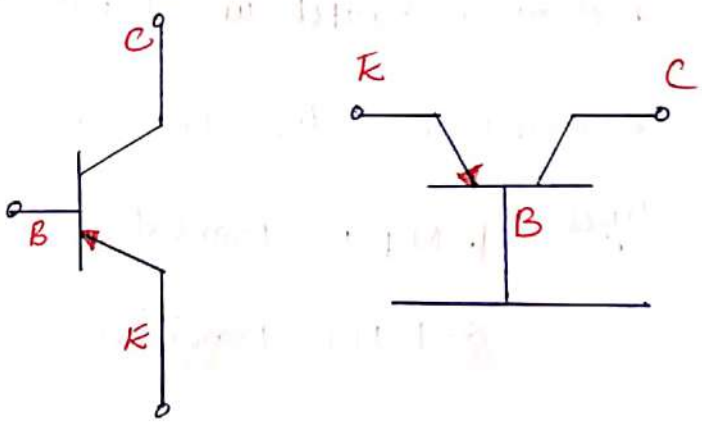

FIG: SYMBOL OF PNP TRANSISTOR.

DIODE-EQUIVALENT REPRESENTATION OF NPN & PNP TRANSISTORS:

* A transistor looks like two PN junction diodes connected back to back.

* It has two PN junctions.

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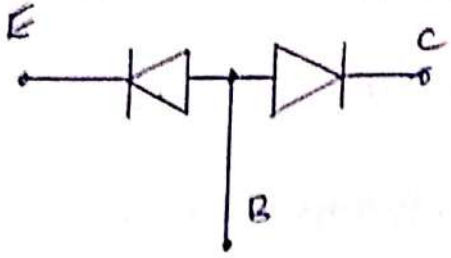
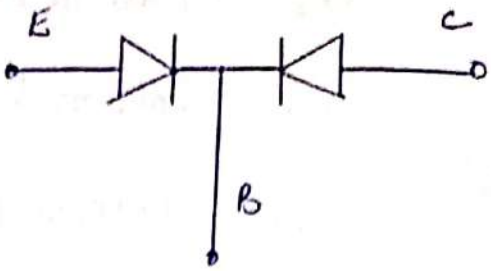


a) NPN



b) PNP

1. A junction between Emitter and Base is called as Emitter to Base junction (EB) & V_{BE} & simply "Emitter junction."

2. A junction between Collector and Base is called as Collector to Base junction & V_{BC} & "Collector junction".

CIRCUIT REPRESENTATION

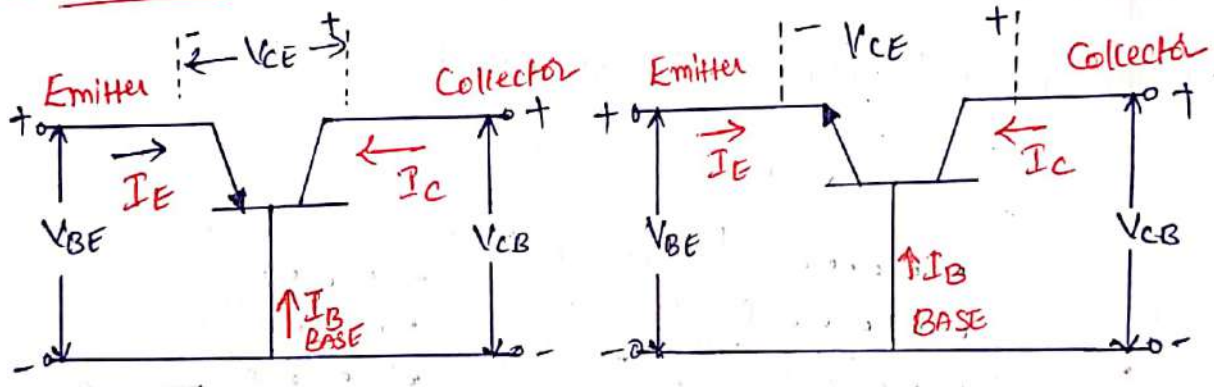


Fig: Circuit Representation of PNP & NPN Transistors

* The arrow on the Emitter lead specifies the direction of current flow when the Emitter-Base junction is forward biased.

I_E - Emitter current

I_B - Base current

I_C - Collector current.

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V_{BE} - Base to Emitter Voltage

V_{CB} - Collector to Base Voltage

V_{CE} - Collector to Emitter Voltage.

* V_{EB} represents the voltage drop from emitter to base.

UNBIASED TRANSISTOR:

* When External Voltage is not applied to the transistor then it is called Unbiased transistor.

* In NPN transistor, ~~free~~ electrons are the majority charge carriers and holes are the minority charge carriers in n-region and holes are the majority charge carriers and electrons are the minority charge carriers in P-region.

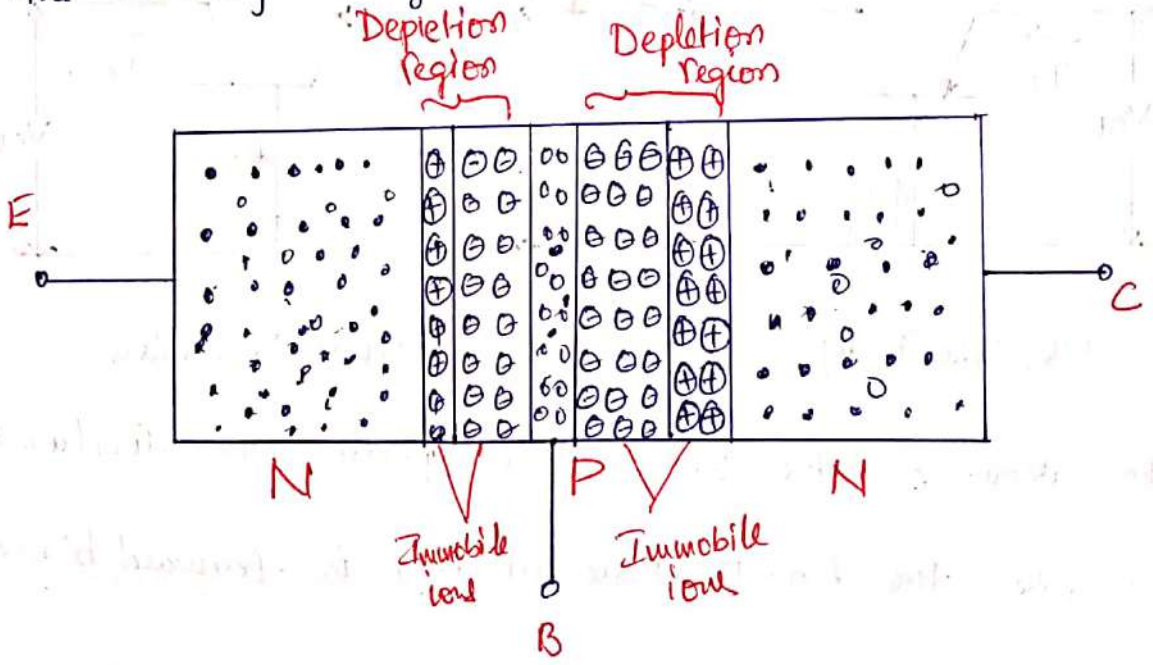

FIG: UNBIASED NPN TRANSISTOR.

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* Transistor is like a p-N junction diodes connected front to front (or) back to back.

* So two junctions are formed, they are Emitter junction and Collector junction.

* The junction between Emitter and base is called as "Emitter to base junction" or Input junction (or) Emitter junction.

* The junction between Collector and base is called as "Collector to base junction" (or) Collector junction (or) "output junction"

* At room temperature, the electrons in n-type (i.e., emitter region) move towards the base region and combine with the holes in base region thus forms the depletion region at emitter base junction.

* Similarly, the electrons in Collector region move towards the base region and combine with the holes in base region thus depletion region is formed at Collector base junction.

* The depletion region is more towards the base region than the emitter and Collector regions as shown in figure.

* This is because of heavy doping in Emitter and Collector regions than the base regions.

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BIASING OF TRANSISTORS (OR) OPERATING MODES OF TRANSISTOR:

* Transistor is operated in three modes depending on biasing voltage.

* In order to operate transistor properly as an Amplifier, it is necessary to correctly bias the two p-n junctions with external voltages.

* Depending on external bias voltage, polarities used, the transistor works in one of the three regions.

REGION	Emitter - Base Junction	Collector - Base Junction
Active	Forward biased	Reverse biased
Cut-off	Reverse biased	Reverse biased
Saturation	Forward biased	Forward biased

1. ACTIVE REGION:

* The region in which transistor Emitter to base junction is forward biased (V_{BE}) and Collector to base junction (V_{CB}) is Reverse biased then that region is called Active region.

* In Active region transistor acts as "Amplifier".

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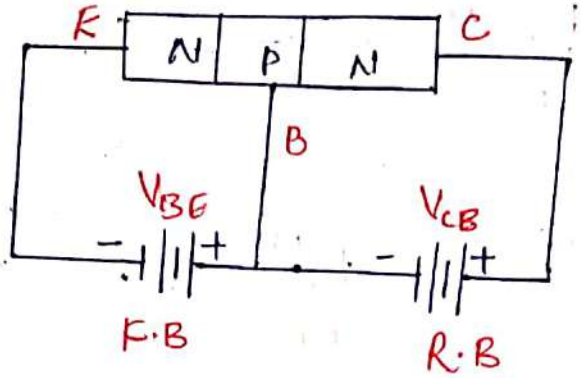
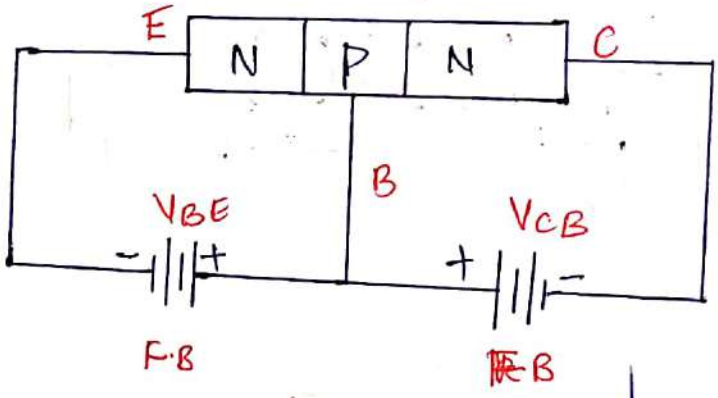


2. SATURATION REGION:

* The Region in which transistor, both emitter to base junction and collector to base junction are forward bias that Region is called "Saturation Region".

* In Saturation Region transistor acts as "ON" Switch.



3. CUT-OFF REGION:

* The Region in which transistor, both emitter to base junction and collector to base junctions are reverse biased, that Region is called "Cut-off Region"

* In Cut-off Region transistor acts as "OFF" Switch.

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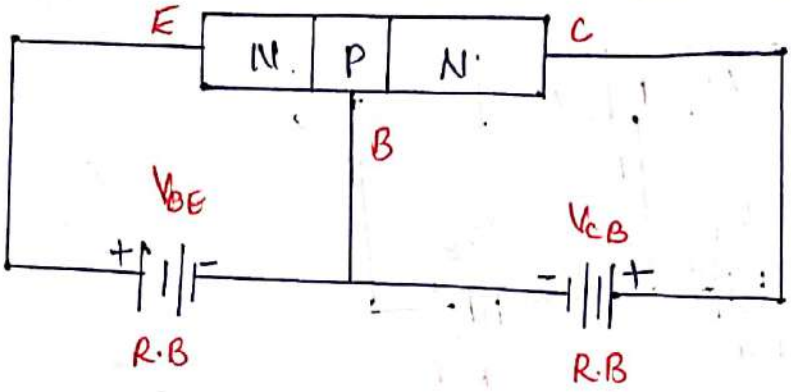

OPERATION OF AN NPN TRANSISTOR:

* NPN transistor with base to emitter junction in forward bias and Collector to emitter junction is reverse bias as shown below.

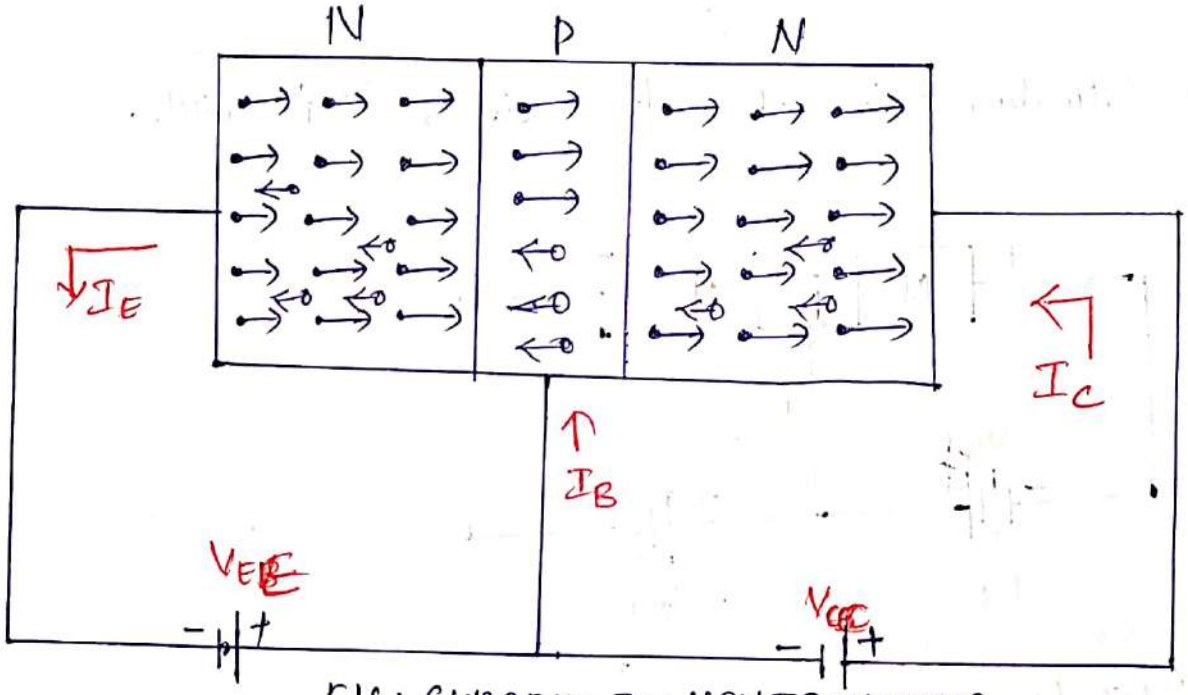

FIG: CURRENT IN NPN TRANSISTOR.

* The forward bias applied to the Emitter-base junction of an NPN transistor causes a lot of electrons from the emitter region to cross over to the base region.

* So, the majority carriers electrons in n-type flow towards the base and constitutes "Emitter Current" (I_E).

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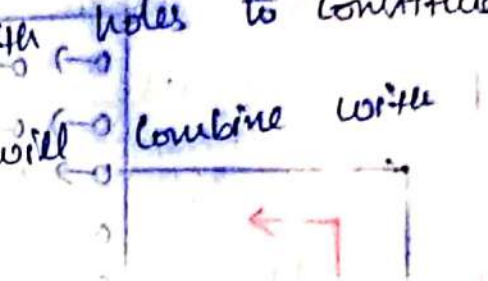
* The base is lightly doped with p-type material, the number of holes in the p-region is very small and hence, the number of electrons that combine with holes in the p-type region is also very small.

* Hence, a few electrons combine with holes to constitute a "Base Current" (I_B). i.e., only 5% will combine with holes in the base region.



* The remaining electrons (more than 95%) cross over into the Collector Region*

* Hence, these electrons constitute the "Collector Current" I_C.

* So, the electrons which are emitted by the Emitter, some combine with holes in p-region gives base current and remaining electrons reaches collector and constitutes Collector Current.

* Thus, Emitter current is the sum of base current and Collector current.

$$I_E = I_B + I_C$$

where I_E → Emitter Current

I_B → Base Current

I_C → Collector Current

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OPERATION OF PNP TRANSISTOR:

* In PNP transistor, base to emitter junction is forward bias and Collector to base junction is reverse biased.

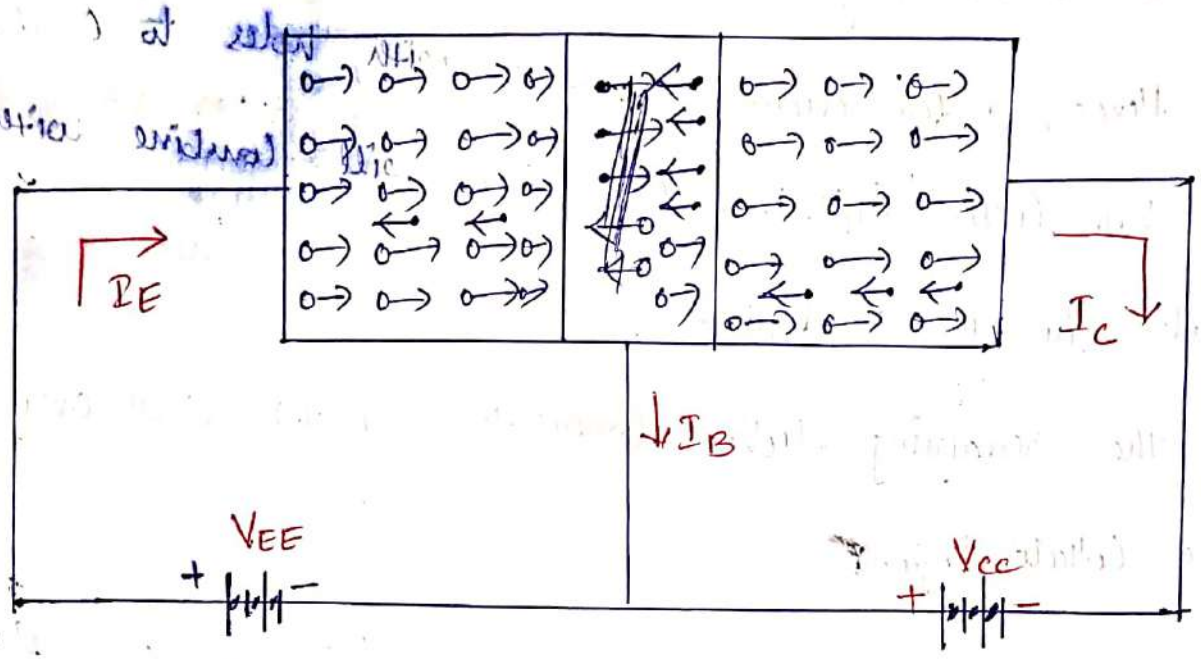

FIG: CURRENT IN PNP TRANSISTOR

* The forward bias applied to the Emitter-base junction of an PNP transistor causes a lot of holes from the emitter region to cross over to the base region.

* So, the majority carriers holes in p-type flow towards the base and constitutes "Emitter Current" (I_E).

* The base is lightly doped with n-type material, the number of elections in n-region is very small, and hence the number of holes that combine with elections also small in n-region.

* Hence, a few holes combine with elections to constitute a "Base Current" i.e., only 5% will combine with elections in n-region

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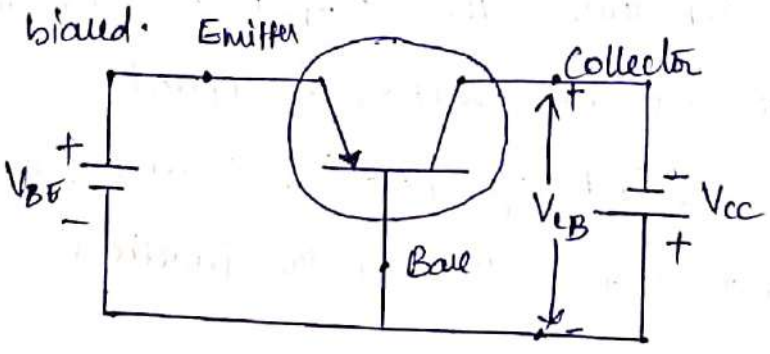
* The remaining holes (more than 95%) cross over into the collector region.
* Hence, these holes constitutes the "collector current" I_C.
* So, the holes which are emitted by the Emitter, some of them combined with the electrons in base region, which gives base current and remaining holes reaches collector and constitutes collector current.
* Thus, Emitter current is sum of base current and collector current.

$$I_E = I_B + I_C$$

where I_E is Emitter current
I_B is Base current
I_C is collector current.

POTENTIAL DISTRIBUTION THROUGH A TRANSISTOR.

* Consider a p-n-p transistor with emitter to base junction is forward biased and collector to base junction is reverse biased.



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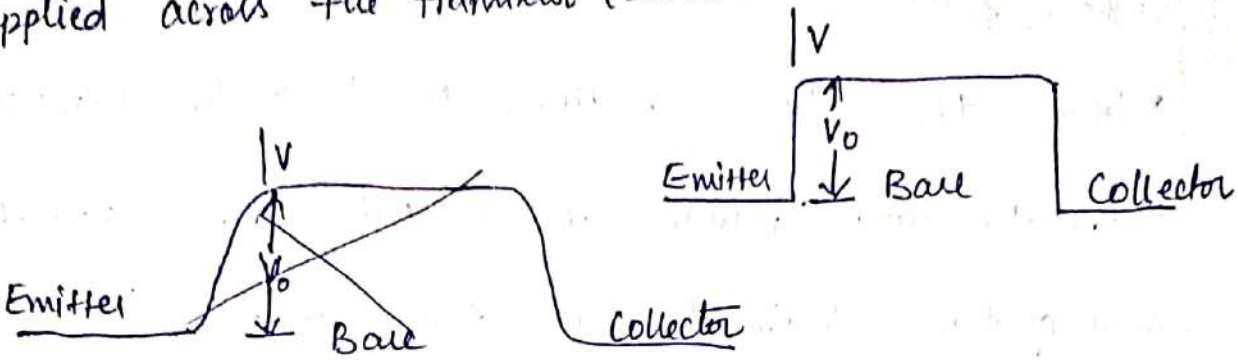
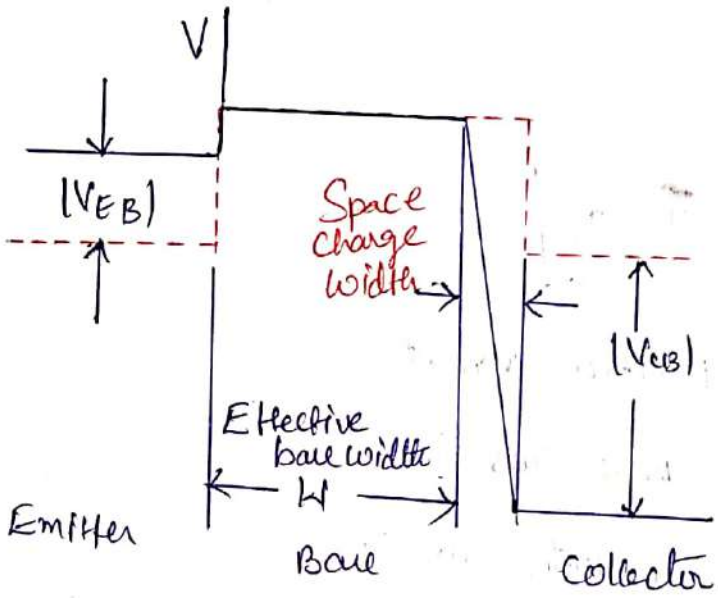
* Fig(b) represents the variation of potential when no voltage is applied across the transistor (unbiased).



fig(b): Variation of potential for unbiased transistor

* The potential variation of biased transistor is as follows.



Fig(c) potential variation of biased PNP transistor

* In fig(c) dashed curve represents the case before the external voltage is applied.

* The solid curve represents the output or variation of potential when the external voltage is applied.

* "V_0" represents the height of potential barrier (may be of few volts) so that no current flows through the junction.

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* If an external voltage is applied, the forward biased emitter-base junction lowers the emitter-base potential by $|V_{EB}|$, where as the reverse biased collector to base junction increases the collector-base potential by $|V_{CB}|$.

* Due to lowering the emitter-base potential it permits the emitter current to increases and holes are injected to base region.

* The potential is constant across the base region, and the injected holes diffuse across the n-type material to the collector-base junction.

* The holes which reach this junction fall down the potential barrier and all therefore collected by the collector i.e., the potential barrier falls across $|V_{CB}|$.

CURRENT COMPONENTS IN TRANSISTOR:

* Let us consider a p-n-p transistor, various current components flow across the forward biased emitter junction and reverse biased collector junction

* the below figure represents the various current components for a forward biased EB junction and reverse biased CB junction.

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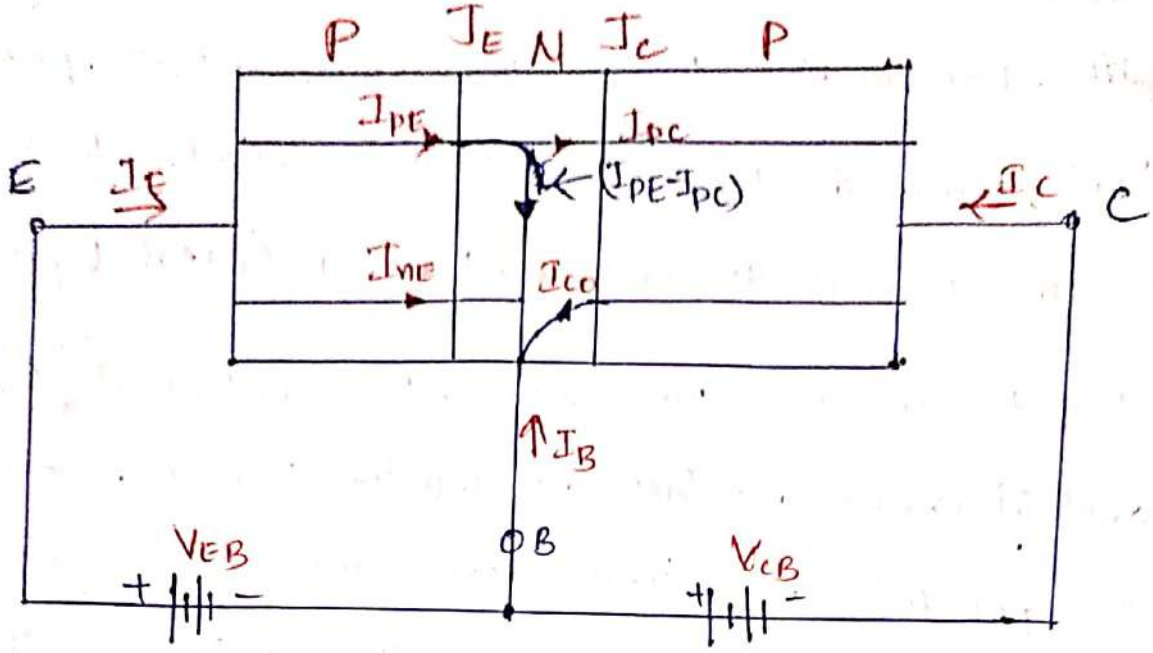

* Emitter current consists of 1. Hole current I_{PE} constituted by holes (Holes crossing from Emitter to base)

2. Electron current I_{NE} constituted by electrons (e^- crossing from base to emitter).

∴ Total Emitter current is given by,

$$I_E = I_{PE}(\text{majority}) + I_{NE}(\text{minority}) \longrightarrow (1)$$

* The holes crossing the emitter-base junction I_E and reaching the collector base junction I_C constitutes collector current I_{PC}.

* But all the holes crossing the base junction cannot reach the collector base junction I_C, because some of the holes will combine with electrons in base region

* Since, base width is small, so only small amount of holes are recombined with electrons. This constitutes base current $I_{PE} - I_{PC}$.

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* If the emitter is open-circuited so that $I_E = 0$, then I_{pc} would be zero. Under these circumstances the base and collector would act as a reverse biased diode, the reverse saturation current I_{co} flows.

where $\boxed{I_{co} = I_{nco} + I_{pco}}$ → (2)

where I_{co} - Reverse Saturation Current

I_{pco} → Current caused by the holes moving from p-region to N-region.

I_{nco} → Current caused by the electrons moving from N-region to p-region.

In general, it is represented as, $I_c = I_{nc} + I_{pc}$

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PARAMETERS OF CURRENT COMPONENTS:

1. EMITTER EFFICIENCY (γ):

Definition: The Ratio of Current of injected carriers at Emitter – base junction (I_E) to the total emitter current is defined as the "Emitter efficiency" (γ).

$$\text{Emitter Efficiency } \gamma = \frac{\text{Current of injected carriers at } I_E}{\text{Total Emitter Current}}$$

In Case of p-n-p transistor

$$\gamma = \frac{I_{PE}}{I_{PE} + I_{nE}}$$

Where $I_E = I_{PE} + I_{nE}$

$$\boxed{\gamma = \frac{I_{PE}}{I_E}}$$

Where I_{PE} is Injected hole diffusion current at emitter junction

I_{nE} is Injected electron diffusion current at emitter Junction.

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2. TRANSPORT FACTOR (β^*):

Definition: The Ratio of injected carrier current reaching at collector junction J_c to the injected carrier current at emitter base junction J_E.

$$\beta^* = \frac{\text{Injected carrier current at } J_c}{\text{Injected carrier current at } J_E}$$

In case of p-n-p transistor

$$\boxed{\beta^* = \frac{I_{pc}}{I_{pE}}}$$

3. LARGE SIGNAL CURRENT GAIN (α):

Definition: The ratio of current due to injected carriers I_{pc} to the total emitter current I_E.

$$\alpha = -\frac{(I_C - I_{CO})}{I_E}$$

where $I_C = I_{CO} - I_{pc}$

$$I_{pc} = I_{CO} - I_C$$

$$\boxed{\alpha = \frac{I_{pc}}{I_E}} \longrightarrow (1)$$

* α ranges from 0.90 to 0.995 and it is positive.

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dividing eq (1) bgth numerator and denominator by I_{PE}

$$\alpha = \frac{I_{PC}}{I_{PE}} * \frac{I_{PE}}{I_E}$$

$$\alpha = \beta^* * \gamma \qquad \left(\because \beta^* = \frac{I_{PC}}{I_{PE}} \text{ \& } \gamma = \frac{I_{PE}}{I_E}\right)$$

∴ The relation between α, β & γ is given by,

$$\boxed{\alpha = \beta^* \gamma}$$

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TYPES OF TRANSISTOR AMPLIFIER CONFIGURATIONS:

* When a transistor is to be connected in a circuit, one terminal is used as an Input terminal, the other terminal is used as an output terminal and the third terminal is common to both the input and output terminals.

* Depending upon the input, and output and common terminal a transistor amplifier can be connected in three configurations

* They are 1) Common Base (CB) Configuration
2) Common Emitter (CE) Configuration
3) Common Collector (CC) Configuration

* Transistor acts as Amplifier in Active mode.

1. COMMON BASE (CB) CONFIGURATION:

Definition: The Configuration in which emitter acts as Input terminal, Collector as the output terminal and base terminal is Common for both input and output terminals then such Configuration is said to be Common Base (CB) Configuration.

* Common Base Configuration is also called as "Grounded Base Configuration".

*

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CIRCUIT DIAGRAM :

* Transistor works as an Amplifier in its Active mode of operation.

* So, while Representing amplifier configurations the Emitter junction must be forward biased and Collector junction must be Reverse biased.

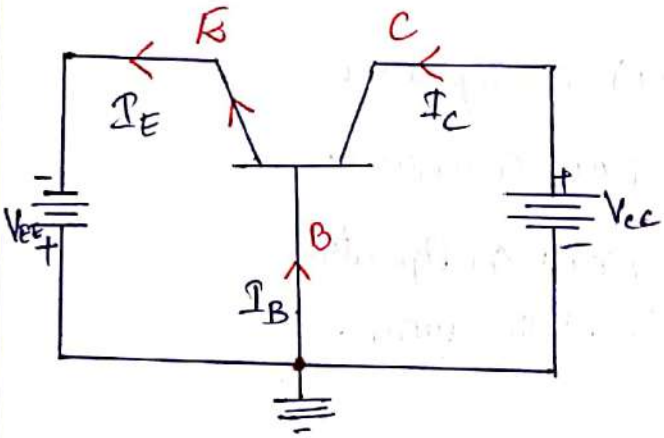

FIG: CB CONFIGURATION FOR NPN TRANSISTOR

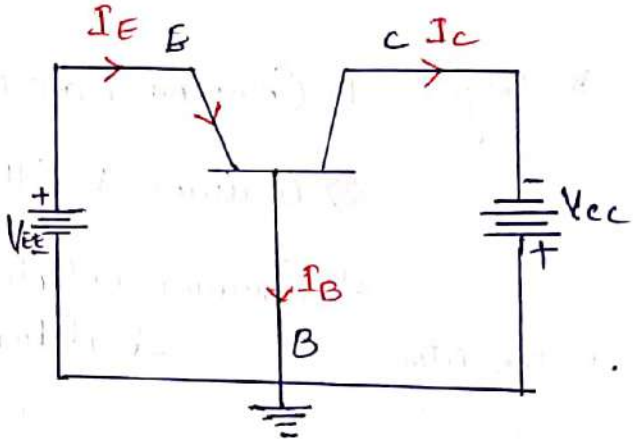

FIG: CB CONFIGURATION FOR PNP TRANSISTOR

* The fundamental relation between Emitter, base and Collector Currents is given by

$$I_E = I_B + I_C$$

* According to transistor equation

$$I_C = -\alpha I_E + I_{CBO}\left(1 - e^{V_C/V_T}\right)$$

where I_{CBO} is the reverse saturation current flowing in CB Configuration

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∵ I_{CBO} is very much less than the emitter current.

$$I_{CBO} << I_E$$

$$I_C = -\alpha I_E$$

$$\boxed{\alpha = -\frac{I_C}{I_E}}$$

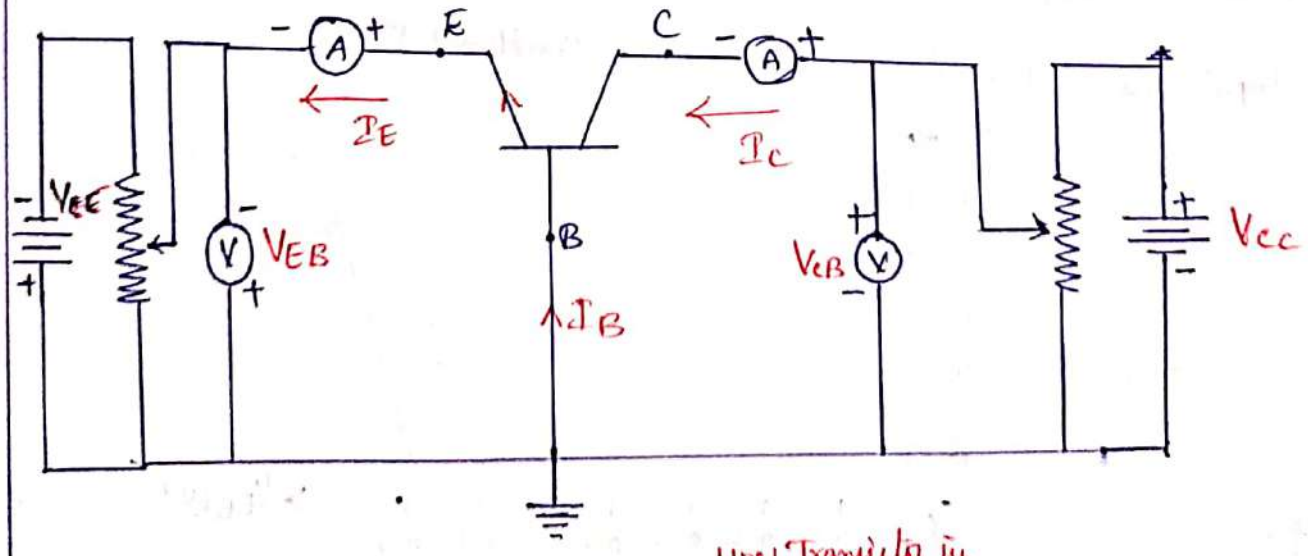
where α values ranges from 0.95 to 0.98 which is +ve.

CURRENT AMPLIFICATION FACTOR:

Definition: The Ratio of Change in output current to the Change in Input Current is known as the Current Amplification factor.

$$\boxed{\alpha = \frac{\Delta I_C}{\Delta I_E}}$$

CIRCUIT DIAGRAM TO DETERMINE STATIC CHARACTERISTICS:



NPN Transistor in

FIG: CIRCUIT DIAGRAM OF CB CONFIGURATION

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* The working of CB configuration can be explained with the help of Static Characteristic Curves.

INPUT CHARACTERISTICS:

Definition: The graphical Representation of Input currents to the I/p Voltages i.e (V-I Characteristics)

* In CB Configuration, INPUT terminal - Emitter
  COMMON terminal - Base
  OUTPUT terminal - Collector

* Input Current - I_E
  Input Voltage - V_{EB}
  Output Current - I_C
  Output Voltage - V_{CB}

Definition: The Graphical representation which explains the Relation between Input Current and Input Voltage is said to be Input Characteristics of the CB Configuration.

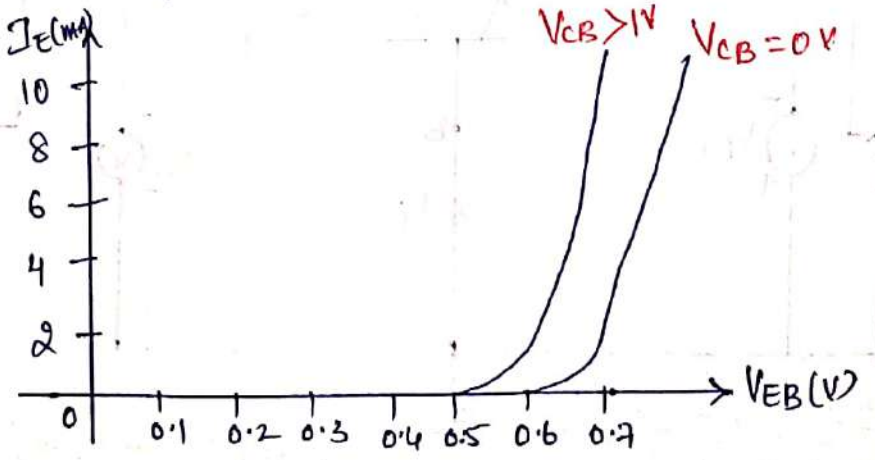

FIG: CB INPUT CHARACTERISTICS

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* To determine the Input Characteristics,

1. The Collector to Base Voltage (V_{CB}) is kept constant at 0V.
2. The Emitter Current I_E is increased by increasing the Emitter to base Voltage (V_{EB}) in suitable steps.
3. This is repeated for higher values of V_{CB}.
4. A curve is drawn between Emitter current I_E and Emitter - base Voltage (V_{EB}) at constant Collector to Base Voltage (V_{CB}).

* CASE : 1 When $V_{CB} = 0V$

* When Collector to base Voltage is zero volts and the Emitter-Base junction is forward biased, the Emitter junction (J_E) behaves as a forward biased PN diode.
* So, Emitter Current I_E increases rapidly with small increase in Emitter - Base Voltage (V_{EB}).
* When V_{EB} exceeds the cut-in voltage then the emitter current increases rapidly for a small change in emitter to base Voltage (V_{EB}).

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Case:2 When $V_{CB} > 1V$

* When collector-base voltage is increased more than zero volts by keeping V_{EB} constant.
* The curve shifted towards left as shown in the Input characteristics when V_{CB} is increased.
* This effect is due to the decrease in width of the Base region, because of this I_E also increases.
* This effect is called Early effect or Base width modulation.

OUTPUT CHARACTERISTICS:

Definition: The Graphical Representation which explains the Relation between output current I_C and output voltage V_{CB} is said to be output characteristics of CB Configuration.

* In CB Configuration, Output current I_C
  Output voltage V_{CB}.
* To determine output characteristics,

1) The Emitter current I_E is kept constant at a suitable value by adjusting the emitter-base voltage V_{EB}.
2) Then Collector to Base voltage V_{CB} is increased in suitable steps and the collector current I_C is noted.

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3) This is repeated for different fixed values of I_E.

4) Now the curves of I_C Vs V_{CB} are plotted for constant values of I_E.

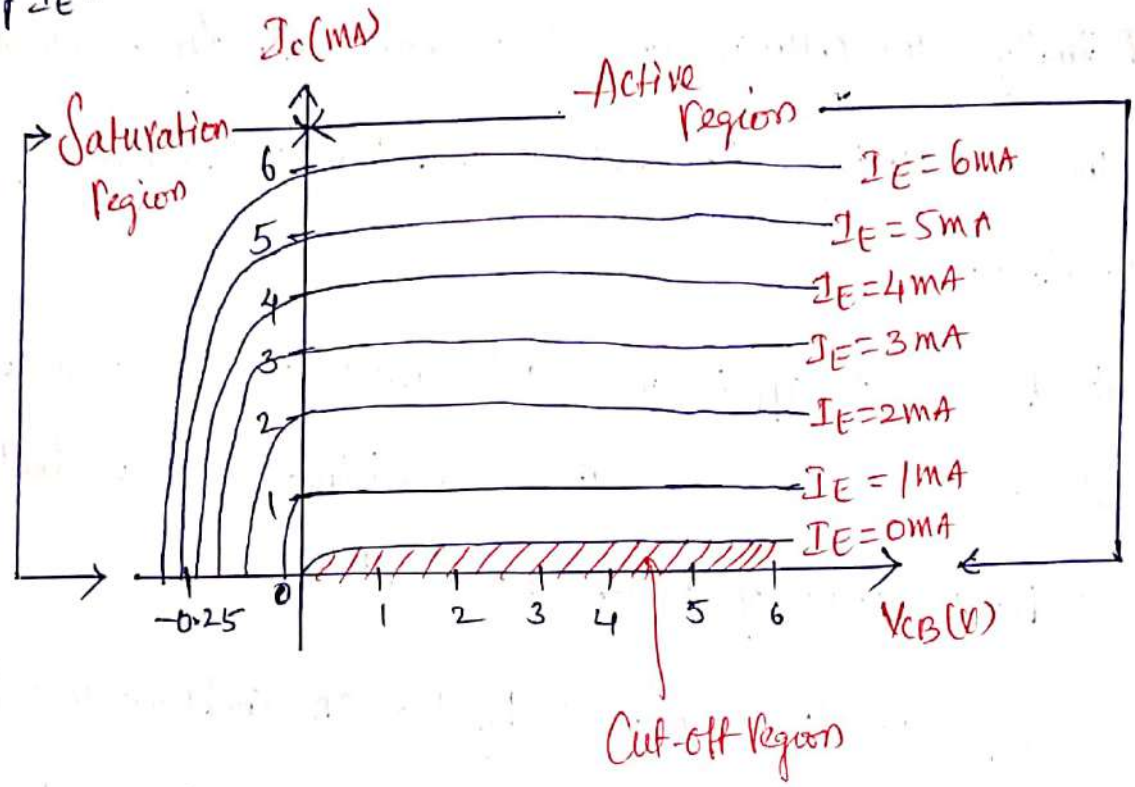

FIG: CB OUTPUT CHARACTERISTICS

* The output characteristics can be divided into three Regions
1. Active Region
2. Cut-off Region
3. Saturation Region.

ACTIVE REGION:

* In active region, the collector-base junction is reverse biased and Emitter-base junction is forward biased.

* The collector current (I_C) is almost independent of the Collector-base voltage (V_{CB}) and depends on the value of the

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Emitter current I_E.

* Therefore, the output characteristics are straight parallel lines in the active region.

* Actually the collector current increases slowly with the collector-base voltage (around 0.5 V). This is because of the early effect.

* But for most applications this increase in collector current can be ignored and it is considered as constant for a fixed value of Emitter current (I_E).

* The output resistance offered by the CB configuration is very high as a very large change in the collector-base voltage produces a very small change in the collector current.

* ~~When the emitter current~~ is zero ~~($I_E = 0$)~~

Cut-off Region:

* In cut-off region both the Emitter-base junction and collector to base junction are Reverse biased.

* When both the junctions are reverse biased they act as a reverse biased diodes.

* In this condition $I_E = 0$ because of this there is no current flow theoretically zero current.

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* But practically because of minority charge carriers small 16 amount of current flows that current is called as Reverse Saturation Current I_{CBO}.

* This Reverse Saturation Current I_{CBO} Increases Rapidly with Increase in temperature.

* The dashed lines below $I_E = 0$ mA curve represents the cut-off region in the o/p characteristics curve.

* In this region, transistor doesn't Conduct.

SATURATION REGION:

* In Saturation Region, both the collector-to base junction and Emitter-to base junctions are forward biased.

* The region left to the $V_{CB} = 0$ V line corresponds to the Saturation Region in the characteristic curve.

* From the figure, the collector-base voltage is ~~Negative~~ slightly Negative in the saturation region, this is because the collector-to-base junction is also forward biased.

* There is an exponential increase in the collector current with a small increase in the collector-base voltage.

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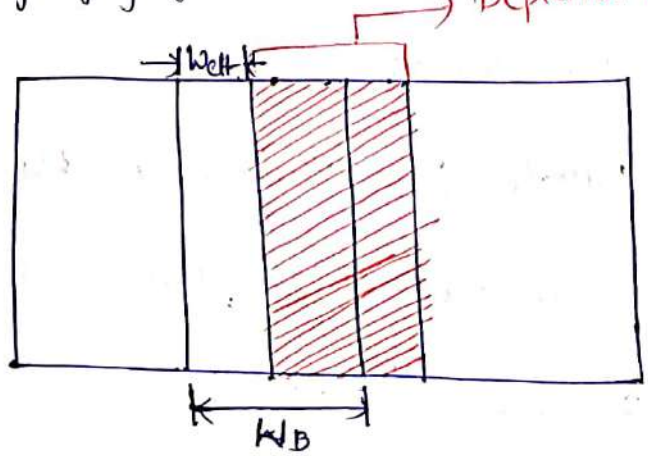
EARLY EFFECT OR BASE-WIDTH MODULATION:

* In I/P characteristic curves of configurations the curve shift left towards the curve, this is because of "Early effect" or "Base-width modulation".

DEFINITION: The Variation in the effective width of the Base Region in a Bipolar junction transistor due to a variation in the applied Reverse biased Collector to base voltages at the Collector junction is called "Early Effect" or "Base-Width modulation".

* Basically, Base is a lightly doped Region in the BJT. When Collector to base junction is Reverse biased the width of the depletion Region is more.
* This depletion Region is penetrated more into the base Region because of lightly doping of base Region.



* As the Collector Voltage V_{cc} is made to increase the Reverse bias, the space charge width i.e., Depletion Region width tends to increase.

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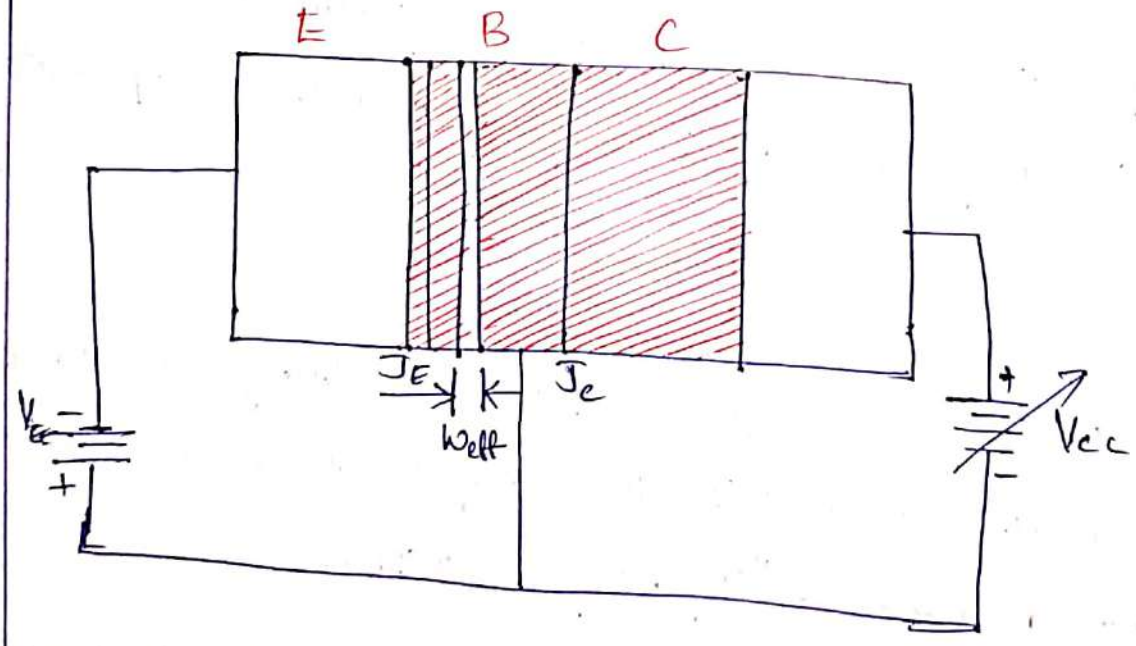
* According to transistor construction, base region is made very thin and very lightly doping.

* Because of this increase in reverse bias voltage, it tries to penetrate more into the base region which reduces the effective depletion region. Electrical width of the Base.

* At the Emitter junction, this reduction in base width affects the barrier potential among the depletion region.

* This barrier potential at the J_E junction also decreases because of this I_E also increases and enters into conduction earlier.



* This dependency of base width on collector to base voltage is known as Early effect.

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* This decrease in Effective base-width has three consequences.

1. There is less chance for recombination within the base region. Hence α increases with increasing $|V_{CB}|$.

2. The charge gradient is increased within the base, and consequently, the current of minority carriers injected across the emitter junction increases.

3. For extremely large voltages, the effective base width may be reduced to zero, causing voltage breakdown in the transistor. This phenomenon is called the punch through.

TRANSISTOR PARAMETERS:

* The slope of the CB characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as base hybrid parameters or h-parameters.

1. INPUT IMPEDANCE (h_{ib}):

Definition: The ratio of change in input emitter voltage to the change in input emitter current with the output collector to base voltage as constant is defined as "Input Impedance" (h_{ib}).

$$\text{Input Impedance } h_{ib} = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right|_{V_{CB}=\text{Constant}}$$

* CB configuration has low input impedance. The typical value of h_{ib} ranges from 20 Ω to 50 Ω.

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2. OUTPUT ADMITTANCE *[h_{ob}]:-

Definition: The ratio of change in the output collector current to the corresponding change in the output collector voltage with the input emitter current I_E kept constant is defined as output admittance (h_{ob}).

$$h_{ob} = \left.\frac{\Delta I_C}{\Delta V_{CB}}\right|_{I_E = \text{Constant}}$$

* The typical value of this parameter is of the order of 0.1 to 10 μmhos.

3. FORWARD CURRENT GAIN (h_{fb}):

Definition: The ratio of change in the output collector current to the corresponding change in the input emitter current keeping the output collector voltage V_{CB} constant is defined as Forward current gain.

$$h_{fb} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB} = \text{Constant}}$$

* Its typical value ranges from 0.9 to 1.0

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4. REVERSE VOLTAGE GAIN: (h_{rb}):-

Definition: The ratio of Change in the input emitter Voltage and the corresponding Change in output collector Voltage with constant input emitter Current I_E is defined as Reverse Voltage Gain (h_{rb}).

$$h_{rb} = \left.\frac{\Delta V_{EB}}{\Delta V_{CB}}\right|_{I_E = \text{Constant}}$$

* Its typical value is of the order of 10^{-5} to 10^{-4}.

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2. COMMON EMITTER (CE) CONFIGURATION:

Definition: The configuration in which base acts as Input terminal of Collector as the output terminal and Emitter terminal is common for both i/p and o/p terminals such configuration is called as "Common Emitter Configuration."

* Common Emitter configuration is also called as "Grounded Emitter Configuration".

CIRCUIT DIAGRAM

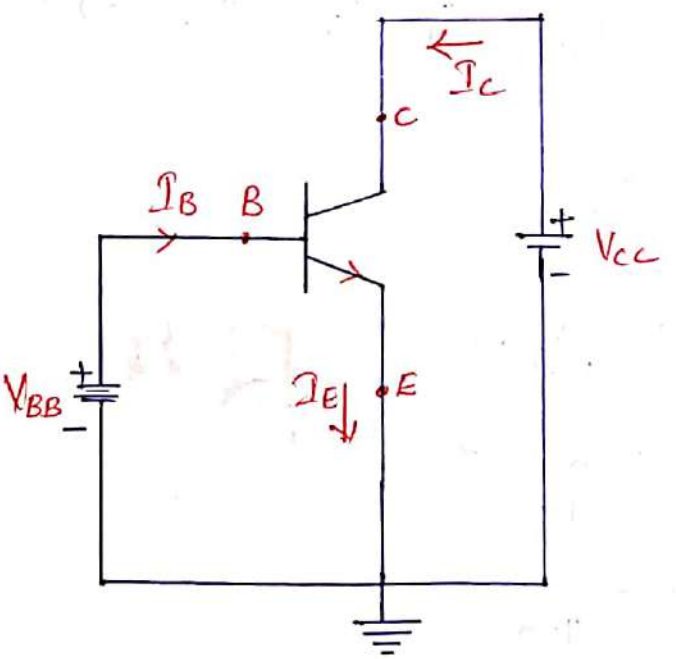

FIG: CE CONFIGURATION FOR NPN TRANSISTOR

RELATION BETWEEN I/P & O/P CURRENTS:

→ In CE configuration, Input current is I_B and o/p current is I_C

From fundamental relation of currents in transistor

$$I_E = I_B + I_C \longrightarrow (1)$$

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$$I_C = \alpha I_E + I_{CBO} \longrightarrow (2)$$

Substituting eq(1) in eq(2)

$$I_C = \alpha (I_C + I_B) + I_{CBO}$$

$$I_C = \alpha I_C + \alpha I_B + I_{CBO}$$

$$I_C - \alpha I_C = \alpha I_B + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO} \rightarrow (3)$$

$\because \beta = \frac{\alpha}{1-\alpha}$

$$\beta + 1 = \frac{\alpha}{1-\alpha} + 1$$

$$= \frac{\alpha + 1 - \alpha}{1 - \alpha}$$

$$\beta + 1 = \frac{1}{1-\alpha}$$

$\therefore$ equation (3) becomes

$$I_C = \beta I_B + (1+\beta) I_{CBO} \rightarrow (4)$$

* In CE Configuration, I_b is the i/p current and I_C is the o/p current.

* If the base circuit is open i.e., $I_B = 0$, then a small collector current flows from the collector to emitter. This is denoted by I_{CEO}.

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∴ Equation (4) becomes

$$I_C = \beta I_B + I_{CEO}$$

Where $I_{CEO} = (1+\beta) I_{CBO}$

Since $I_B >> I_{CEO}$

$$I_C = \beta I_B$$

$$\beta = \frac{I_C}{I_B}$$

CURRENT AMPLIFICATION FACTOR:

Definition: The ratio of change in o/p current (I_C) to the change in i/p current (I_B) is defined as current amplification factor

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

Relation between α & β:

By definition $I_C = \alpha I_E$

$$I_E = I_B + I_C$$

$$I_E = I_B + \alpha I_E$$

$$I_E - \alpha I_E = I_B$$

$$I_B = (1-\alpha) I_E \rightarrow (1)$$

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Dividing both sides of eq(1) by I_C, we get

$$\frac{I_B}{I_C} = \frac{I_E}{I_C}(1-\alpha)$$

$$\frac{1}{\beta} = \frac{1}{\alpha}(1-\alpha)$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

$$\boxed{\alpha = \frac{\beta}{1+\beta}}$$

$(\because \beta = \frac{I_C}{I_B}$

$\frac{1}{\beta} = \frac{I_B}{I_C}$

$\because \alpha = \frac{I_C}{I_E}$

$\frac{1}{\alpha} = \frac{I_E}{I_C}$

INPUT CHARACTERISTICS:

DEFINITION: The Graphical Representation which explains the relation between I/p current (I_B) and I/p voltage (V_{BE}) is said to be the Input characteristics of CE Configuration.

* In CE configuration, I/p terminal - BASE
  Common terminal - EMITTER
  O/p terminal - COLLECTOR

∴ Input current - I_B
Input Voltage - V_{BE} (Base to Emitter Voltage)

output current - I_C
output Voltage - V_{CE} (Collector to Emitter Voltage)

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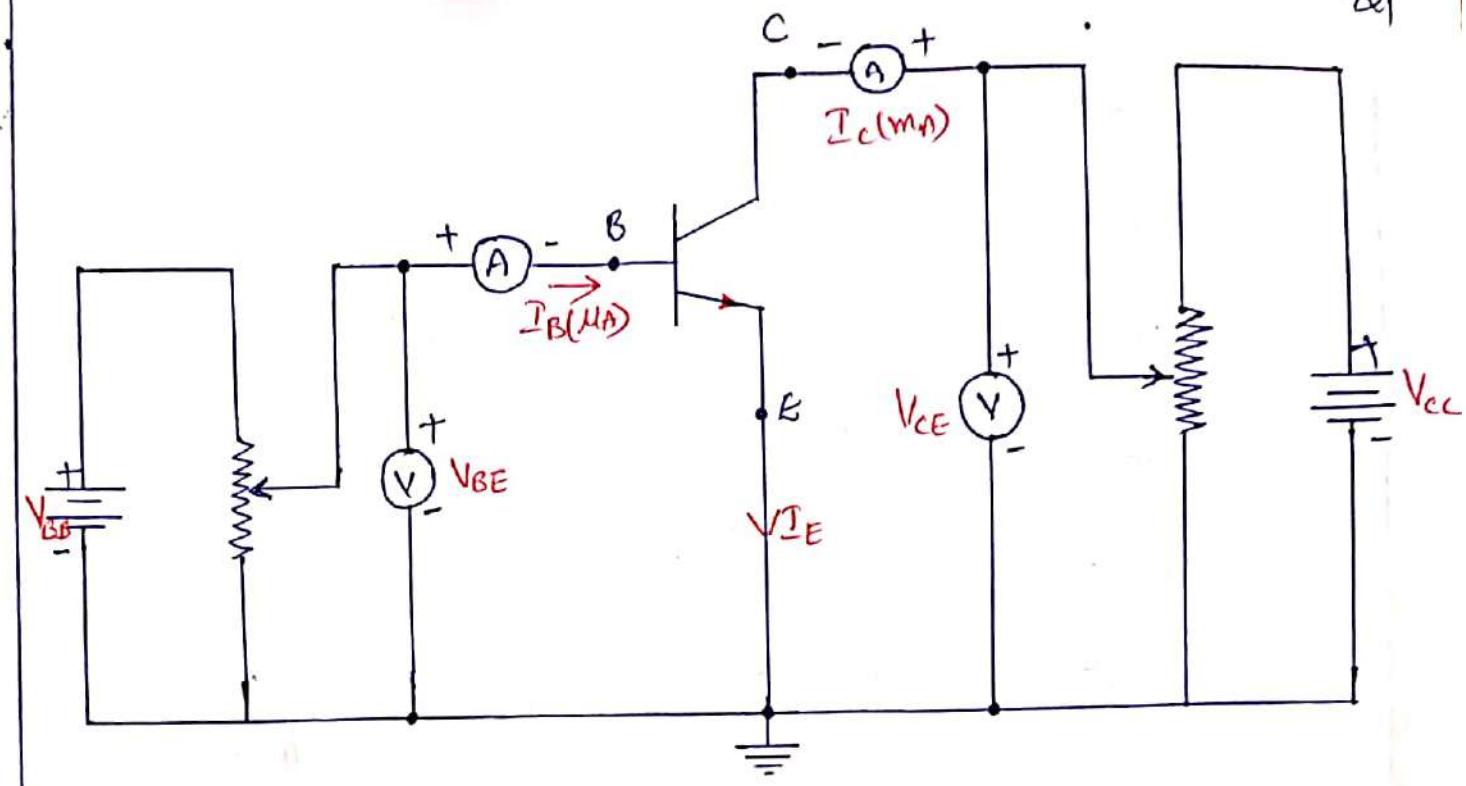

FIG: CIRCUIT TO DETERMINE CE STATIC CHARACTERISTICS

* To determine Input Characteristics,

1) Keep the output Voltage i.e., Collector to ~~base~~ Emitter Voltage (V_{CE}) Constant at zero volts.

2) Increase the Input current i.e, base current in equal steps from zero by increasing Input Voltage i.e, Base to Emitter Voltage V_{BE}.

3) Note the corresponding V_{BE} and I_B values.

4) This procedure is repeated for higher fixed values of V_{CE} and the curves of I_B Vs V_{BE} are drawn.

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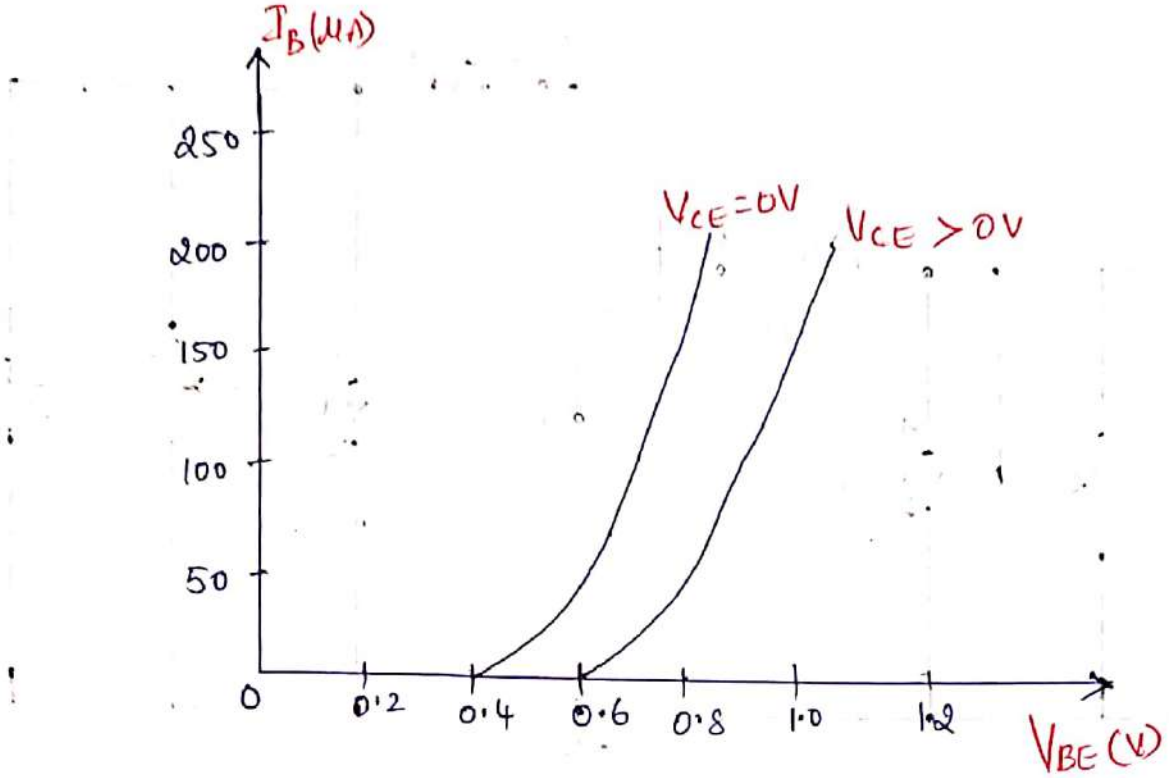

FIG: CE INPUT CHARACTERISTICS.

CASE:1 When V_{CE}=0V

* When V_{CE}=0V, the emitter-base junction is forward biased and the junction behaves as a forward biased diode.

* Hence the Input characteristic curve for V_{CE}=0V will be similar to that of a forward biased diode.

* The current (I_B) increases exponentially when V_{BE} exceeds the cut-in voltage.

Case:2 when V_{CE}>0V

* When collector to emitter voltage (V_{CE}) is increased, the width of the depletion Region at the reverse biased collector-base junction will also increases.

* Because of this, effective width of the base decreases.

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* This effect causes a decrease in the base current I_B.
* Hence to get the same value of I_B for $V_{CE} = 0$, V_{BE} should be increased.

(Eg: $V_{BE} = 0.4$, $I_B = 0\mu A$; $V_{BE} = 0.6$, $I_B = 0\mu A$).

* As a result the curve shifts to right as V_{CE} increases.

OUTPUT CHARACTERISTICS:

DEFINITION: The Graphical Representation which explains relation between output current I_C and output voltage V_{CE} by keeping I/P current I_B constant is said to be "Output characteristics of CE configuration"

* In CE configuration, output current is collector current (I_C) and output voltage is collector to Emitter voltage (V_{CE}).
* To determine the output characteristics,

1) Keep the base current I_B constant at a suitable value by adjusting base-emitter voltage V_{BE}.
2) Increase the collector to emitter voltage (V_{CE}), from zero and note the corresponding collector current values (I_C).
3) Repeat the same procedure for different fixed values of I_B.
4) Now the curves of I_C Vs V_{CE} are plotted for constant values of I_B.

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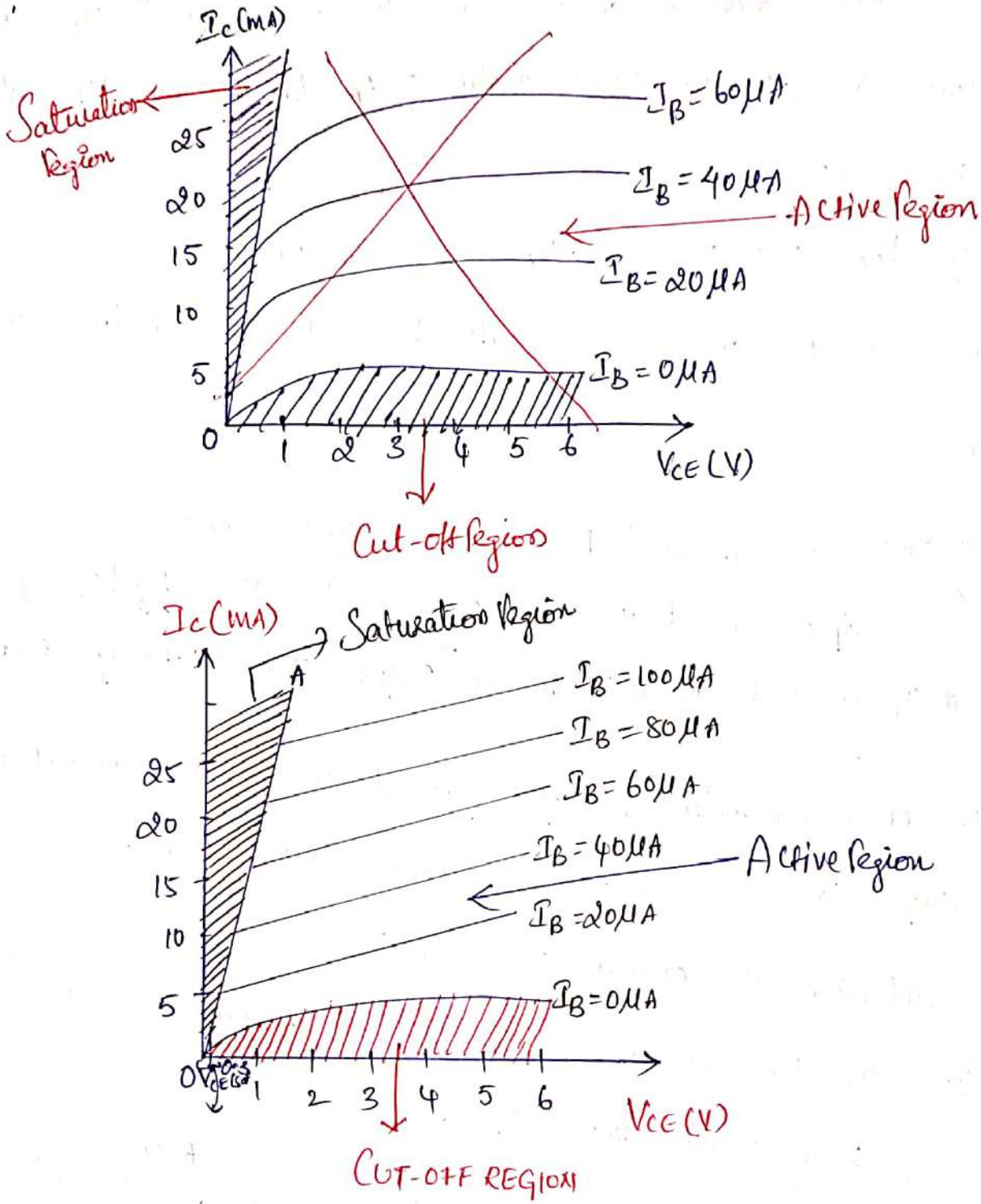

FIG: CE OUTPUT CHARACTERISTICS

* For larger values of V_{CE}, due to Early effect, a very small change in α is reflected in a very large change in β

* For Eg: When $\alpha = 0.98$ $\beta = \frac{0.98}{1-0.98} = 49$

$\alpha = 0.98$ $\beta = \frac{0.98}{1-0.98} = 49$

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* Here, a slight increase in α results in an more increase in β.
* Hence, the o/p characteristics of CE configuration shows a larger slope when compared with CB configuration.
* The output characteristics have three regions namely,

1. Active Region
2. Saturation Region
3. Cut-off Region.

1. ACTIVE REGION:

* In this region emitter-base junction is forward biased and collector-base junction is reverse biased.
* The central region in the o/p characteristics where the curves are uniform in spacing is called Active Region.
* As V_{CE} is increased, reverse bias increases at collector junction. This causes depletion region to spread more in base than in collector, reducing the chances of recombination in the base.
* This early effect causes Collector current to rise more sharply with increasing V_{CE} in the active region.

2. SATURATION REGION:

* In Saturation Region both the emitter-base junction and Collector-base junctions are forward biased.

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* If V_{CE} is reduced to a small value such as 0.2V, then Collector-base junction becomes forward biased, since the emitter-base junction is already forward biased.

* The input junction in CE configuration is base to emitter junction, which is always forward biased to operate transistor in active region.

* The reduced V_{CE} voltage is called as Saturation Voltage i.e., $V_{CE(sat)}$ whose value ranges from 0.1 to 0.3V

* In Saturation Region, the value of the collector current is independent of the base current and depends on the value of Saturation Resistance.

* Saturation Resistance: The ratio of Saturation Voltage $V_{CE(sat)}$ to the Collector Current I_C is called Saturation Resistance.

$$\text{Saturation resistence } R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$$

* The Region of OA line in the curve represents the Saturation Region.

3. CUT-OFF REGION:

* The Region in which the emitter-base junction and collector base junction are reverse biased is called Cut-off Region.

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* Also the i/p current I_B is, base current $I_B = 0$ in the cut off Region.

* We know that, $I_C = \beta I_B + (\beta+1) I_{CBO}$

When $I_B = 0$; $I_C = \beta(0) + (\beta+1) I_{CBO}$

$$I_C = (\beta+1) I_{CBO}$$

$\because (\beta+1) I_{CBO} = I_{CEO}$ $\quad (\because (\beta+1) I_{CBO} = I_{CEO})$

$$I_C = I_{CEO}$$

* In cut-off region the collector current is equal to reverse saturation current i.e., leakage current I_{CEO}.

* This is considerable amount of collector current flowing through the transistor.

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TRANSISTOR PARAMETERS:

a) INPUT IMPEDANCE (hie):

Definition: The ratio of change in input base to emitter voltage to the change in input base current with the o/p voltage constant i.e., V_{CE} is called Input Impedance.

$$h_{ie} = \left.\frac{\Delta V_{BE}}{\Delta I_B}\right|_{V_{CE} \text{ is constant}}$$

RANGE: The typical value of hie ranges from 500 to 2000Ω

b) OUTPUT ADMITTANCE:

Definition: The ratio of change in the output collector current to the corresponding change in the output collector to emitter voltage with the input base current I_B kept constant is called as output Admittance.

$$h_{oe} = \left.\frac{\Delta I_C}{\Delta V_{CE}}\right|_{I_B \text{ is constant}}$$

RANGE: The typical value of hoe ranges from 0.1 to 10 mhos.

c) FORWARD CURRENT GAIN:

Definition: The ratio of the change in the collector current to the corresponding change in the base current keeping the output collector to emitter voltage constant is called "forward current gain".

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$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}\Big|_{V_{CE}=\text{Constant}}$$

Range: The typical value of h_{fe} ranges from 20 to 200.

d) REVERSE VOLTAGE GAIN:

Definition: The ratio of change in input Base to Emitter Voltage to the corresponding change in output Collector to Emitter Voltage with constant input current I_B is defined as Reverse Voltage gain.

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}\Big|_{I_B \text{ Constant}}$$

Range: The typical value of h_{re} ranges from 10^{-5} to 10^{-4}

ADVANTAGES OF CE

1. A Common Emitter amplifier is inverting and has low i/p Impedance.
2. ~~High~~ moderate output Impedance.
3. High Voltage gain.
4. High Current gain.

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DISADVANTAGES

1. It has a high o/p resistance.
2. It responds poorly to high frequencies
3. It has high thermal instabilities
4. It's voltage gain is very unstable.

APPLICATIONS :

1. The Common emitter circuit is popular because it's well-suited for voltage amplification, especially at low frequencies.
2. Common emitter amplifiers are also used in Radio frequency transceiver circuits
3. It is commonly used in low-noise amplifiers.

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3. COMMON COLLECTOR CONFIGURATION:

Definition: The Configuration in which base acts as a Input terminal, emitter as a output terminal and collector is common to both input and output terminals then such configuration is called "Common collector configuration".

* Common collector configuration is also called as "Emitter follower" & "Grounded collector configuration".

CIRCUIT DIAGRAM:

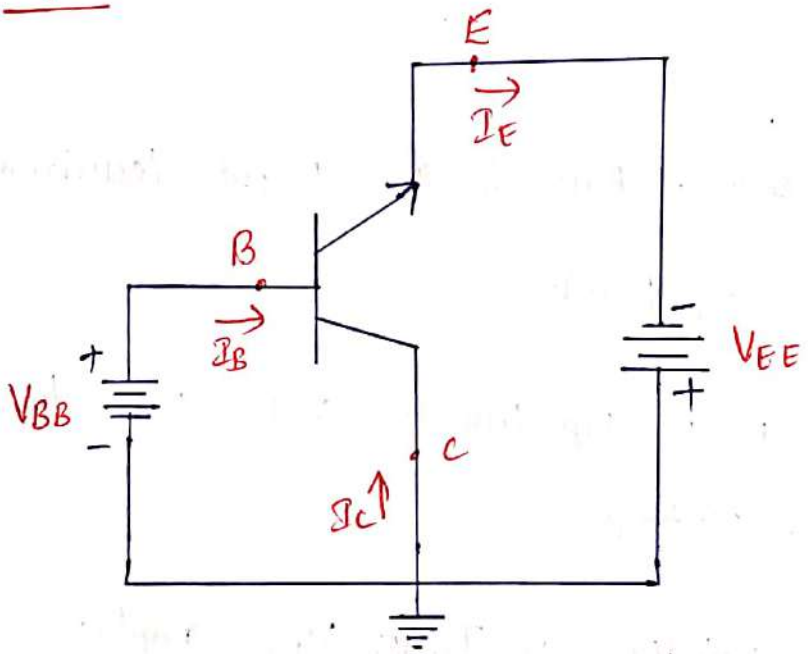

FIG: CE CONFIGURATION FOR NPN TRANSISTOR

* We know that $I_E = I_B + I_C \rightarrow (1)$

$$I_C = \alpha I_E + I_{CBO} \rightarrow (2)$$

Sub eq (2) in eq(1)

$$I_E = I_B + (\alpha I_E + I_{CBO})$$

$$I_E - \alpha I_E = I_B + I_{CBO}$$

$$I_E (1-\alpha) = I_B + I_{CBO}$$

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$$I_E = \frac{1}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

$$I_E = (\beta+1) I_B + (\beta+1) I_{CBO}$$

$$\boxed{I_E = \gamma I_B + \gamma I_{CBO}} \quad \because I_B >> I_{CBO} \Rightarrow I_E = \gamma I_B$$

$$\boxed{\gamma = \frac{I_E}{I_B}}$$

INPUT CHARACTERISTICS:

*Definition: The Graphical Representation which explains the relationship between Input current i.e, base current and Input Voltage i.e., Base to collector V_{BC} defines the I/p characteristics of CC Configuration.

* In cc Configuration, Base is the Input terminal and Emitter is the o/p terminal

* So base current is I/p current and Base to collector voltage is o/p voltage.

* So I/p characteristics is I_B Vs V_{BC} graph.

* The circuit to determine the Static characteristics of cc is as shown below.

Current Amplification factor: The ratio of change in o/p current I_E to the change in i/p current I_B is called current amplification factor.

$$\boxed{\gamma = \frac{\Delta I_E}{\Delta I_B}}$$

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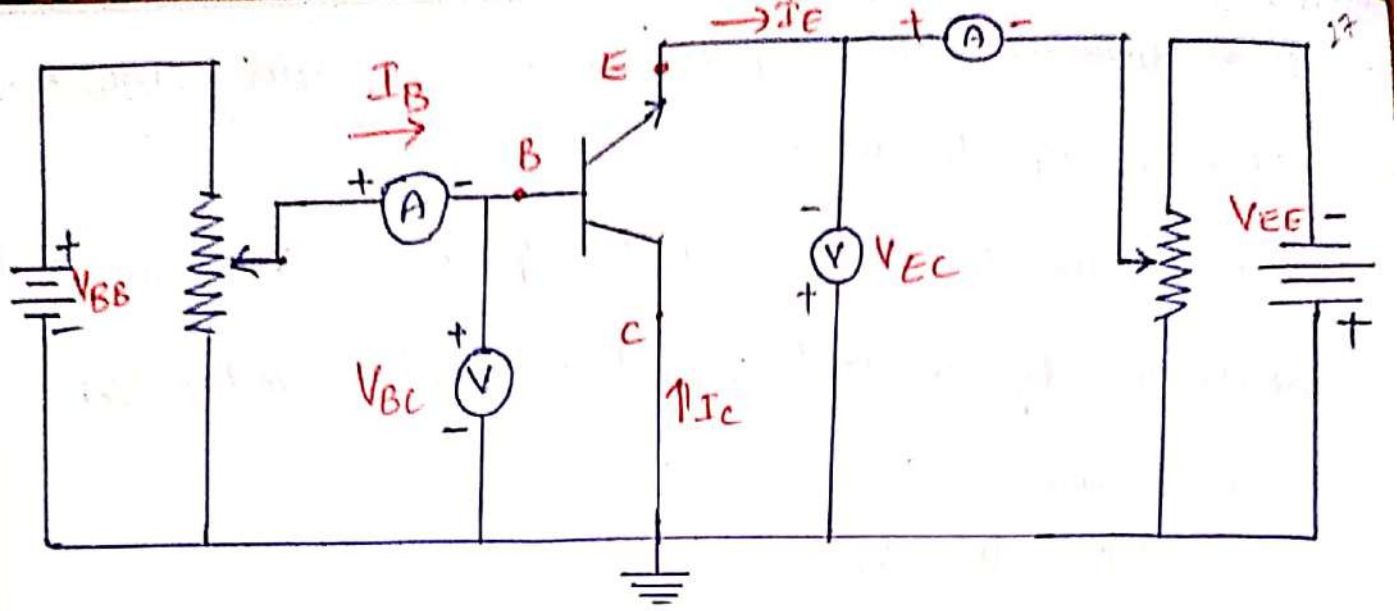

FIG: CIRCUIT TO DETERMINE CC STATIC CHARACTERISTICS

* To determine the Input characteristics,

1. Keep Emitter to collector Voltage V_{EC} i.e., o/p Voltage.
2. Increase the Base to collector Voltage V_{BC} in equal steps and note the corresponding I_B values.
3. This is Repeated for different fixed values of V_{EC}.

⇒ Plots for different values of I_B Vs V_{EC} is as shown below.

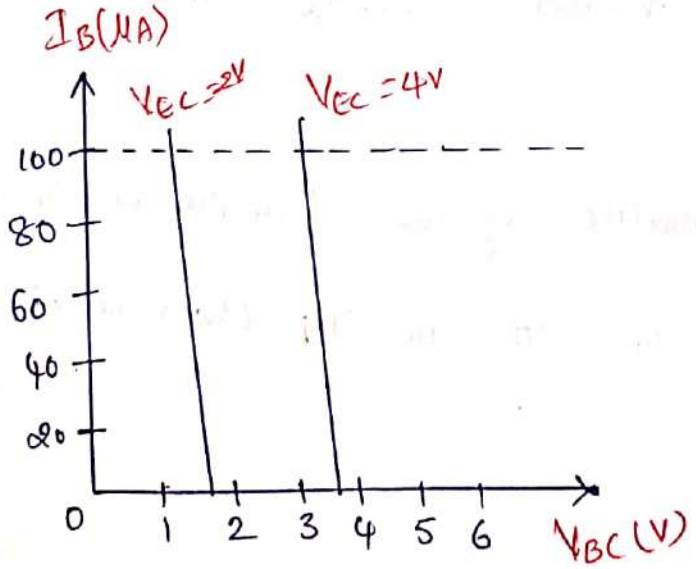

FIG: INPUT CHARACTERISTICS OF CC CONFIGURATION

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* The Common Collector i/p Characteristics are quite different from CB & CE i/p Characteristics.

* This is due to the fact that i/p Voltage V_{CC} is largely determined by the level of Collector to Emitter Voltage V_{CE}.

From the circuit

→ $V_{CE} = V_{CB} + V_{BE}$

Case1 when $V_{EC} = 0V$

* If Collector to base Voltage V_{CB} is increased then the depletion width increases this will reduce the effective width of the base.

* So, the probability of recombination in base region also reduces. due to this base current I_B reduces.

Case2 when $V_{EC} = 4V$

* When forward biased voltage at emitter junction increases this causes more number of charge carriers will reach the base terminal

* So, for higher values of V_{CC} base current increases thats why Curve shifts to right in I/p Characteristics.

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OUTPUT CHARACTERISTICS:

* We know that $I_C = \alpha I_E + I_{CBO}$

$$I_E >> I_{CBO}$$

$$\boxed{I_C = \alpha I_E}$$

* α ranges from 0.95 to 0.98 which is approximately equal to unity

$$\boxed{I_C \simeq I_E}$$

* Because of this o/p ~~Eo~~ Emitter Current is almost equal to Collector Current.

* Plot is ~~equ~~ similar to the o/p curves of CE configuration

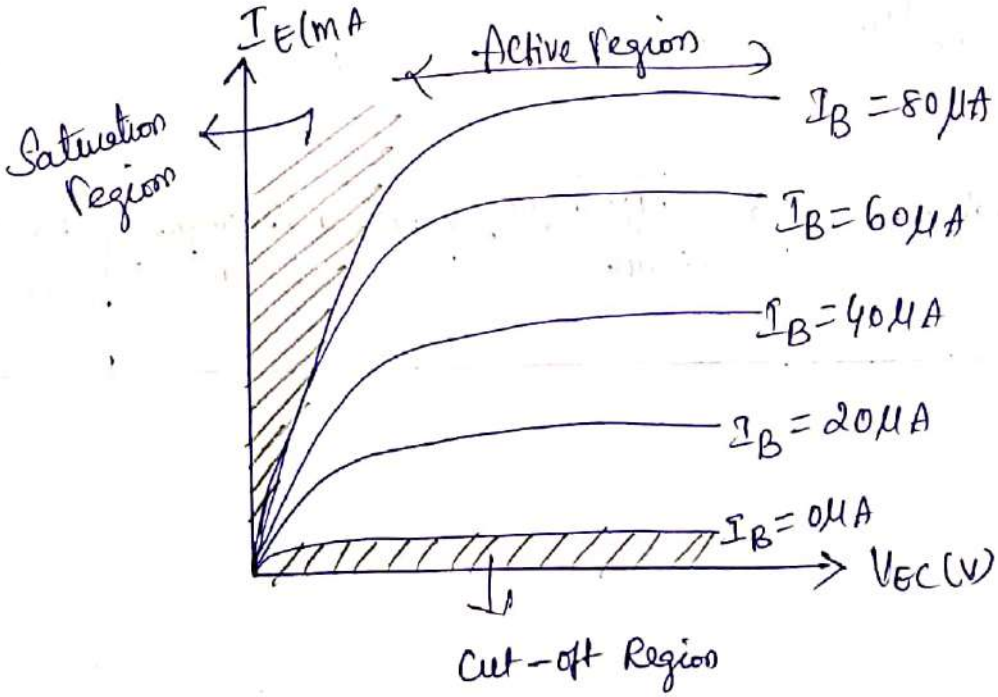

FIG: OUTPUT CHARACTERISTICS OF CC CONFIGURATION

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ADVANTAGES

1. It has high Current gain
2. It has lowest O/p impedance
3. The Voltage gain of a CC is at best slightly lessen than one.

COMPARISON OF CB, CE and CC Configurations:

PROPERTY	CB	CE	CC
1. Input Resistance	low (about 100Ω)	Moderate (about 750Ω)	High (about 750kΩ)
2. Output Resistance	High (about 450kΩ)	Moderate (about 45kΩ)	Low (about 25Ω)
3. Current gain	1	High	High
4. Voltage gain	About 150	About 500	Less than one
5. phase shift between i/p & o/p Voltages	0 & 360°	180°	0 & 360°
6: Application	For high frequency circuits	For Audio frequency circuits	For Impedance matching

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Relation between α, β & γ:

* In CC configuration current amplification factor is given by

$$\gamma = \frac{I_E}{I_B} \rightarrow (1)$$

W.K.T $I_E = I_B + I_C$

$$I_B = I_E - I_C \rightarrow (2)$$

Sub eq 2 in eq (1)

$$\gamma = \frac{I_E}{I_E - I_C} \rightarrow (3)$$

divide eq 3 Numerator & denominator with I_E

$$\gamma = \frac{I_E / I_E}{\frac{I_E}{I_E} - \frac{I_C}{I_E}}$$

$$\boxed{\gamma = \frac{1}{1-\alpha}} \quad \left(\because \alpha = \frac{I_C}{I_E}\right)$$

Similarly $\gamma = \frac{I_E}{I_B}$

$$\gamma = \frac{I_B + I_C}{I_B}$$

divide numerator & denominator with I_B

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$$\gamma = \frac{\frac{I_B}{I_B} + \frac{I_C}{I_B}}{\frac{I_B}{I_B}}$$

$$\boxed{\gamma = 1 + \beta} \quad \left(\because \beta = \frac{I_C}{I_B}\right)$$

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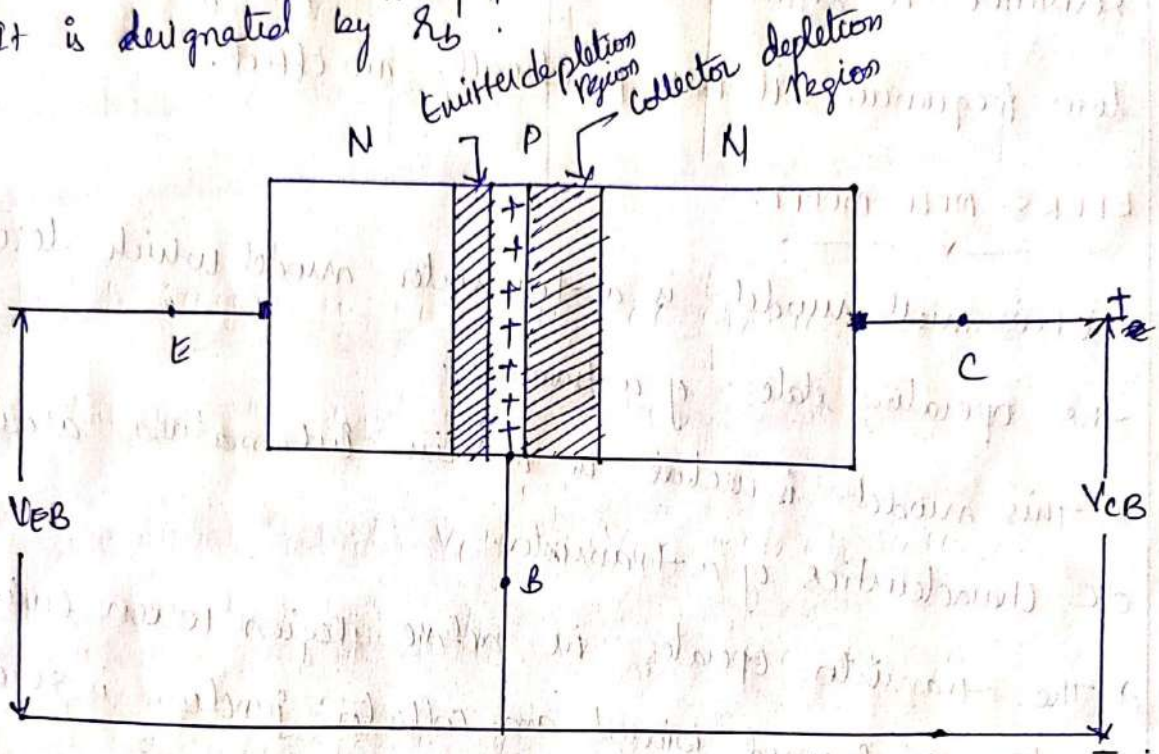
BASE SPREADING RESISTANCE:

Definition: The Resistance offered by the narrow path region of base terminal is called "Base spreading Resistance".

* It is designated by "$r_{bb'}$".



* We know that width of the base region of a transistor is extremely small. Therefore, the current which enters the base region, across the emitter-base junction, has a narrow path to reach the base terminal.
* The value of base spreading resistance can be increased by increasing the reverse-bias voltage (V_{CB}) across the collector-base junction.
* The width of collector-base depletion layer increases and it penetrates more into the base region than that of collector. Because of this cross-sectional area of base reduces.
* The small cross-sectional area means a large base-spreading resistance. It is about 50 to 150 Ω, in some cases it may be 1000 Ω

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* When a current passes through the base spreading resistance, it produces a voltage drop across it.

* It has been observed that the effect of Base spreading resistance is significant in high frequency circuits. At low frequencies, it has practically no effect.

EBERS-MOLL MODEL:

* Ebers-moll model is a transistor model which describes the operating states of a transistor.

* This model is useful to obtain information about the dc characteristics of a transistor.

* The transistor operates in active region when emitter junction is forward biased and collector junction is reverse biased.

* This model generalises the behaviour of a transistor by taking into account the inverted mode of operation of transistor.

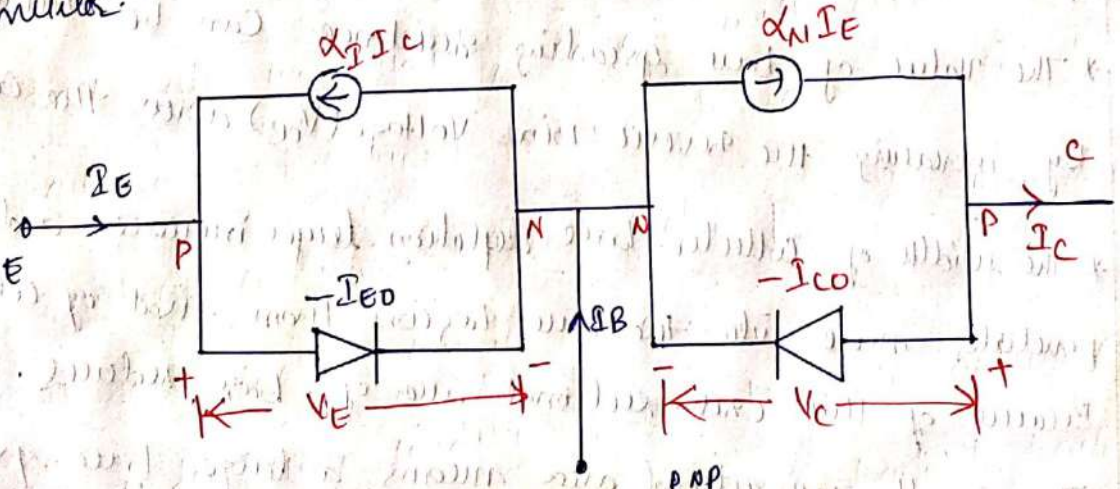

FIG: EBERS MOLL MODEL OF A TRANSISTOR

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By applying KCL at collector node

Collector current $I_C = -\alpha_N I_E + I$

$$I_C = -\alpha_N I_E + I_0(e^{V_C/V_T} - 1)$$

⇒ where I is the diode current. as I_0 is the magnitude of reverse saturation current then $I = -I_{CO}$, then

$$I_C = -\alpha_N I_E - I_{CO}(e^{V_C/V_T} - 1)$$

* The base spreading resistance has been omitted and the difference b/n I_{CBO} & I_{CO} have also been neglected.

* From the fig, it is evident that dependent current sources can be eliminated from the fig provided $\alpha_N = \alpha_I = 0$.

* In such a condition,

* For example, by making the width of the base much larger than the diffusion length of the minority carriers in the base, all the minority carriers will recombine in the base and none will survive to reach the collector.

* In such as condition transport factor β and then also current gain factor α will be zero.

* Thus under these conditions, the transistor action ceases and we simply have two diodes placed back to back

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* The dependency of the currents in a transistor is upon the junction voltages & vice-versa may be obtained by starting with the equation here;

$$I_C = -\alpha_N I_E - I_{CO}(e^{V_C/V_T} - 1) \rightarrow (1) \quad (\because I_C = \alpha I_E + I_{CO})$$

* Here N in α_N indicates the normal mode of operation of the transistor and minus (-) sign indicates its direction

* For Inverted mode of operation, equation will be,

$$I_E = -\alpha_I I_C - I_{EO}(e^{V_E/V_T} - 1) \rightarrow (2)$$

* Here α_I is the Inverted common base current gain, just like α_N in normal operation.

I_{EO} → Reverse saturation current flowing at emitter junction

V_E → Voltage drop at the emitter junction

* Ebers moll model involves two ideal diodes connected back to back with reverse saturation currents I_{EO} and I_{CO}.

* Two dependent Current Controlled current sources shunting the ideal diodes. The current sources account for the minority carrier transport across the base.

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* From above discussion, it is clear that a transistor cannot be constructed by simply connecting two seperate diodes back to back.

TRANSISTOR AS AN AMPLIFIER:

AMPLIFIER: An Amplifier is an electronic device or circuit which is used to increase the magnitude of the signal applied to its input.

* For a transistor to act as an amplifier, it should be properly biased.

* A transistor acts as an amplifier by raising the strength of a weak signal.

* the DC bias voltage applied to the emitter base junction, makes it remain in forward biased condition.

* This forward biased is maintained regardless of the polarity of the signal.

* The below figure shows how a transistor looks like when connected as an amplifier.

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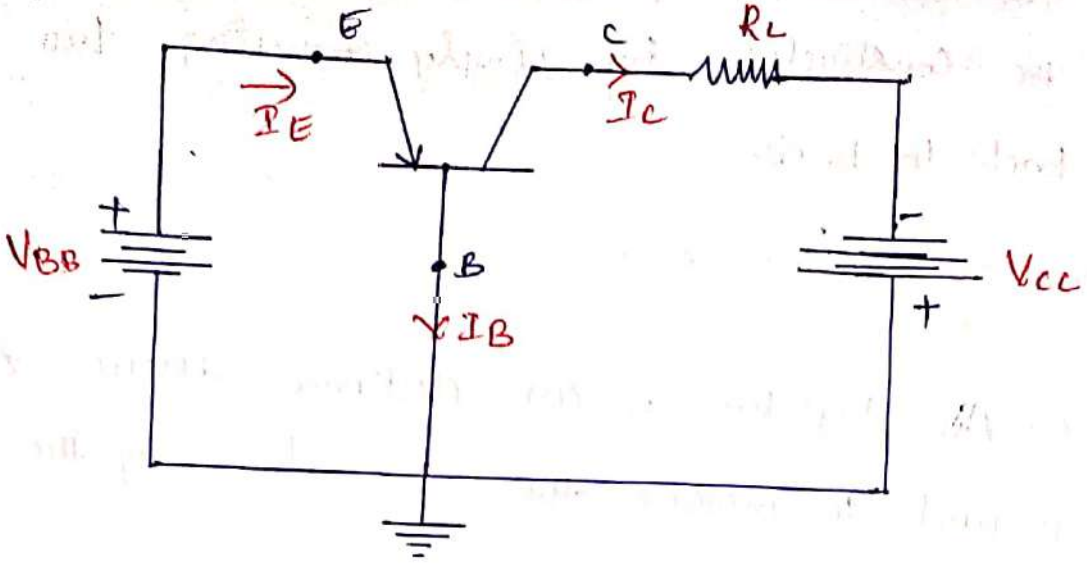

FIG: TRANSISTOR AS AN AMPLIFIER

* To explain the amplification process consider a p-n-p transistor connected to a load Resistor (R_L).

* The load resistor 'R_L' is connected in series with the collector power supply (V_{CC}).

* When emitter to base junction is in forward bias V_{BE} and collector to base junction (V_{CB}) is in reverse bias the transistor is operated in active region and acts as a Amplifier.

* The emitter current caused by the input signal contributes the collector current, which when flows through the load Resistor R_L, results in a large voltage drop across it.

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* A small change in the I/p voltage between emitter and base (ΔV_i) causes a large change in emitter current (ΔI_E).

* A fraction of this change in current is collected and it is passed through R_L and it is denoted as α'.

* The change in voltage across load resistor R_L due to this current is

$$\boxed{\Delta V_o = \alpha' R_L \Delta I_E} \rightarrow (1)$$

* The voltage amplification factor $\boxed{A_V = \frac{\Delta V_o}{\Delta V_i}} \rightarrow (2)$

* If $\frac{\Delta V_o}{\Delta V_i} > 1$, then voltage amplification takes place.

* The change in i/p voltage (ΔV_i) across the dynamic resistence r_e' at emitter voltage is,

$$\boxed{\Delta V_i = r_e' \Delta I_E} \rightarrow (3)$$

Substituting eq (1) & (3) in eq (2) we get,

$$A_V = \frac{\Delta V_o}{\Delta V_i} = \frac{\alpha' R_L \Delta I_E}{r_e' \Delta I_E} = \frac{\alpha' R_L}{r_e'} > 1$$

* From the above equation A_V is greater than unity so transistor acts as amplifier.

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LIMITS OF OPERATION (BREAKDOWN IN TRANSISTORS):-

* There is a possibility of voltage breakdown in the transistor at high voltages even though the rated dissipation of the transistor is not exceeded.
* Therefore, there is an upper limit to the maximum allowable collector junction voltage.
* There are two types of breakdown, namely
  1. Avalanche multiplication (or) Avlanche Breakdown
  2. Reach through (or) Punch through.

1. AVALANCHE MULTIPLICATION (OR) BREAKDOWN:

* When the diode is reverse biased, there is a limit on the voltage that can be applied which is the avalanche voltage.
* Similarly, in the transistor, the maximum reverse biasing voltage which may be applied before breakdown voltage between the collector and base terminals with the emitter open is called breakdown voltage BV_{CBO}.
* Therefore, an upper limit is set on the collector voltage V_{CB} by avalanche breakdown in the reverse biased collector-base junction.

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* Breakdown may occur because of Avalanche multiplication of the current I_{CO} that cross the collector junction.

* As a result of this multiplication of the current I_{CO} that crosses the collector junction

* As a result of this multiplication, the current becomes MI_{CO}.

Where M is the multiplication factor.

* At the breakdown voltage BV_{CBO}, multiplication factor M becomes infinite and the current rises abruptly in the breakdown region. There will be large changes in current with small changes in applied voltage.

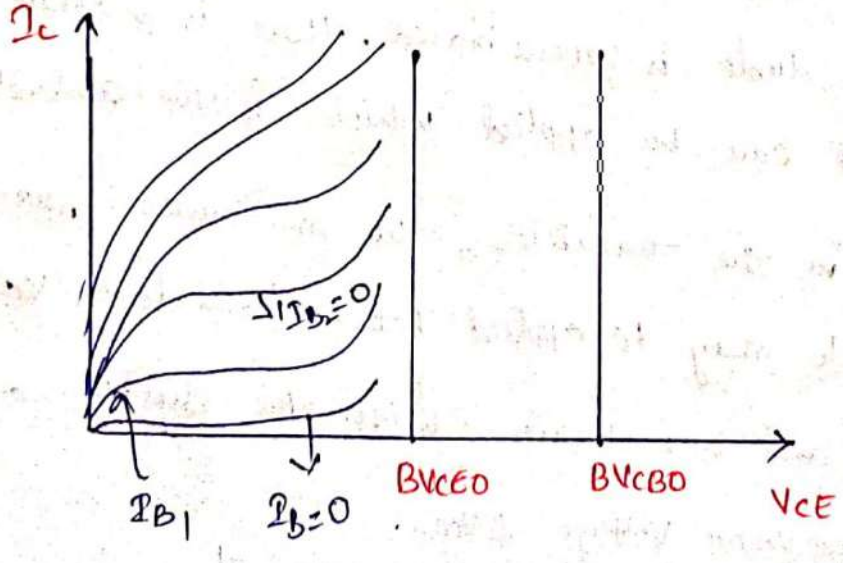

FIG: CE CHARACTERISTICS IN THE BREAKDOWN REGION

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* The Avalanche multiplication factor depends on the voltage V_{CB} between collector and base; which has been found to be given empirically by,

$$M = \frac{1}{1 - \left[\frac{V_{CB}}{BV_{CBO}}\right]^n} \rightarrow (1)$$

* Where the empirical constant n depends on the lattice material and the carrier type, which is usually in the range of about 2 to 10.

For N-type $n = 4$

P-type $n = 2$

* For the CE configuration, the collector to emitter breakdown voltage with base open is,

$$BV_{CEO} = BV_{CBO} \sqrt[n]{\frac{1}{h_{FE}}}$$

* In general, BV_{CEO} is 40 to 50% of BV_{CBO}. This is the upper limit of V_{CE} that can be placed across the transistor without damaging it.

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2. REACH THROUGH (OR) PUNCH THROUGH:

* According to Early effect, the width of the collector-junction transition region increases with increased collector-junction voltage.
* As the voltage applied across the junction V_{CB} increases the transition region penetrates deeper into the base and will have spread completely across the base to reach the emitter junction, as the base is very thin.
* Thus, the collector voltage has reached through the base region.
* this effect, known as reach-through, also effects the o/p characteristics of a transistor.
* It is possible to raise the punch-through voltage by increasing the doping concentration in the base, but this automatically reduces the Emitter efficiency.
* Punch through takes place at a fixed voltage between Collector and base and is not dependent on circuit configuration.
* whereas Avalanche multiplication takes place at different voltages depending upon the circuit configuration.

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PHOTO TRANSISTOR:

Definition: The phototransistor is a three-layer semiconductor device which has a light-sensitive base region. The base senses the light and converts it into the current which flows between the collector and the emitter region.

* The main difference between BJT and phototransistor is that there is no electrical connection for base terminal.

* The main advantage of phototransistor is that it produces more output than photodiode even though same input is applied.

SYMBOL:

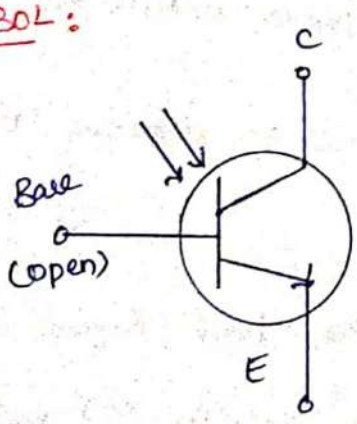

FIG: SYMBOL FOR PHOTOTRANSISTOR

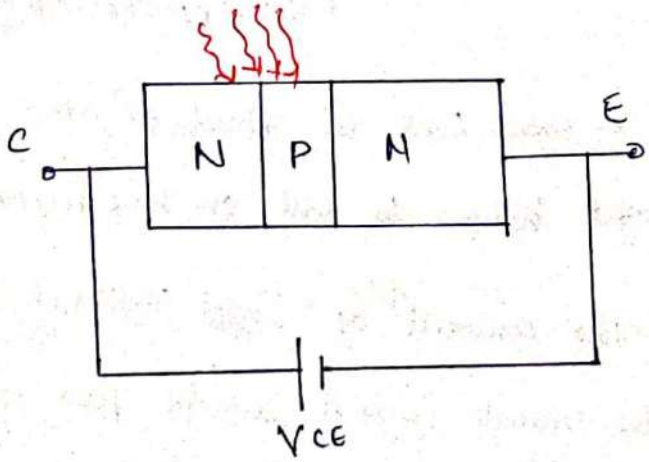

FIG: PHOTOTRANSISTOR CONNECTION

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CONSTRUCTION:

* Similar to BJT, photo-transistor is a three terminal device in which base region is enlarged.

* In photo-transistor a small window is provided near Collector-base junction

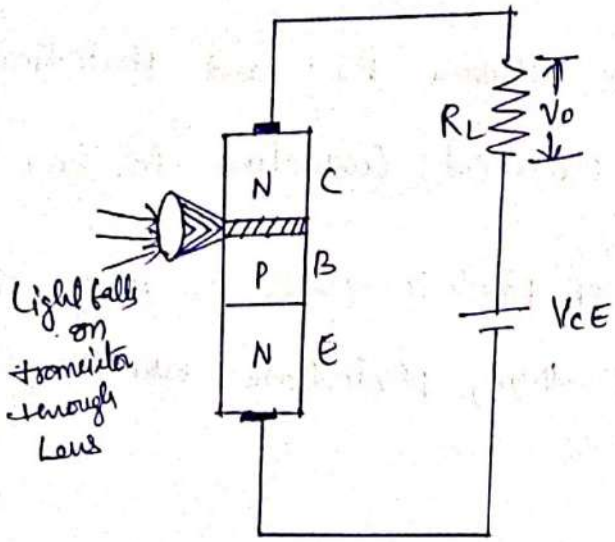

FIG: CONSTRUCTION OF PHOTO TRANSISTOR

* A small Lens is fixed on the window for allowing a focused light beam to fall on base region.

* The amount of light incident on the base region determines how much current should pass through collector (C) and out from Emitter (E).

* The collector base junction is sensitive to light falling on it. Therefore brighter light results more current and less bright results less current.

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* When there is no incident light on the phototransistor, the collector current is due to the thermally generated carriers and is given by

$$I_c = (\beta+1) I_{CO}$$

* Where I_{CO} is the Reverse Saturation current.

* In phototransistor this current is referred to as the current.

* Dark current is the current which is due to Reverse Saturation current when there is no incident of light.

* When light is incident on the photo transistor, photo-current is generated and the magnitude of the collector current increases.

* the expression for collector current is given by,

$$\boxed{I_c = (\beta+1)(I_{CO} + I_\lambda)}$$

* Where I_λ is the photo current which is due to incident light photons.

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* The V-I Characteristics of phototransistor is given by,

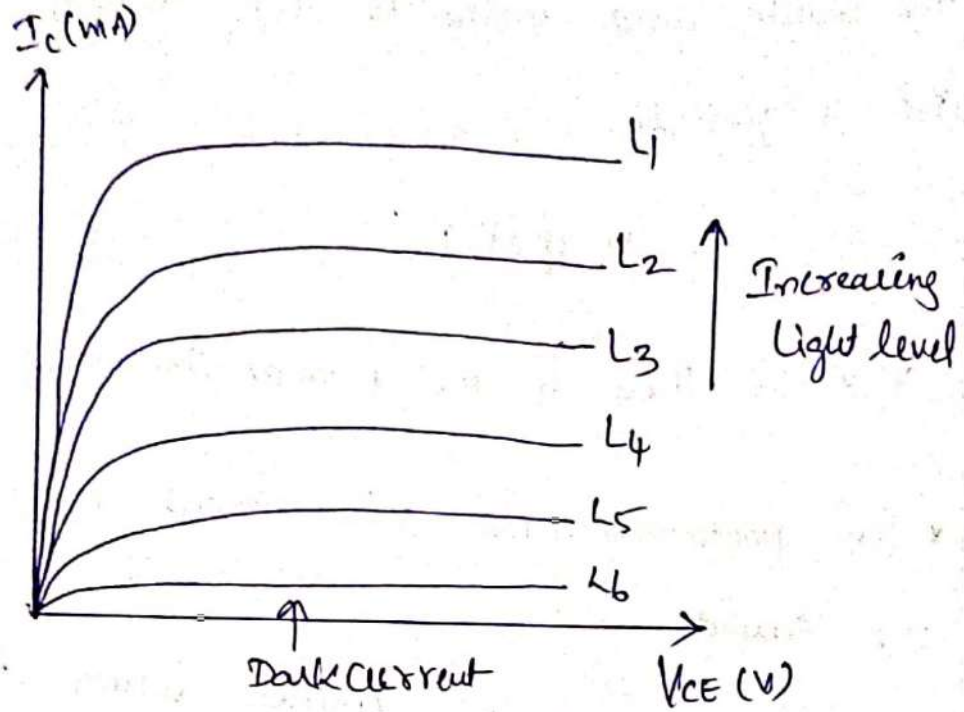

FIG: V-I CHARACTERISTICS OF PHOTO TRANSISTOR.

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TYPICAL TRANSISTOR JUNCTION VOLTAGE VALUES:

* In different conditions such as active, saturation and cut-off there are different junction voltages.

* The junction voltages for a typical n-p-n transistor at 25°C are given by,

TYPE	$V_{CE\,sat}$	$V_{BE\,sat}$	$V_{BE\,active}$	$V_{BE\,cut\text{-}in}$	$V_{BE\,cut\text{-}off}$
Si	0.3	0.7	0.6	0.5	0.0
Ge	0.1	0.3	0.2	0.1	−0.1

* For p-n-p transistors the signs of all values should be reversed.

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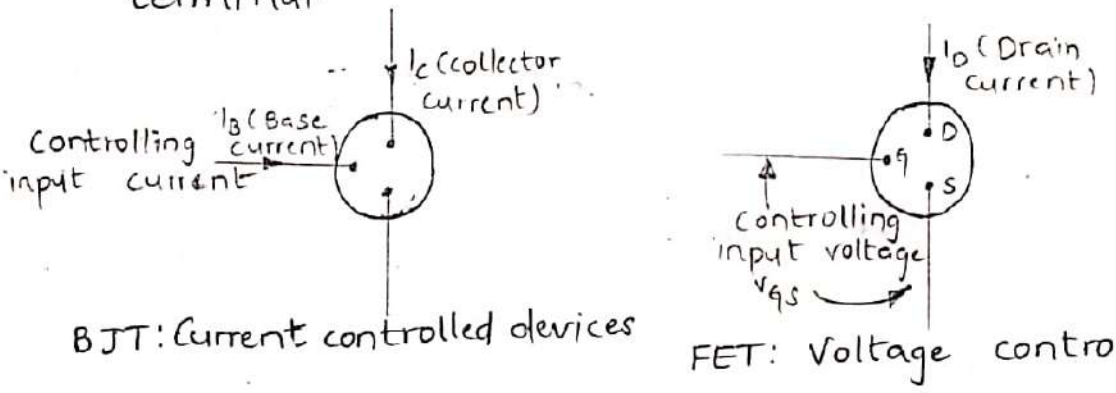
2. FIELD EFFECT TRANSISTORS AND ITS BIASING

Background:

The field effect transistor abbreviated as FET is an another semiconductor device like a BJT which can be used as an amplifier or switch. Like BJT, FET is also a three terminal device; however, the principle of operation of JET is completely different from that of BJT.

The three terminals of FET are named as Drain(D), Source(S) and gate(G), as shown in the Fig 6.1. Out of these terminals gate terminal acts as a controlling terminal. Controlled output current Controlled output current



BJT: Current controlled devices FET: Voltage controlled device

Fig 6.1 Controlling element for BJT and FET

FET: Voltage Controlled Device:

As shown in fig 6.1 in BJT the output current, I_C is controlled by the base current I_B. Hence BJT is a current controlled device. On the other hand, in FET, the voltage applied between gate and source (V_{GS}) controls the drain current I_D. Therefore, FET is a voltage controlled device. The name "Field effect" is derived from the fact that the output current.

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current flow is controlled by an electric field set up in the device by an externally applied voltage between gate and source terminals.

FET: Unipolar Device

We know that in BJT, the current is carried by both electrons and holes, and hence the name "bipolar" junction transistor. However in FET, current is carried by only one type of charge particles, either electrons or holes. Hence FET is called "unipolar device".

FET : Other Important Features

* Like BJT, the parameters of FET are also temperature dependent. In FET, as temperature increases drain resistance also increases, reducing the drain current. Thus unlike BJT, thermal runaway does not occur with FET. Thus we can say that FET is "more temperature stable" as compared to the BJT.
* FET has very high input impedance. Typically it is in the range of one to several megaohms. Because FETs have higher input impedance than BJT they are preferred in amplifiers where high input impedance is required.
* FETs require less space than that for BJTs, hence they are preferred in integrated circuits.
* FET is less noisy than a bipolar transistor.
* FET exhibits no offset voltage at zero drain current, and hence makes an excellent signal chopper.

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* Gain-bandwidth product of FET is relatively small as compared to conventional transistor. This is the disadvantage of the FET.

FET: Different Types and Application Areas

The FETs are categorized as:

* Junction Field Effect Transistors (JFETs)
* Metal Semiconductor Field Effect transistors (MESFETs)
* Metal oxide Semiconductor Field Effect transistors (MOSFETs)

The JFETs and MESFETs are further classified into two types as, n-channel JFET/MESFET and p-channel JFET/MESFET and MOSFETs are further classified into two types as, depletion MOSFET and enhancement MOSFET. The Fig 6.2 shows the different types of FETs.

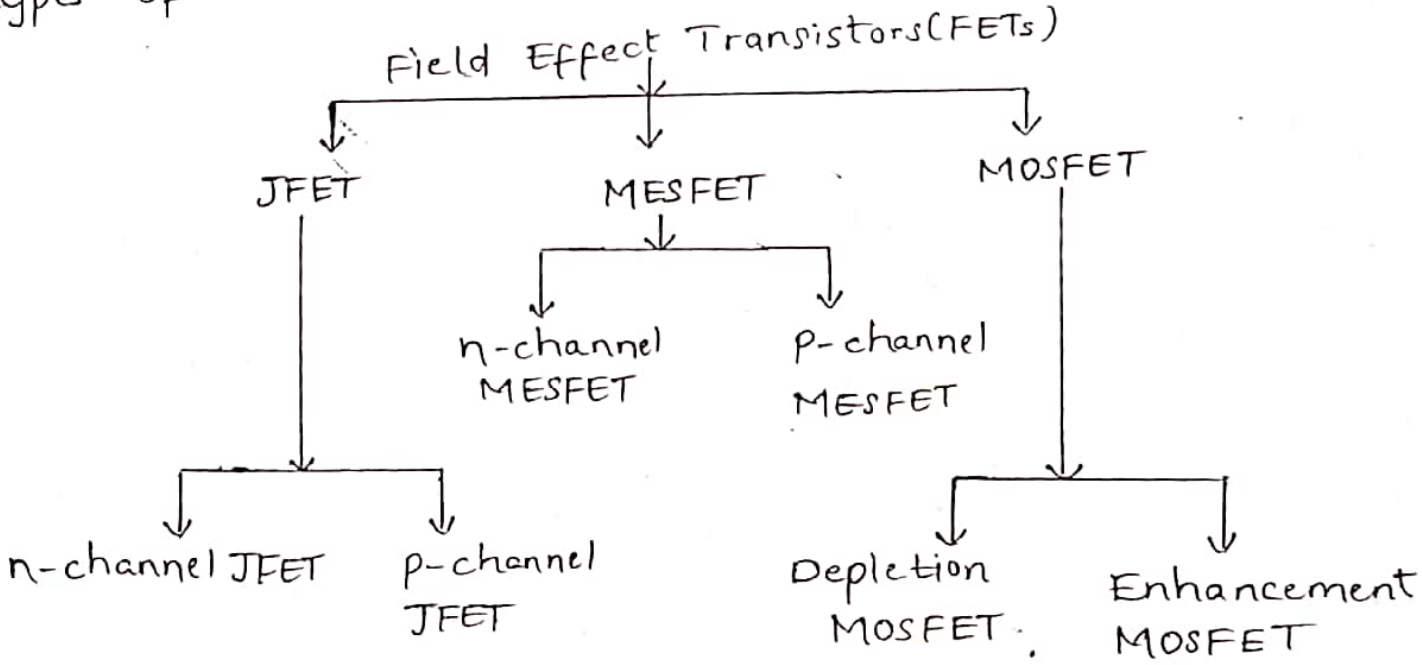

Fig 6.2 Different types of FETs

In the Junction FET, the gate junction may be a p-n junction, which forms a p-n JFET or simply JFET

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or a Schottky barrier junction, which forms a metal-semiconductor FET, or MESFET.

In general like BJTs the FETs can be used in switch, digital and linear amplifier applications. Because of Shottky barrier junction MESFETs have smaller transit time and faster response. Hence they are used in very high speed or high frequency applications, such as microwave amplifiers.

In JFET, there is a direct electrical connection between the gate terminal and the channel of a JFET. On the other hand, in MOSFETs, the gate is insulated from the channel by a very thin layer of dielectric material, silicon dioxide (SiO_2). Thus in MOSFETs, there is no direct electrical connection between the gate terminal and the channel. Due to this extra layer the input resistance of MOSFET is very very high.

The MOSFETs can be used in place of resistors in a circuit, so that circuits containing only MOSFETs can be designed. The MOSFET, compared to BJTs, can be made very small. Since digital circuits can be designed using only MOSFETs, with essentially no resistors or diodes required, high density VLSI circuits including microprocessors and memories, can be fabricated using MOSFETs. The MOSFET has made possible the hand-held calculator and the powerful personal computer. MOSFETs can also be used in analog circuits.

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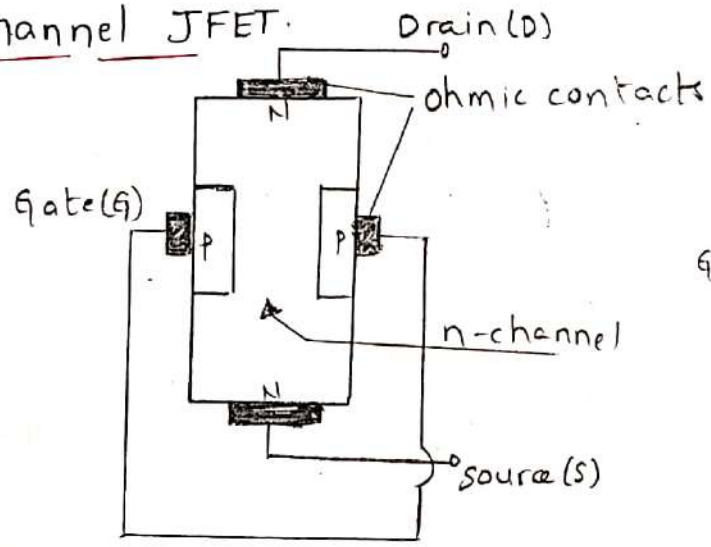
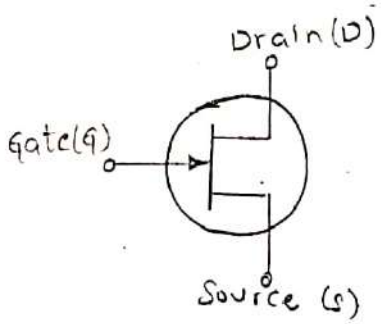
Junction Field Effect Transistor

Construction of n-channel JFET and Symbol:

The fig 6.3 shows structure and symbol of n-channel JFET. A small bar of extrinsic semiconductor material, n-type is taken and its two ends, two ohmic contacts are made which are the drain and source terminals of FET. Heavily doped electrodes of p type material form p-n junctions on each side of the bar. The thin region between the two p gates is called the channel. Since this channel is in the n type bar, the FET is known as n-channel JFET.





Symbol for n-channel JFET

Structure and symbol for n-channel JFET

The electrons enter the channel through the terminal called source and leave through the terminal called drain. The terminals taken out from heavily doped electrodes of p-type material are called gates. Usually those electrodes are connected together and only one terminal is taken out, which is called gate, as shown in fig.

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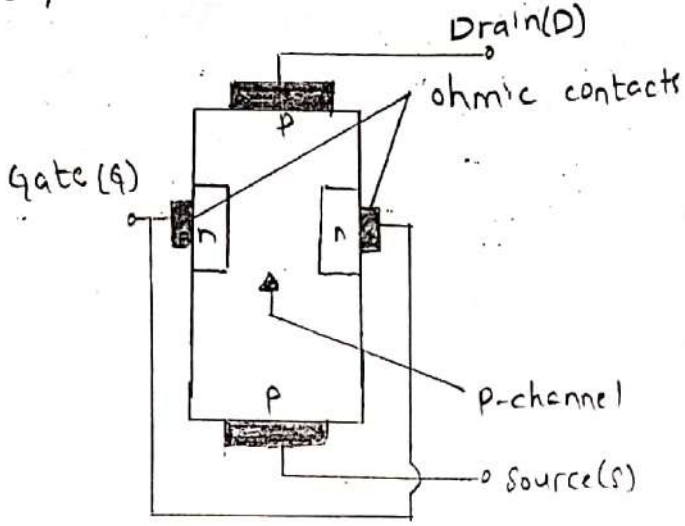
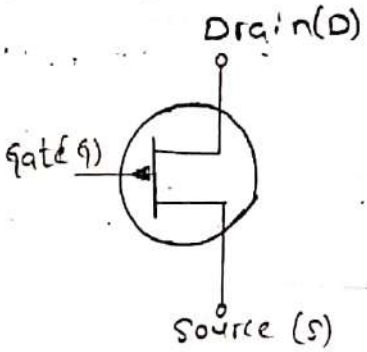
Construction of p-channel JFET and Symbol:

The device could be made of p type bar with two n type gates as shown in the fig. Then this will be p-channel JFET. The principle of working of n-channel JFET and p-channel JFET is similar; the only difference being that in n-channel JFET the current is carried by electrons while in p-channel JFET, it is carried by holes.





symbol for p-channel JFET

Structure and symbol for p-channel JFET

Unbiased JFET:

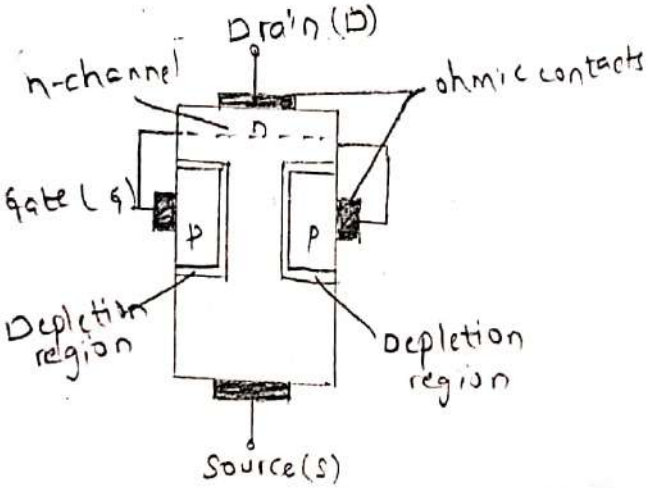


Fig 6.5 Junction Field effect Transistor

In the absence of any applied voltage, JFET has gate channel junctions under no bias conditions. The result is a depletion region at each junction, as shown in Fig. 6.5. This represents same depletion region of a diode under no bias conditions. Recall also that depletion region which does not have any free carriers and therefore is unable to support conduction through the region.

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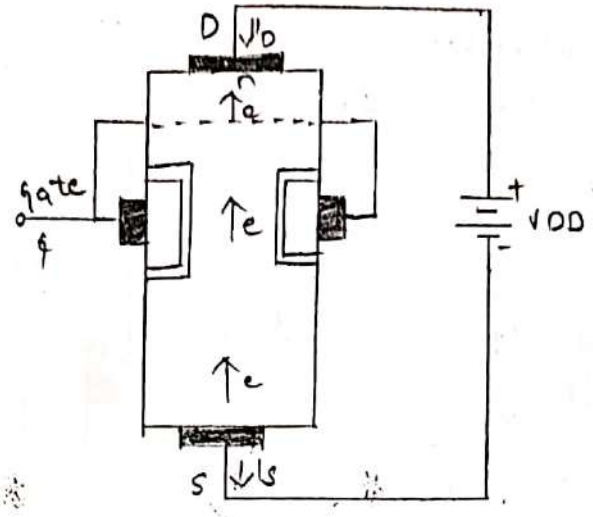
Operation of JFET:



n-channel JFET with gate open and V_{DD} is applied between drain and source.

In JFET, the p-n junction between gate and source is always kept in reverse biased conditions. Since the current in a reverse biased p-n junction is extremely small, practically zero; the gate current in JFET is often neglected and assumed to be zero.

Let us consider the circuit shown in fig 6.6 as shown in fig 6.6 voltage V_{DD} is applied between drain and source. Gate terminal is kept often open. The bar is of n-type material. Due to the polarities of applied voltage as shown in Fig 6.6, the majority carriers ie; the electrons start flowing from the source to the drain. This flow of electrons makes the drain current, I_D.

The majority carriers move from source to drain through the space between the gate regions. This space is commonly known as channel. The width of this channel can be controlled by varying the gate

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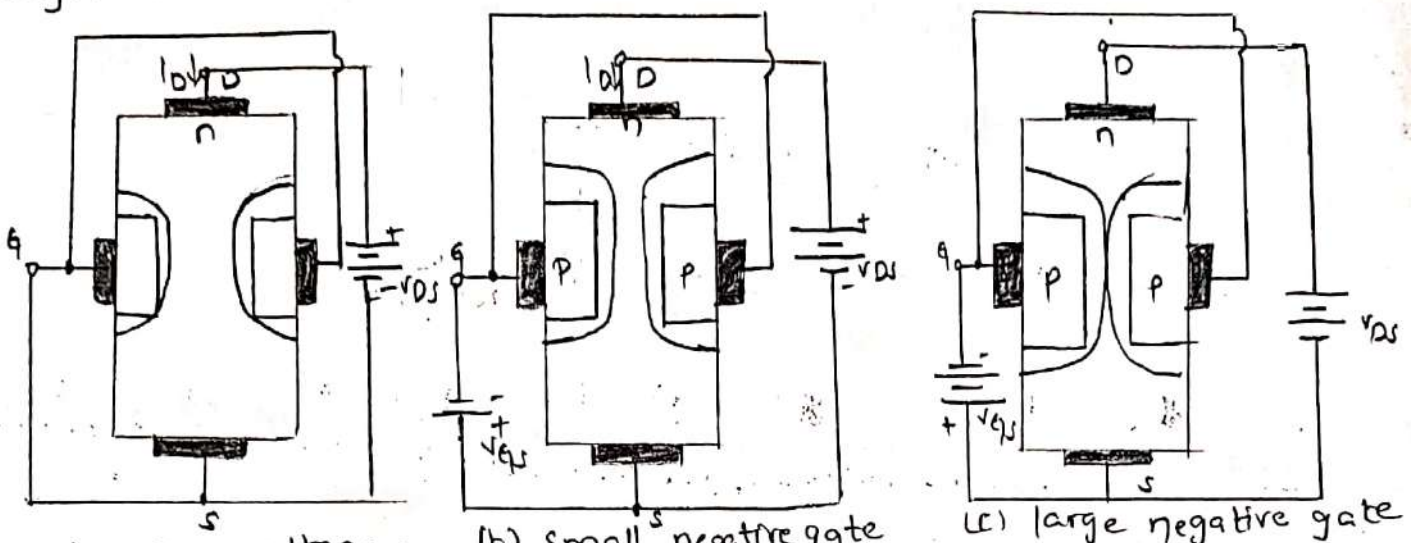
voltage. To see the effect of gate voltage on channel width and on drain current I_D, consider the diagrams shown in Fig. 6.7.



(a) No bias voltage on gates (b) Small negative gate source bias (c) large negative gate source bias

Fig. 6.7(a) shows that an n-channel JFET with the gate directly connected to the source terminal. When drain voltage V_{DS} is applied, a drain current I_D flows in the direction shown. Since the n-material is resistive the drain causes a voltage drop along the channel. This voltage drop reverse biases the p-n junctions and causes the depletion regions to penetrate into the channel. Since gate is heavily doped and the channel is lightly doped, the width of the depletion region will mainly be spread in the channel shown in fig. The penetration depends on reverse bias voltage. Looking at the fig, we can observe that depletion region, width is more at the drain side as compared to source side because near the junction, voltage at drain side is more than the voltage at the source side. This shows that the reverse bias is not uniform near the junction; it gradually increases from source side to drain side.

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JFET as Voltage Controlled Current Source

As we know, depletion region does not contain charge carriers, the space between two depletion regions is available for the conducting portion of the channel. If we externally apply reverse voltage to the gate, the reverse bias will further increase and hence increase the penetration of the depletion region, which reduces the width of the conducting portion of the channel. As width of the conducting portion of the channel reduces, the number of electrons flowing from source to drain reduces and hence the current flowing from drain to source reduces. If we go in increasing the reverse bias voltage to the gate as shown in Fig 6.7(b) and 6.7(c) depletion regions will increase more and more and stage will come when the depletion regions will be equal to original width of the channel, leaving zero width for conducting portion of the channel, as shown in fig 6.7(c). This will prevent any current flow from drain to source and this will cut-off the drain current. The gate to source voltage that produces cut-off is known as cut-off voltage and it is denoted by $V_{GS(off)}$.

When the gate is shorted to source, there is minimum reverse bias between gate and source p-n junction, making depletion region width minimum and constructing channel width maximum. In this case maximum drain current flows which is designated by I_{DSS} and this is the maximum possible drain

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current in JFET. From above dissusion it is cleared that the gate to source voltage controls the current flowing through channel and hence FET is also called "Voltage Controlled Current Source."

Key point:

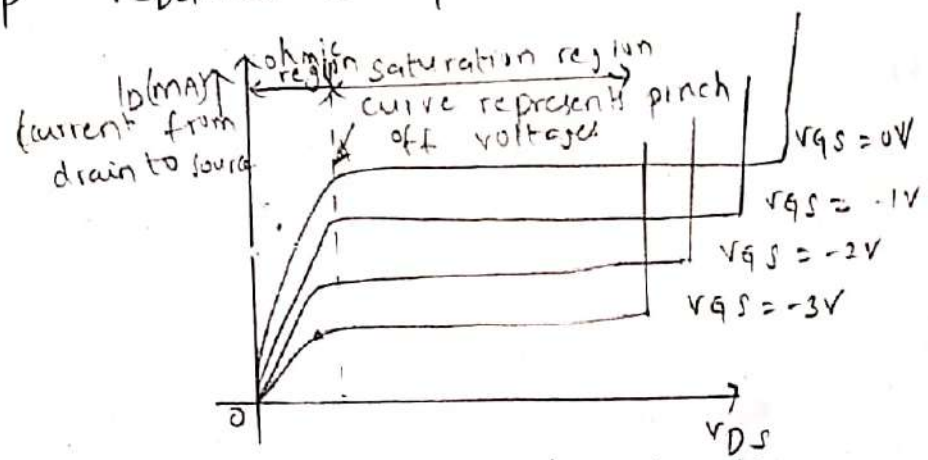
The JFET is always operated with gate-Source Pn junction reverse-biased.

JFET VI characteristics:

To understand electrical behaviour of a JFET, it is necessary to study the interrelation of the current and voltages in JFET. These relationships can be plotted graphically which are commonly known as characteristics of JFET. The important characteristics of JFET are drain characteristics and transfer characteristics. The following section explains these characteristics in detail.

Drain V-I characteristics for n-channel JFET

Fig 6.10 shows the drain characteristics of a n-channel JFET. The curves represent relationship between the drain current I_D and drain to source voltage V_{DS} for different values of V_{GS}. Fig 6.11 shows the experimental setup required to plot this characteristics.



6.10 Drain V-I characteristics of n-channel JFET

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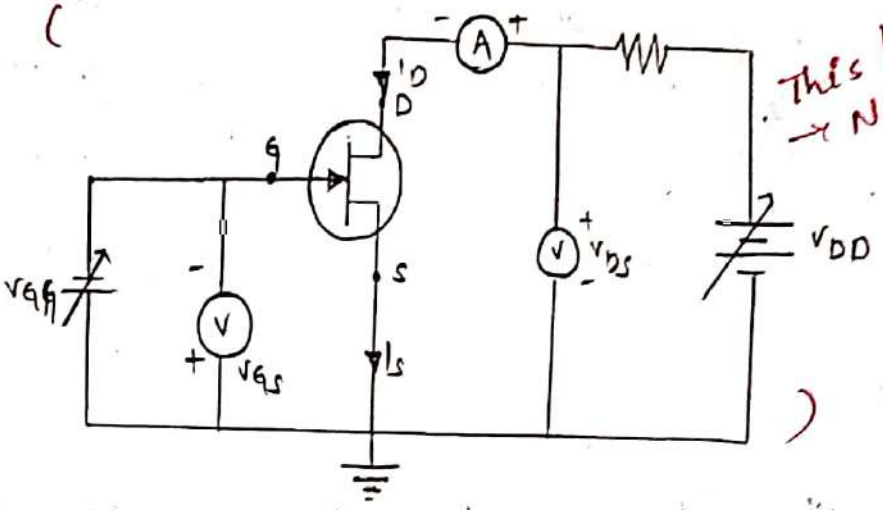

This figure → No need

Operation:-

6.11 Experimental setup to plot JFET Characteristics

From this characteristics we observe following points:

1: V_{GS} and V_{DS} both = 0:

When $V_{GS}=0$ the channel is entirely open. But $V_{DS}=0$, so there is no attractive force for the majority carriers and hence drain current does not flow.

2. Self pinch-off at no bias ($V_{GS}=0$):

At $V_{GS}=0$, in response to small applied voltage V_{DS}, the n-type bar acts as a simple semiconductor resistor, and the current I_D increases linearly with V_{DS}. As V_{DS} increases, the voltage drop along the channel also increases. The increase in voltage drop increases the reverse bias on gate source junction and causes the depletion regions to penetrate into the channel, reducing channel width. The effect of reduction in channel width provides more opposition to increase in drain current I_D. Thus, rate of increase in I_D, with respect to V_{DS} is now reduced. This is shown by the curved shape in the characteristics

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At some value of V_{DS}, drain current I_D cannot be increased further, due to reduction in channel width. Any further increase in V_{DS} does not increase drain current I_D. I_D approaches the saturation value. The voltage V_{DS} at which the current I_D reaches to its constant saturation level is called 'Pinch of voltage', V_p.

3. V_{GS} with negative bias:

When an external bias, of say -1V is applied, between the gate and source, the gate channel junctions are further reverse biased, reducing the effective width of the channel available for conduction. Because of this, drain current will reduce and pinch off voltage is reached to a lower drain current than when $V_{GS} = 0$, as shown in fig. 6.10.

By applying several values of negative external bias voltage (V_{GS}) a family of curves are obtained. It can be observed that for more negative values of V_{GS}, the pinch-off voltage is reached at lesser values of I_D.

4. Breakdown region:

We can observe from fig 6.10 that if we increase value of V_{DS} beyond pinch-off voltage, V_p, the drain current I_D remains constant, upto certain value of V_{DS}. If we further exceed V_{DS}, the voltage will be reached at which the gate-channel junction breaks down, due to avalanche effect

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At this point the drain current increases very rapidly, and the device may be destroyed.

It can be observed that the values of V_{DS} for breakdown are reduced as the negative gate bias is increased.

Ohmic and Saturation regions:

It is seen that the drain characteristics of JFET is divided into two regions: ohmic region and Saturation region. In ohmic region, the drain current I_D varies with V_{DS} and the JFET is said to behave as voltage variable resistance. In the saturation region, the drain current I_D remains freely constant and does not vary with V_{DS}. Saturation in FET is refered to the limiting value to drift velocity. Thus the number of carriers that can be transported through the channel per unit time is limited or saturated and I_D remains constant. To use FET as an amplifier, it is operated in this Saturation region.

Cut-off:

As we know, for an n-channel JFET, the more negative V_{GS} causes drain current to reduce and pinchoff voltage to reach at a lower drain current. When V_{GS} is made sufficiently negative, I_D is reduced to 0, as shown in Fig 6.12. This is caused by the widening of depletion region to a

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Point where it completely closes the channel. The value of V_{GS} at the cut-off point is designated as $V_{GS(OFF)}$.

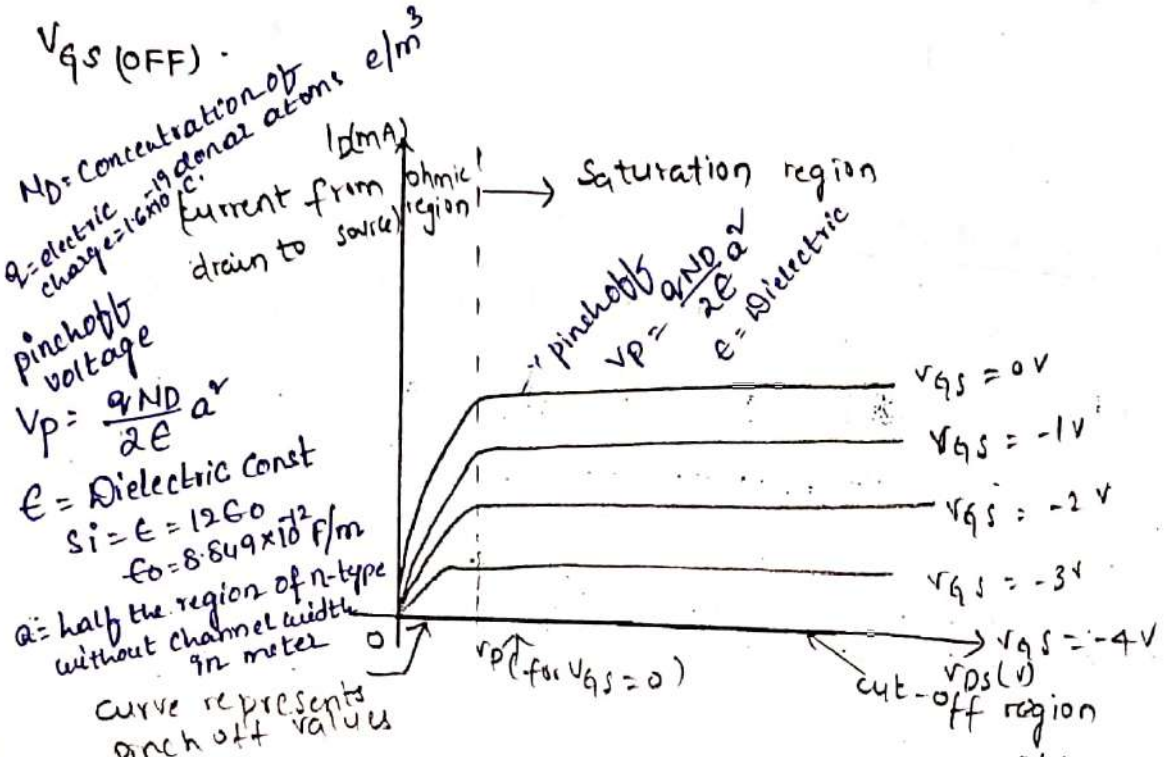

Fig 6.12 n-channel JFET characteristics with $I_{DSS} = 8mA$ & $V_{GS(off)} = -4V$

Key point:

1. Do not confuse cut-off with pinch off. The pinch off voltage V_p is the value of V_{DS} at which the drain current I_D reaches a constant value for a given value of V_{GS}.

2. The cutoff voltage $V_{GS(off)}$ is the value of V_{GS} at which the drain current is 0. I_D is 0 only when magnitude of V_{GS} is equal to or greater than the magnitude of V_p.

Relation of $V_{GS(off)}$ and V_p:

I_D is 0, when $V_{GS} = -V_p$, because a 0 drain current corresponds to an off, condition, the magnitude of V_p is equivalent to the magnitude of $V_{GS(off)}$

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Most JFET data sheets specify a value only for $V_{GS(off)}$ and not for V_p. But once we know $V_{GS(off)}$ we also know V_p. For example if $V_{GS(off)} = -4V$, then $V_p = 4V$.

The p-n junction between gate and source is reverse biased and the gate current is practically zero. Then the resistance between gate and source will be very large, ideally infinite. Thus input impedance of FET is very large. Also we have seen that the drain current depends on V_{GS} and almost independent of V_{DS}. By changing V_{GS}, I_D can be varied. Hence FET is basically a voltage controlled device. The input voltage controls the output current.

Drain V-I characteristics for p-channel JFET:

In a p-channel JFET the source is positive w.r.t drain. Here the source is the source of holes which flow through the channel to the drain. The pinch-off is achieved by making the source to gate voltage V_{SG} negative there by reverse biasing the p-n junction diode formed by the channel and gate.

The fig 6.13 shows the drain characteristics of p-channel JFET. Note the similarities between these characteristics and those shown for n-channel JFET in fig 6.10.

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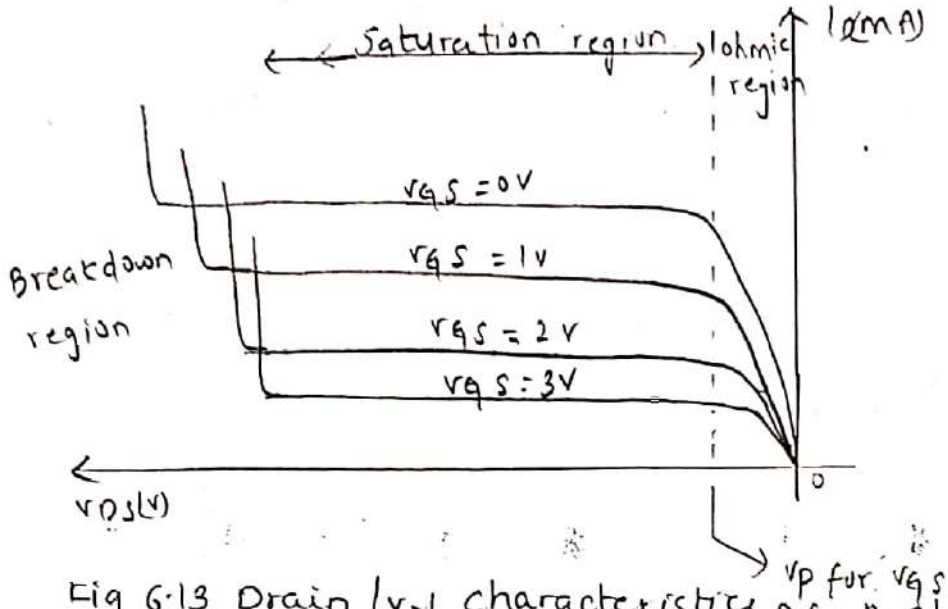

Fig 6.13 Drain / v-I characteristics of p-channel JFET

Key point: The curves are identical except that voltage V_{GS} and V_{DS} have reversed polarities and current I_D flows in reverse direction.

Transfer characteristics for n-channel JFET:

Fig 6.14 shows the transfer characteristics of n-channel JFET. The curves represent relationship between drain current I_D and gate to source voltage V_{GS}.

From this characteristics we observe following points:

1. The relationship between the drain current I_D and V_{GS} is non linear. This relationship is defined by Shockley's equation.

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \longrightarrow (1)$$

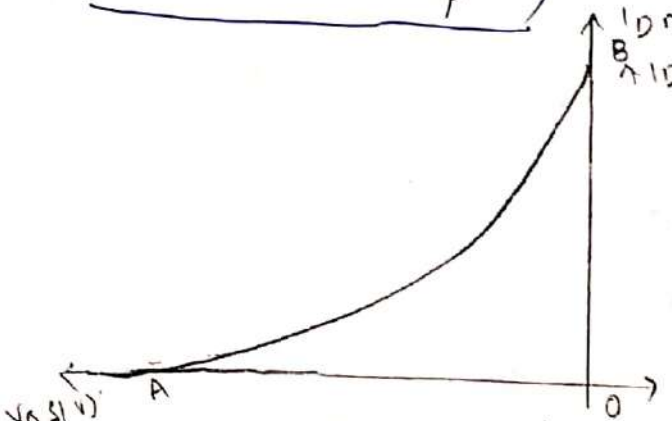

Fig 6.14 Transfer characteristics of n-channel JFET

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The squared term of the equation will result in a non-linear relationship between I_D and V_{GS}, producing a curve that grows exponentially with decreasing magnitudes of V_{GS}.

From equation, we can also write

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right) \longrightarrow (2)$$

In the equation values of I_{DSS} and V_P are constant value of V_{GS} controls I_D.

2. A point 'A' at the bottom end of the curve on V_{GS}-axis represents $V_{GS(off)}$ and point 'B' at the top end of the curve on the I_D axis represents I_{DSS}. Thus this curve shows the operating limits of JFET.

$I_D = 0$ when $V_{GS} = V_{GS(off)}$

$I_D = I_{DSS}$ when $V_{GS} = 0$.

Obtaining the Transfer characteristics from Drain characteristics:

The transfer characteristics curve can be developed from the drain characteristics curves by plotting values of I_D for the values of V_{GS} taken from the set of drain curves in the pinch-off region. Each point on the transfer characteristics curve corresponds to specific values of V_{GS} and I_D on drain curves.

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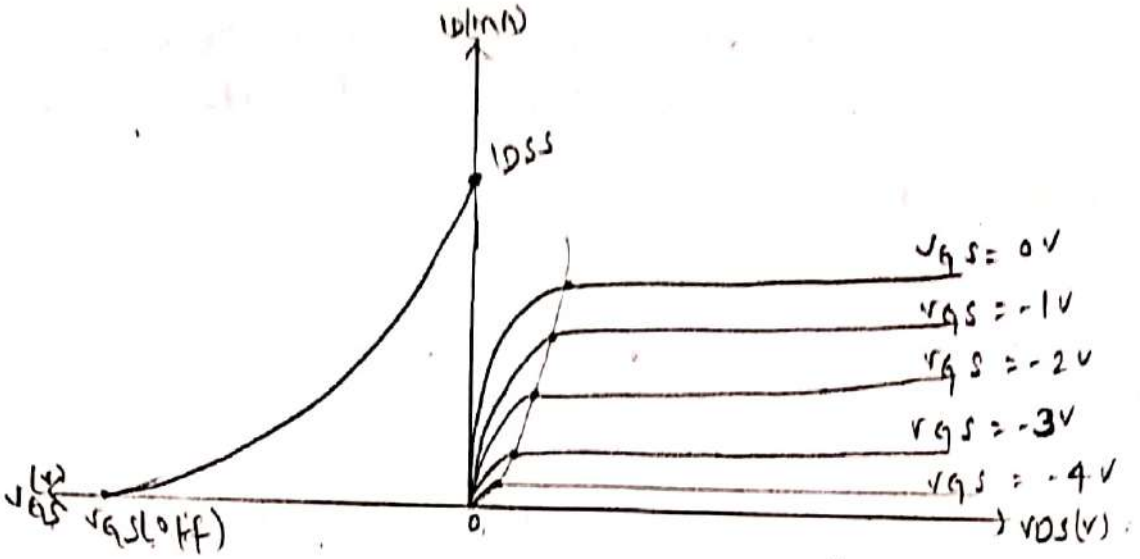

Fig 6.15 Obtaining the transfer characteristics from drain characteristics.

Transfer Characteristics for P-channel JFET:

The fig 6.16 shows the transfer characteristics of p-channel JFET. It is identical to transfer characteristics of n-channel JFET except that the polarities of v_{GS} and I_D are reversed.

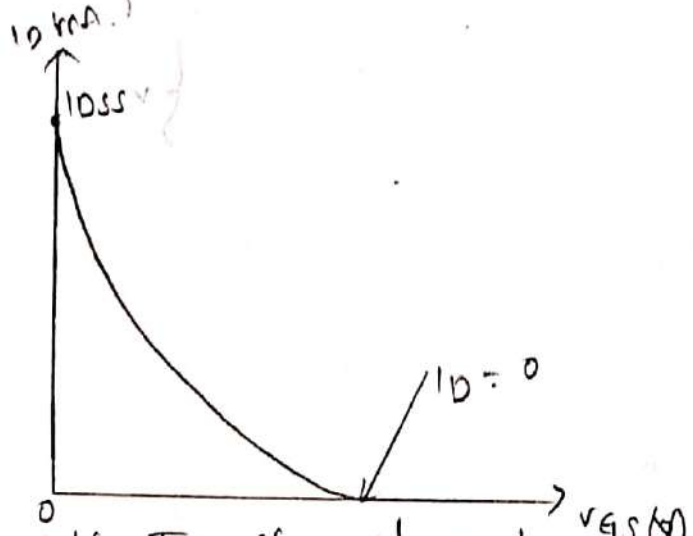

Fig 6.16 Transfer characteristics of p-channel JFET

Keypoint: Polarities of v_{GS} and I_D are reversed than that of the characteristics of n-channel JFET.

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JFET: Small Signal Model:

The JFET parameters are the major components of low frequency small signal model for JFET. Hence before examining the low frequency small signal model we see JFET parameters.

JFET Parameters:

The important parameters of JFET are as follows:

* Transconductance (g_m):
* Input resistance and capacitance
* Drain to source resistance (r_d)
* Amplification factor (μ)

Transconductance:

The transconductance g_m is the change in the drain current for given change in gate to source voltage with the drain to source voltage constant as shown in fig 6.17

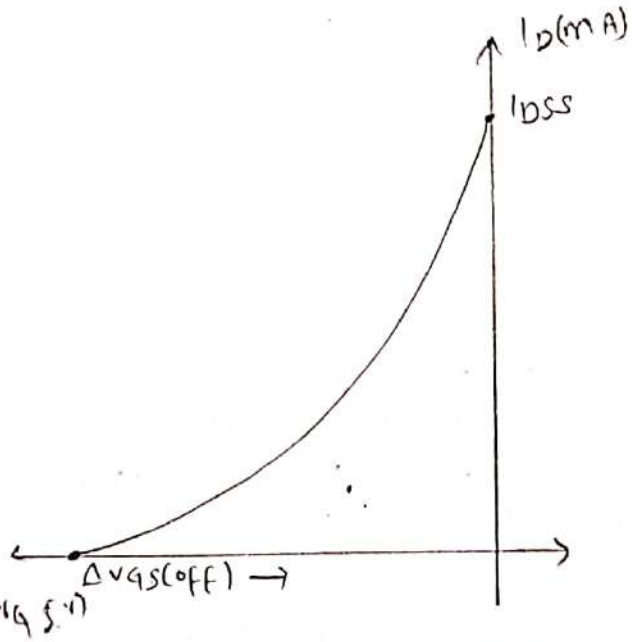

Fig 6.17 Transconductance g_m varies depending on the bias point (V_{GS})

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Looking at Fig 6.17 we can say that the slope of the transfer characteristic. Since the slope varies g_m also varies. g_m has a greater value near the top of curve than it does not near the bottom.

The transconductance g_m is defined as

$$g_m = \frac{\Delta I_D}{\Delta V_{GS} / V_{DS} \text{ constant}} \quad \text{—— (1)}$$

The transconductance g_m is also called mutual conductance. The practical unit for g_m is mS (millisiemen) or mA/V. we can calculate an approximat value for g_m at any point on the transfer characteristic curve using the following equation.

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_{GS(off)}}\right] \quad \text{—— (2)}$$

where g_{mo} is the value of g_m for $V_{GS} = 0$ and is given by,

$$g_{mo} = \frac{-2I_{DSS}}{V_p} \quad \text{—— (3)}$$

This can be proved as given below, we know that

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2$$

Differentiating this equation w.r.t V_{GS} we get

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{-2I_{DSS}}{V_p}\left[1 - \frac{V_{GS}}{V_p}\right]$$

$$g_m = g_{mo}\left[1 - \frac{V_{GS}}{V_p}\right] \quad \text{where } g_{mo} = \frac{-2I_{DSS}}{V_p}$$

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Input Resistance and Capacitance:

We know that JFET operates with its gate source junction reverse biased. Therefore the input resistance at the gate is very high. This high input resistance is one advantage of the JFET over bipolar Transistor. JFET data sheets often specify the input resistance by giving a value of gate reverse current I_{GSS}, at a certain gate to source voltage V_{GS}. The input resistance can then be determined using the following equation,

$$R_{IN} = \left|\frac{V_{GS}}{I_{GSS}}\right|$$

For example, if a maximum I_{GSS} of 10nA for $V_{GS} = 10V$ at 25°C. Therefore

$$R_{IN} = \left|\frac{10V}{10nA}\right| = 1000M\Omega$$

From the data sheet of 2N3909 we can also observe that I_{GSS} is 1.0μA for $V_{GS} = 10V$ at 100°C. This shows that I_{GSS} increases with temperature.

$$R_{IN} = \left|\frac{10V}{1\mu A}\right| = 10M\Omega$$

Key point:

The input resistance decreases with increase in temperature.

Drain to Source Resistance:

From the drain characteristics, the important Parameter of JFET, drain resistance r_d, can be calculated.

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The drain resistance r_d is the ac resistance between drain and source terminals when the JFET is operating in saturation region. It is the reciprocal of slope of the drain characteristic in the saturation region. It is given by

** $$r_d = \frac{\Delta V_{DS}}{\Delta I_D}\Big|_{V_{GS}\ \text{constant}} \quad \text{—— (4)}$$

Since the characteristics in the saturation region is almost flat, r_d is not easily determined from the characteristics: Values of r_d range from about 50 kΩ to several hundred kΩ. Since r_d is usually the output resistance of the JFET, it may also be expressed as an output admittance $|y_{os}| = \frac{1}{r_d}$.

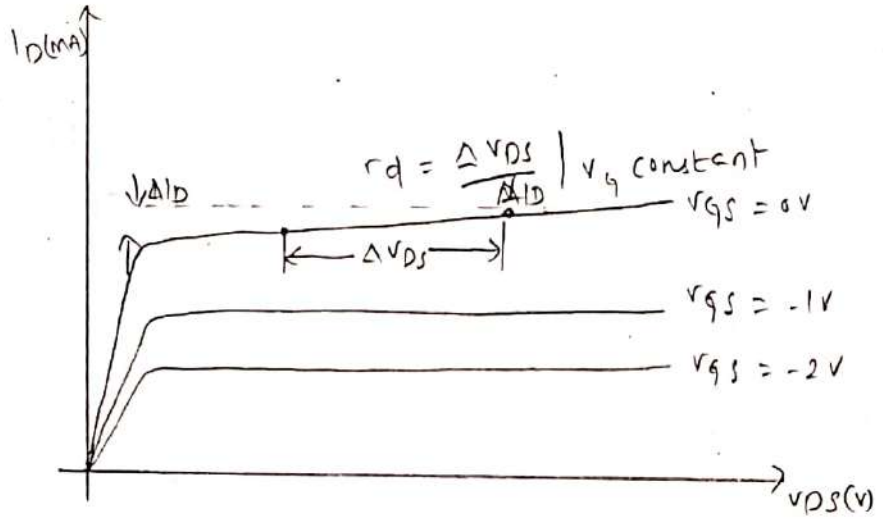

Fig 6.18 Drain characteristics of n channel JFET

Amplification factor:

Amplification factor, denoted by μ, is defined as

Amplification factor ** $$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}}\Big|_{I_D\ \text{constant}}$$

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Relationship between μ, r_d, g_m :-

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} = \frac{\Delta V_{DS}}{\Delta I_D} \times \frac{\Delta I_D}{\Delta V_{GS}}$$

$$\mu = r_d \times g_m \quad \text{— (5)}$$

Key point:

Since parameter μ is the ratio of two similar quantities viz. ratio of two voltages; μ is unitless.

W.K.T; drain to source current of JFET is controlled by gate to source voltage. The change in the drain current due to change in gate to source voltage can be determined using the transconductance factor g_m.

$$\Delta I_d = g_m \Delta V_{GS} \quad \text{— (6)}$$

W.K.T, in BJT the relation between an output and input quantity is given by amplification factor β whereas JFET this relation is given by transconductance factor g_m.

Power Dissipation (P_D) :

The power dissipation in JFET is given by

$$P_D = I_D \times V_{DS}$$

Expression for Saturation Drain Current:

In a transfer characteristics we have seen that the relationship b/n the drain an current I_D and

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gate to source voltage v_{GS} is non-linear. This relationship is defined by Shockley's equation.

$$I_D = I_{DSS}\left[1 - \frac{V_{GS}}{V_p}\right]^2 \quad -(7)$$

The squared term of the equation will result in a non-linear relationship between I_D and v_{GS} producing a curve that grows exponentially with decreasing magnitudes of V_{GS}.

In eq (7) I_D represents saturation drain current. I_{DSS} is the value of I_D when $v_{GS}=0$ and V_p is the pinchoff voltage. Differentiating this expression, we get

$$\frac{\partial I_D}{\partial v_{GS}} = I_{DSS} \times 2\left[1 - \frac{V_{GS}}{V_p}\right]\left[-\frac{1}{V_p}\right]$$

$$\therefore g_m = \frac{-2I_{DSS}}{V_p}\left[1 - \frac{V_{GS}}{V_p}\right] \text{ since } \left.\frac{\partial I_D}{\partial v_{GS}}\right|_{\substack{v_{DS} \\ \text{constant}}} = g_m \quad -(8)$$

From equation (7) we also have

$$1 - \frac{V_{GS}}{V_p} = \sqrt{\frac{I_D}{I_{DSS}}} \quad -(9)$$

Substituting this value in eq (8) we have

$$g_m = \frac{-2I_{DSS}}{V_p}\sqrt{\frac{I_D}{I_{DSS}}}$$

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$$= \frac{-2\sqrt{I_D I_{DSS}}}{V_p} \quad -(10)$$

When $V_{GS} = 0$, $g_m = g_{mo}$ then from eq(8)

$$g_{mo} = \frac{-2I_{DSS}}{V_p}$$

Therefore from equations (8) and (11)

$$g_m = g_{mo}\left(1 - \frac{V_{GS}}{V_p}\right) \quad -(12)$$

The equation (10) shows that g_m varies as the square root of the saturation current I_D and equation (12) shows that g_m decreases linearly with increase of V_{GS}.

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MOSfet:

MOSFET (metal oxide semiconductor field effect transistor). It is a second ategory of field effect transistor. It became a practical reality in ne 1970s. The MOSFETs, compared to BJTs, can be made very small nd hence can be used to design high density VLSI circuits.

The MOSFET differs from the JFET in that it has no p-n junction tructure; instead, the gate of the MOSFET is insulated from the channel by a silicon dioxide (SiO_2) layer. Due to this the input esistance of MOSFET is greater than JFET. Because of the insulated gate, OSFETs are also called IGFETs. TWO basic types of MOSFETs are: depletion (D) MOSFET and enhancement (E) MOSFET. The terms depletion and enhancement define their basic mode of operation.

Depletion MOSFET:

onstruction of n-Channel MOSFET:

Two highly doped n regions are diffused into a lightly doped P type substrate. These two highly doped n regions represent source and drain. In some cases substrate is internally connected to the source terminal.

The source and drain terminals are connected through netallic contacts to n-doped regions linked by an n-channel. The gate is also connected to a metal contact surface but emains insulated from the n-channel by a very thin layer of dielectric material, silicon dioxide (SiO_2). This layer is in-

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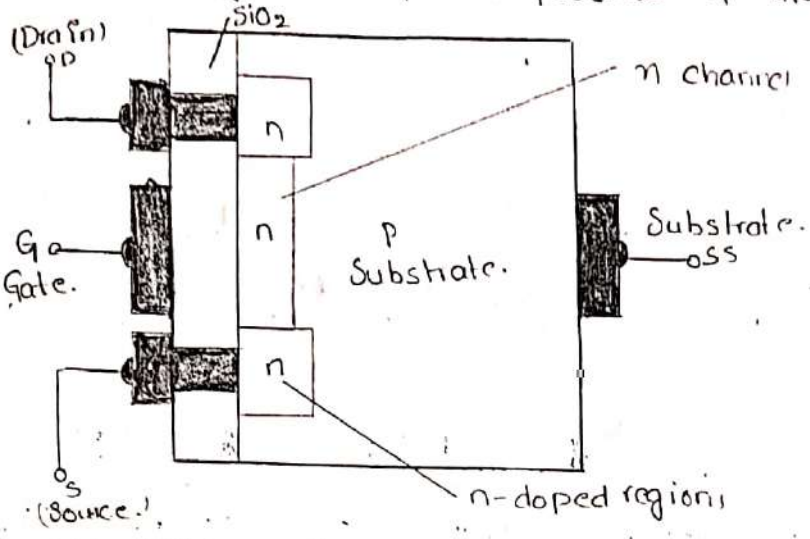
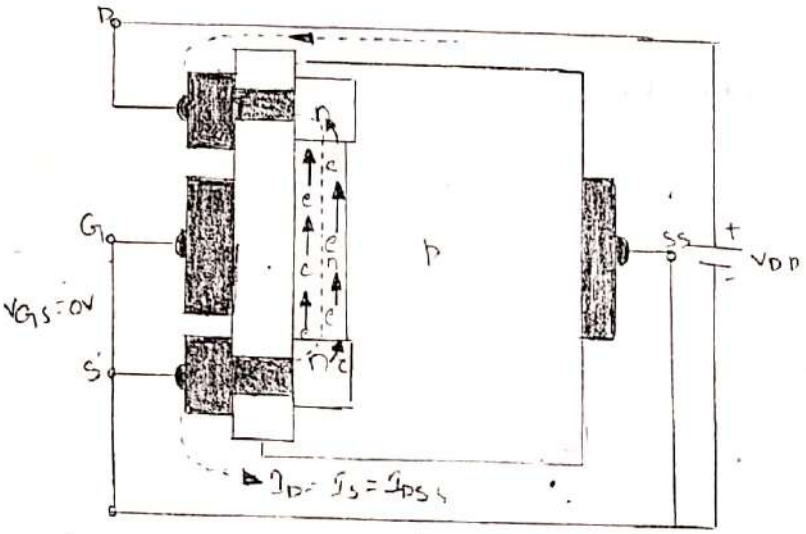
rect electrical connection between the gate terminal and the channel ; a MOSFET, increasing the input impedance of the device.



Operation, Characteristics and Parameters of n-channel MOSFET:-

On the application of drain to source voltage, V_{DS}, and keeping gate to source voltage to zero by directly connecting gate terminal to the source terminal, free electrons from the n-channel are attracted towards positive potential of drain terminal. This establishes current through the channel to be denoted as I_{DSS} at $V_{GS}=0V$.

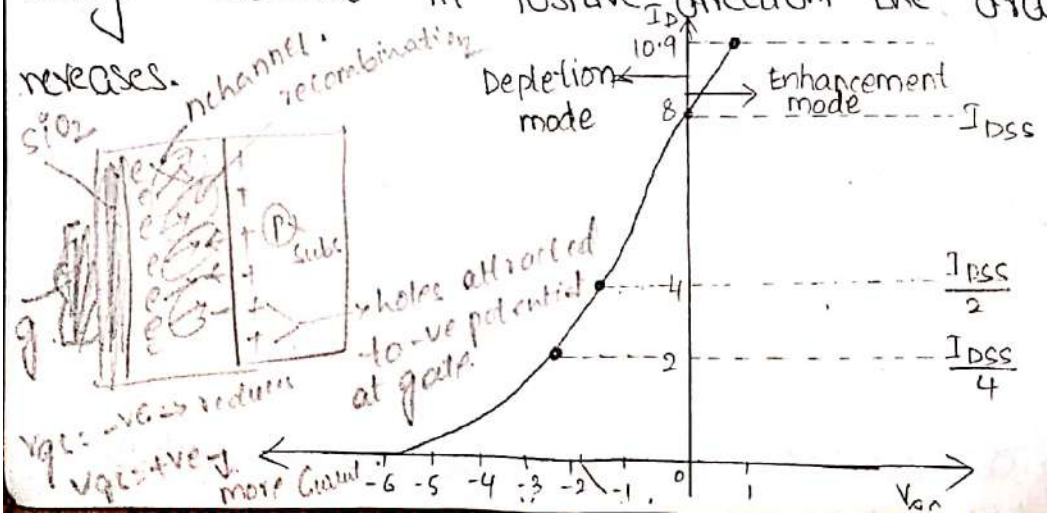

D
n
e
e
e

The level of recombination between electrons and holes depends on the magnitude of the negative voltage applied at the gate. This recombination reduces the number of free electrons in the n-channel for the conduction, reducing the drain current.

In other words we can say that, due to recombinations, n-channel is depleted of some of its electrons, thus decreasing the channel conductivity. The greater the negative voltage applied at the gate, the greater the depletion of n-channel electrons. The level of drain current will reduce with increasing negative bias for V_{GS} as shown in the transfer characteristics of depletion type MOSFET.

Transfer characteristics for an n-channel depletion type MOSFET:-

For positive values of V_{GS} the positive gate will draw additional electrons from the p-type substrate due to reverse leakage current and establish new carriers through the collisions between accelerating particles. Because of this, as gate to source voltage increases in positive direction, the drain current also increases.



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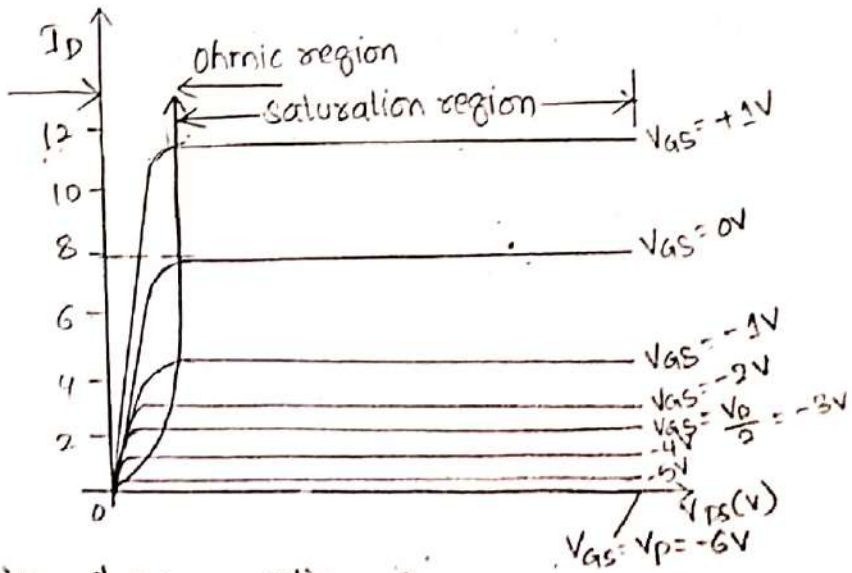
rain Characteristics for an n-channel depletion type MOSFET:-

The application of a positive gate to source voltage has nhanced the level of free carriers in the channel compared to at encountered with V_{GS} = 0V. For this reason the region of sitive gate voltages on the drain or transfer characteristics is eferred to as enhancement region and the region between ut-off and the saturation levels of I_{DS} referred to as epletion region. Drain characteristics for an n-channel depletion ype MOSFET is similar to that of JFET. The only difference s that it has positive part of V_{GS}.

Key points:

1. $I_D = 0$ corresponds to $V_{GS(off)}$, $V_{GS(off)} = -V_p$.
2. $V_{GS} = 0$ corresponds to I_{DSS}.
3. Both positive and negative values of V_{GS} can be used to bias D-MOSFET.



Drain characteristics for an n-channel depletion type

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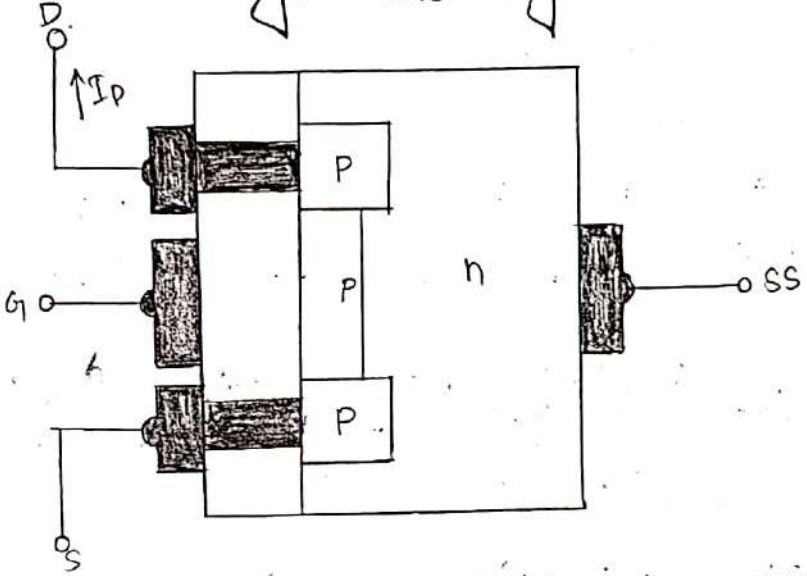
P-Channel Depletion Type MOSFET:

The construction of the P-channel depletion type MOSFET is exactly opposite of that of n-channel depletion type MOSFET. Here, the substrate is of n-type and regions and channel are of p-type.



Drain characteristics of P-channel depletion type MOSFET:

Voltage polarities and current directions are reversed. The drain characteristics appear exactly, but V_{DS} with negative values, I_D in the opposite direction and V_{GS} having opposite polarities.

Transfer characteristics of P-channel depletion type MOSFET:-

In the P-channel depletion type MOSFET, the transfer characteristics is a mirror image about the I_D axis (Y-axis) of the transfer characteristic of n-channel depletion type MOSFET, since the V_{GS} is positive in P-channel depletion region.

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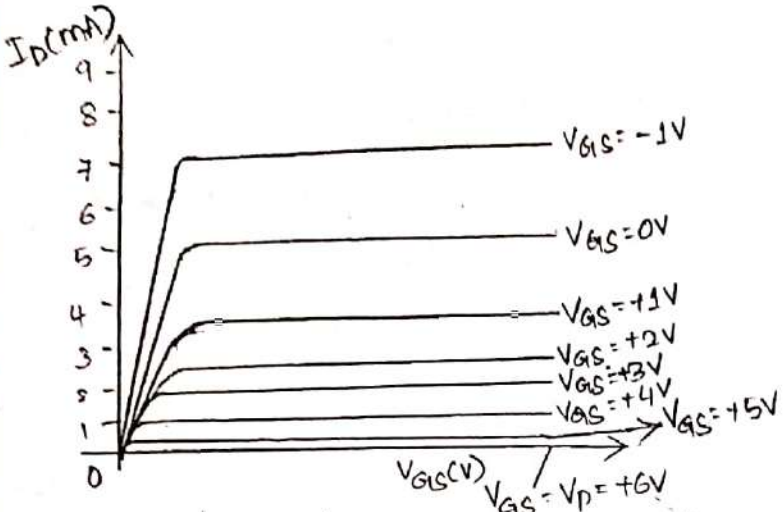
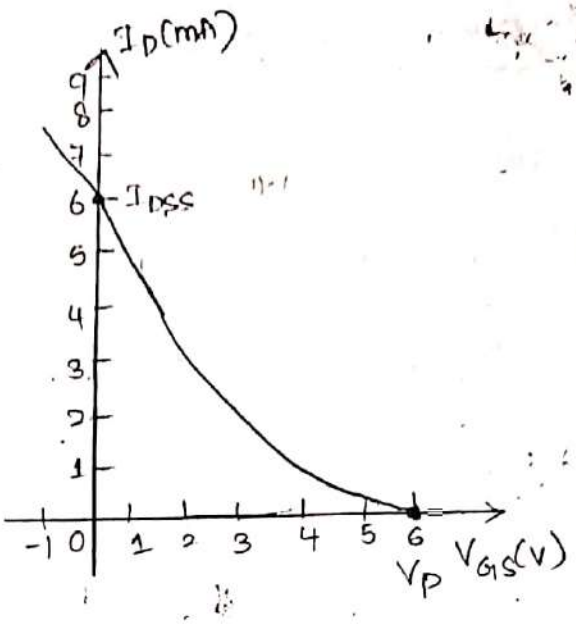
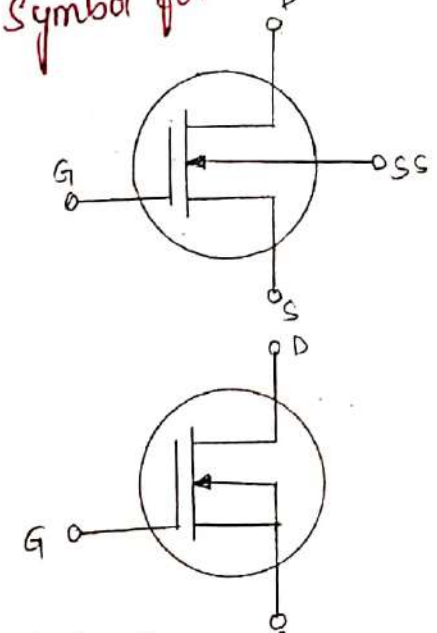




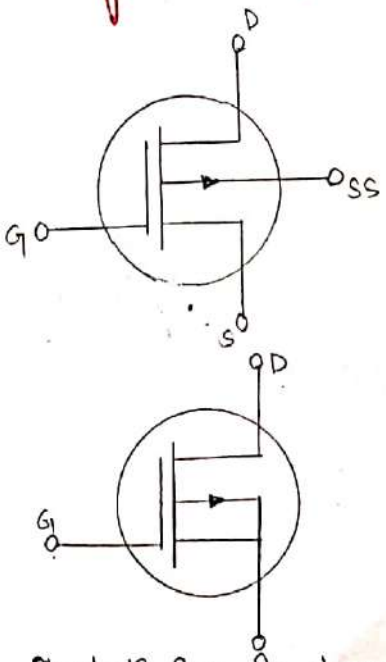
D)- MOSFET Symbols :-

In the symbol insulation between gate and channel is represented by a space between the gate and other terminals of the symbol. The vertical line represents that the channel is connected between the drain and source and is "supported" by the substrate. Two symbols are given for each type of channel to reflect the fact that, in some cases it is internally shorted to source terminal.

Symbol for N-channel



Symbols for p-channel



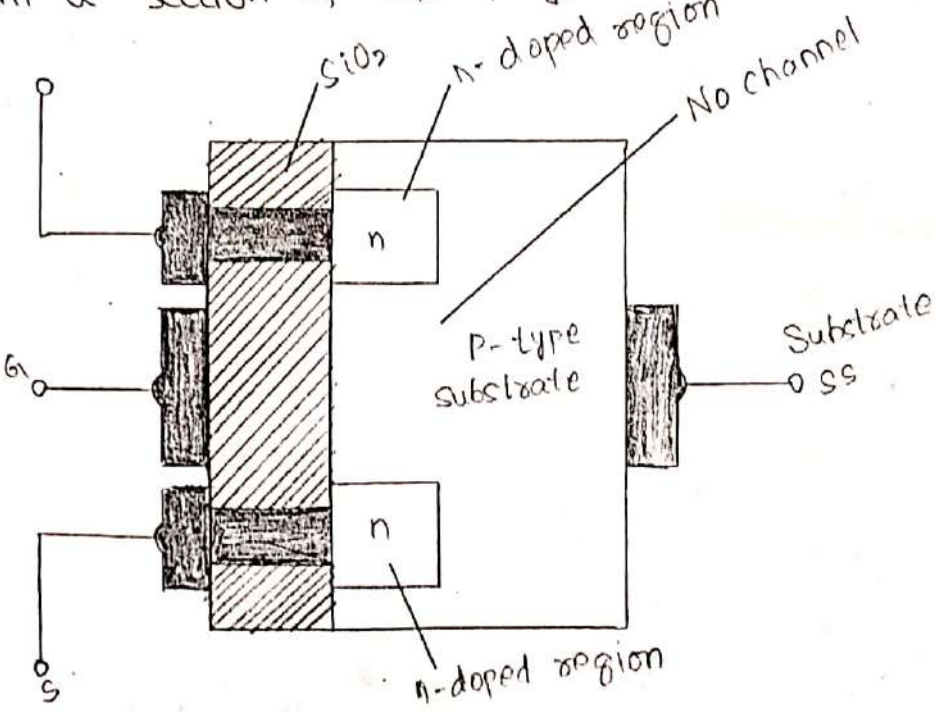
Symbols for p-channel type

Enhancement MOSFET (E-MOSFET):-

This type of MOSFET operates only in the enhancement mode and has no depletion mode. It differs in construction from the depletion MOSFET in that it has no physical channel.

Construction of n-channel E-MOSFET:-

Two highly doped n regions are diffused into a lightly doped p-type substrate. The source and drain are taken out through metallic contacts to n-doped regions. But the channel between two n-regions is absent in the enhancement type MOSFET. The SiO_2 layer is still present to isolate the gate metallic platform from the region between the drain and source, but now it is simply separated from a section of the p-type material.



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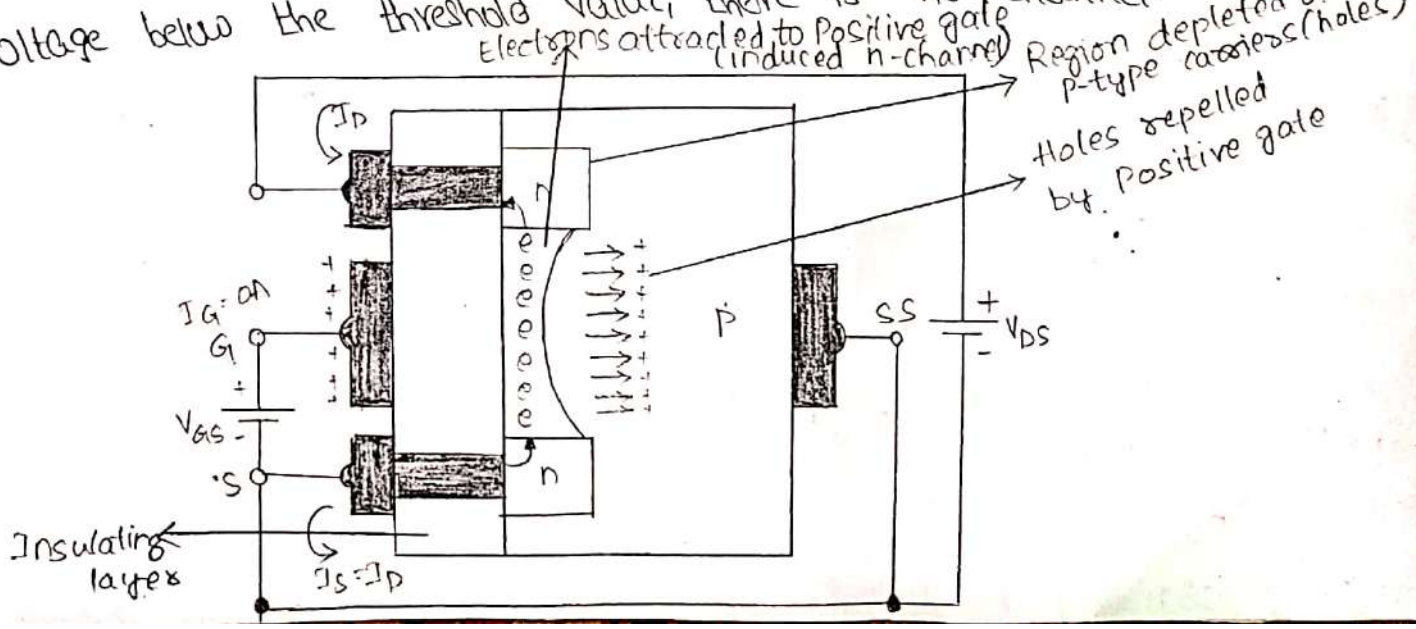
Operation, characteristics and parameters of n-channel E-MOSFET:

On application of drain to source voltage V_{DS} and keeping gate to source voltage zero by directly connecting gate terminal to the source terminal, practically zero current flows - quite different from the depletion type MOSFET and JFET - If we increase magnitude of V_{GS} in the positive direction, the concentration of electrons near the SiO_2 surface increases. At a particular value of V_{GS} there is a measurable current flow between drain and source. This value of V_{GS} is called threshold voltage denoted by V_T. Thus we can say that in an enhancement type n-channel MOSFET, a positive gate voltage above a threshold value induces a channel and hence the drain current by creating a thin layer of negative charges in the substrate region adjacent to the SiO_2 layer. The conductivity of the channel is enhanced by increasing the gate to source voltage and thus pulling more electrons into the channel. For any voltage below the threshold value, there is no channel.



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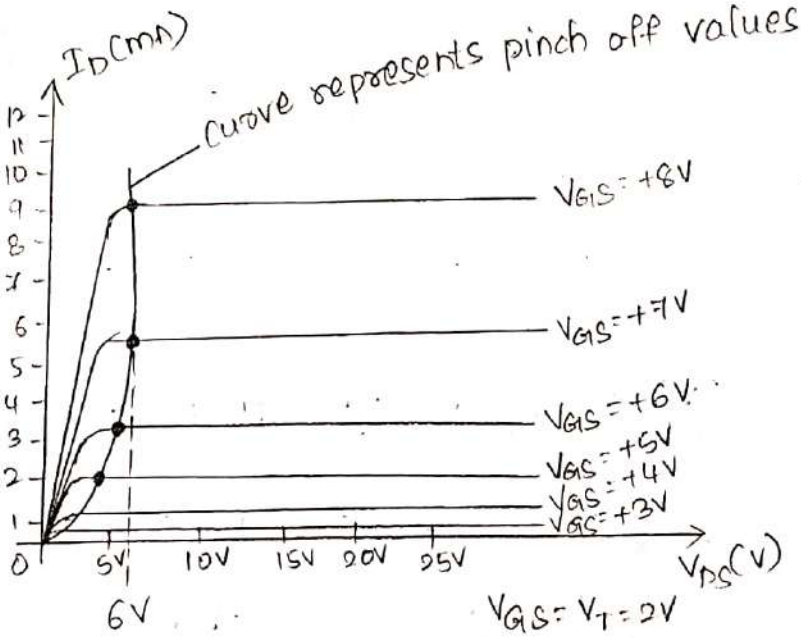
Drain characteristics of an n-channel enhancement type MOSFET:-

The channel does not exist with $V_{GS} = 0V$ and "enhanced" by the application of a positive gate to source voltage, this type of MOSFET is called an enhancement type MOSFET.

V_{GS} increases beyond the threshold level, the density of free carriers in the induced channel increases, increasing the drain current. However, at some point of V_{DS}, for constant V_{GS}, the drain current reaches a saturation level. The leveling off of I_D is due to a pinch-off process, is as described earlier for the JFET.



Transfer characteristic for n-channel enhancement type MOSFET:-

This characteristic is quite different from characteristic that we obtained for JFET and depletion type MOSFET. For an n-channel enhancement type MOSFET it is now totally in the positive V_{GS} region and as we know I_D does not flow till $V_{GS} = V_T$.

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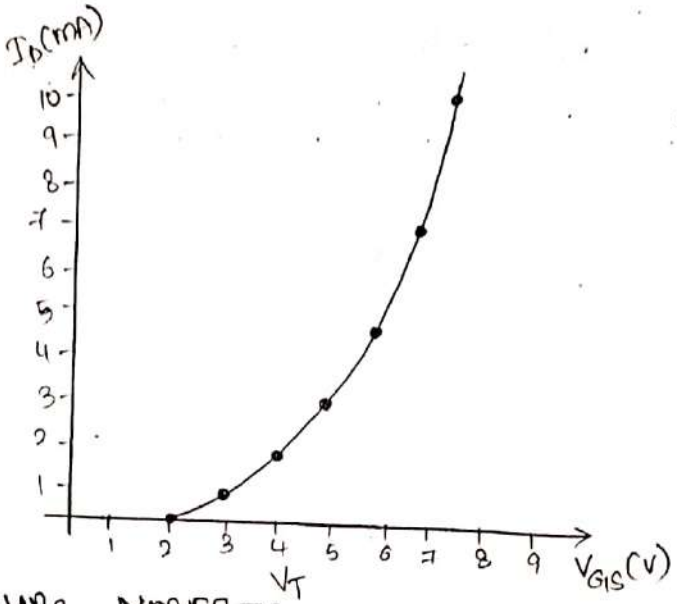
For $V_{GS} > V_T$ the relationship between drain current and V_{GS} is nonlinear and it is given as

$$I_D = K(V_{GS} - V_T)^2.$$

The K term is a constant that is a function of the construction of the device. The value of K can be determined from equation.

$$K = \frac{I_{D(ON)}}{(V_{GS(ON)} - V_T)^2}$$



-channel Enhancement Type MOSFET:-

The construction of the P-channel enhancement type MOSFET is exactly opposite to that of n-channel enhancement type MOSFET. Here, the substrate is of n-type and regions are of P-type.

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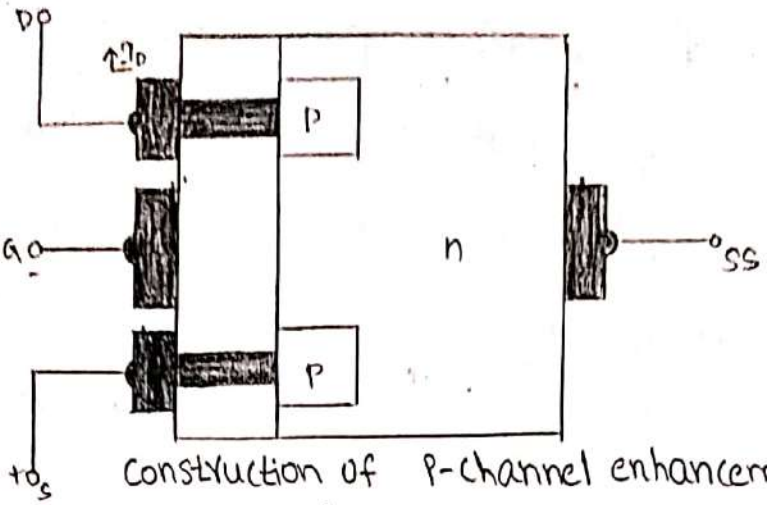
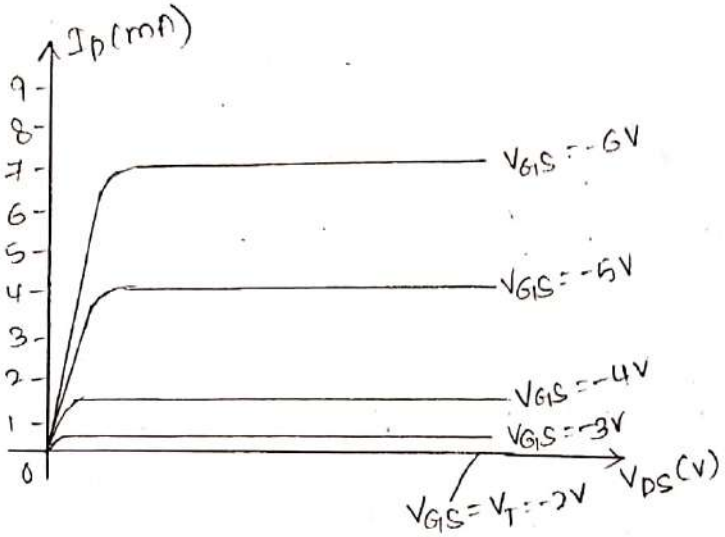


Construction of P-channel enhancement type MOSFET

Drain characteristics of P-Channel enhancement MOSFET:-

AS. shown in figure voltage polarities and current directions are reversed. The drain characteristics appear exactly. But with V_{DS} negative values, I_D in opposite direction and V_{GS} having opposite polarities.



Transfer characteristics of P-channel enhancement type MOSFET:-

In the P-channel enhancement type MOSFET, the transfer characteristic is a mirror image about the I_D axis of the transfer characteristics of n-channel depletion type MOSFET, since the V_{GS} is negative.

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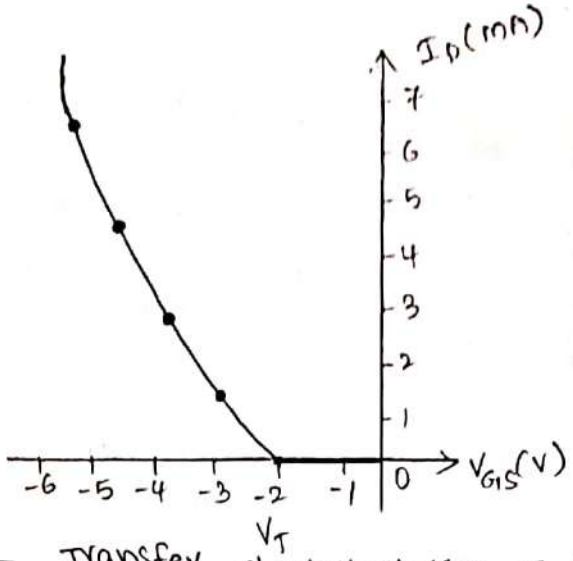
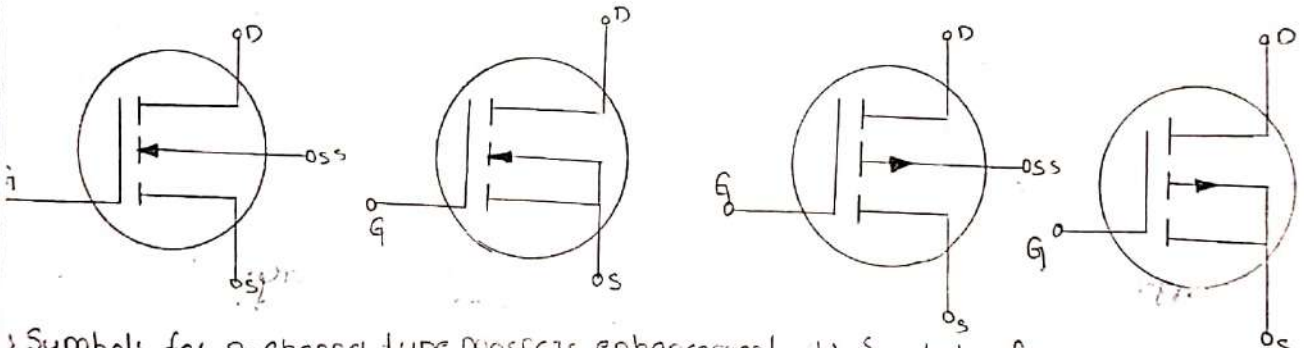


E-MOSFET Symbols:- Transfer characteristics of P-channel enhancement type MOSFET

The below figures shows graphic symbols for an n and p channel enhancement type MOSFET. The dashed line between drain and source represents the fact that a channel does not exists between the two under no-bias conditions. It is the only difference between the symbols for the depletion type and enhancement type.



a) Symbols for n-channel type MOSFETs enhancement b) Symbols for P-channel type MOSFETs enhancement

Channel Length Modulation:-

In the figure, the thickness of the induced channel layer qualitatively indicates the relative charge density. In this figure (a) applied V_{DS} is small and for this case the relative charge density is constant along the entire channel

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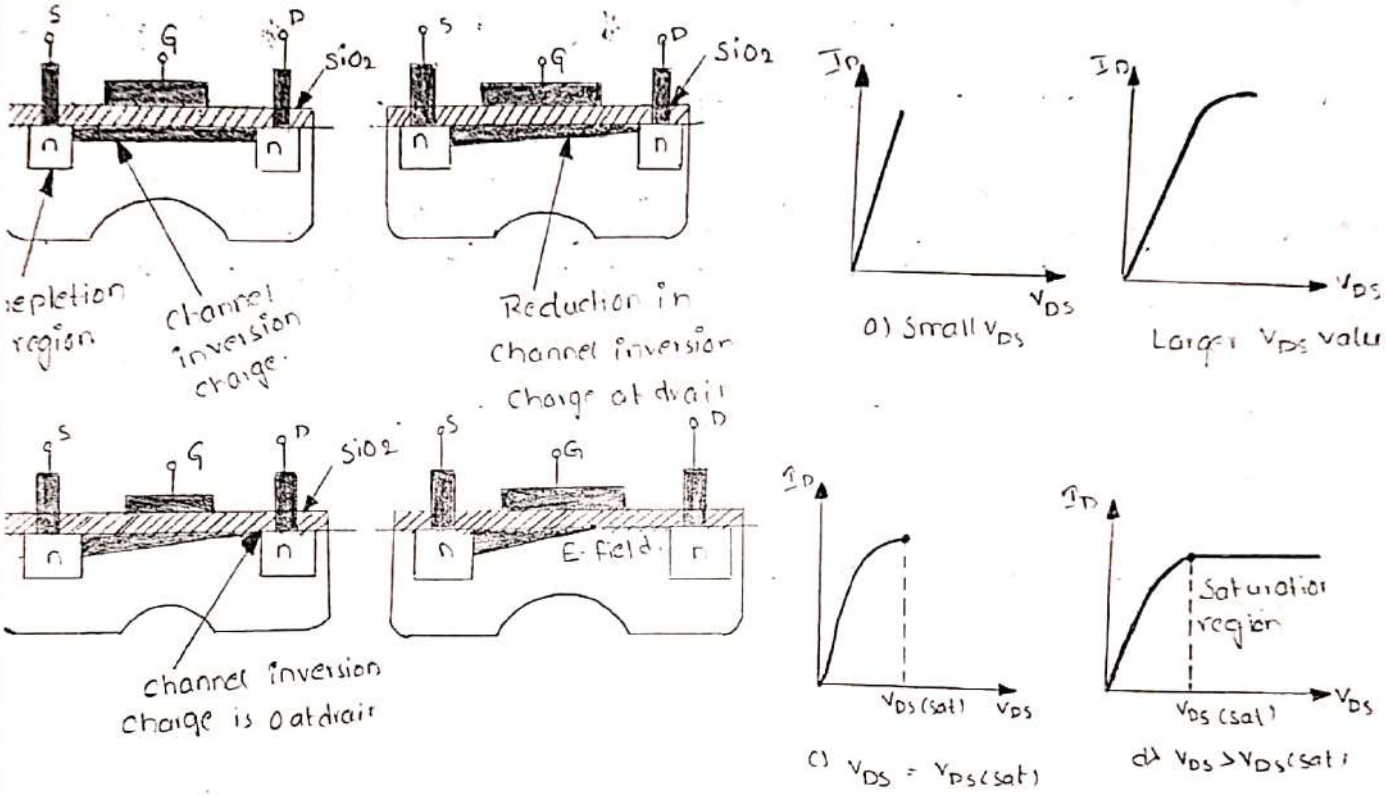
As the drain voltage increases, the voltage drop across the oxide near the drain terminal decreases, which means that the induced inversion charge density near the drain also decreases. The incremental conductance of the channel at the drain then decreases, which causes the slope of the I_D versus V_{DS} curve to decrease. This effect is shown in the versus curve



As V_{DS} increases to the point where the potential difference across the oxide at the drain terminal is equal to V_T, the induced inversion charge density at the drain terminal is zero. When V_{DS} becomes larger than $V_{DS(sat)}$, the point in the channel at which the inversion charge is just zero moves towards the source terminal. In this case, electrons enter the channel at the source, travel through the channel towards the drain, and then at the point where the charges once to zero, are injected into the depletion region

where they are swept by the E-field to the drain contact. It is observed that as V_{DS} increases beyond $V_{DS(sat)}$ effective channel length decreases, producing the phenomenon called "channel length modulation".

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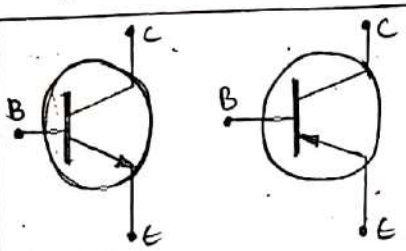
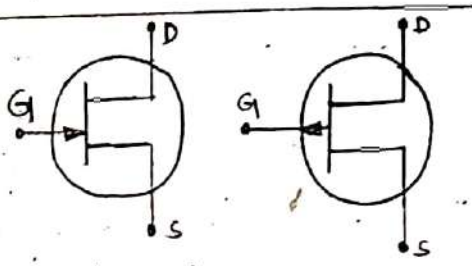
Comparision of BJT and FET :-

S.NO	Parameter	BJT	FET
1.	control element	current controlled device. Input current I_B controls output current I_C	voltage controlled device. Input voltage V_{GS} controls drain current I_D
2.	Device type	current flows due to both majority and minority carriers and hence bipolar device	current flows only due to majority carriers and hence unipolar device
3.	Types	npn and pnp	nchannel and p-channel
4.	symbols	 npn pnp	 n-channel p-channel
5.	configurations	CE, CB, CC	CS, CG, CD
6.	Input resistance	Less compare to JFET	High compare to BJT
7.	size	Bigger than JFET	smaller in construction than BJT, thus making them useful in Integrated-circuits
8.	sensitivity	Higher sensitivity to changes in the applied signals	Less sensitivity to changes in the applied voltage
9.	Thermal stability	Less	More
10.	Thermal runaway	exists in BJT, because of cummulative effect of increase in I_C with temperature, resulting increase in temperature in the device	Does not exist in JFET, because drain resistance r_d increases with temperature, which reduces I_D, reducing the I_D and hence the temperature of the device
11.	Ration of o/p to i/p	$\frac{\Delta I_C}{\Delta I_B} = \beta$	$\frac{\Delta I_D}{\Delta V_{GS}} = g_m$

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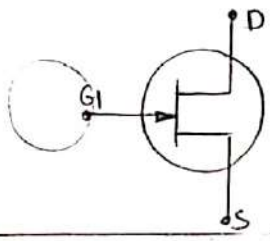
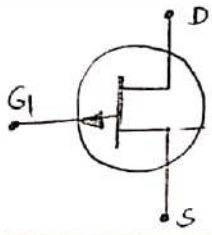
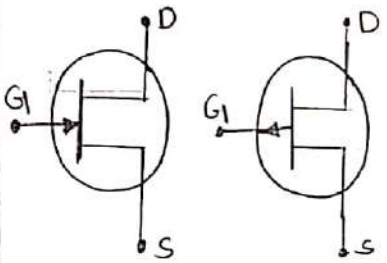
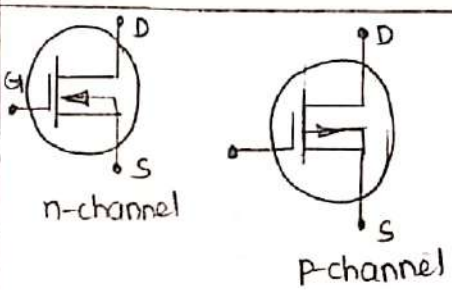
S.NO	Parameter	BJT	FET
12.	Relation between input and output	Linear	Non-linear
13.	Thermal noise	More in BJT as more charge carries cross junctions	Much lower in JFET as very few charge carriers cross the junction
14.	Gain bandwidth product	High	Low

Comparison of Transistors:-

comparison between N-channel and p-channel JFET

S.NO	N-channel JFET	p-channel JFET
1.		
2.	Electrons are the current carriers	Holes are the current carriers
3.	Mobility of electrons is large in N-channel JFET	Mobility of holes is poor in p-channel JFET
4.	Input noise is less	Input noise is more
5	Large transconductance	Less transconductance

comparison of FET and MOSFET

S.NO	parameter	JFET	MOSFET
1.	symbols.	 n-channel p-channel	 Depletion type

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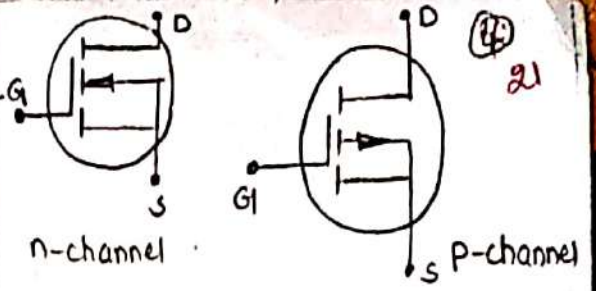
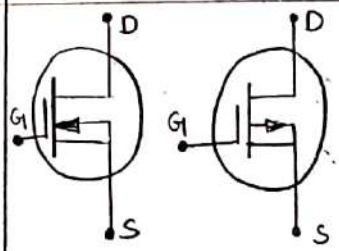
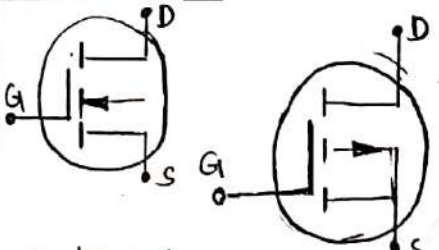
	—	—	 Enhancement type
2.	Types	(a) n-channel (b) p-channel	(A) n-channel depletion type MOSFET (B) p-channel depletion type MOSFET (c) n-channel enhancement type MOSFET (d) p-channel enhancement type MOSFET
3.	Operation mode	operated in depletion mode	operation in depletion and enhancement mode
4.	Input impedance	High (> 10 MHz)	Very high (> 10,000 MΩ)
5.	Gate	Gate is not insulated from channel	Gate is insulated from channel by a layer of SiO_2
6.	channel	channel exists permanently	channel exists permanently in depletion type MOSFET, but not in enhancement type MOSFET

comparison of D-MOSFET and E-MOSFET

SNO	Parameter	Depletion type	Enhancement type
1.	Symbols		
2.	operation	can be operated in depletion mode as well as enhance mode	can only be operated in enhance mode

Turnover

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S.NO	Parameter	Depletion type	Enhancement type
3.	channel	Exists permanently	channel is physically ... It is induced after appli... of positive gate voltage above the threshold value for n-channe enhancement type MOSFET and negative gate voltage above threshold value for p-channel enhancement type
4.	current flow	Drain current flows on application of drain to source voltage, at $V_{GS}=0$	Practically no current flows on application of drain to source at $V_{GS}=0$. current flows only when V_{GS} is above threshold level

comparison between N-channel and p-channel MOSFET

S.NO	N-channel MOSFET	P-channel MOSFET
1.	It is costlier and some what difficult to produce than P-channel MOSFET	P-channel enhancement MOSFET is easier and cheaper to produce than N-channel MOSFET
2.	since the hole mobility is nearly 2.5 times lower than the electron mobility, n-channel MOSFET occupy less area than p-channel MOSFET for same I_D rating	It occupies larger area than N-channel MOSFET for same I_D rating
3.	Drain resistance is lower than the identical p-channel MOSFET	Drain resistance is three times higher than that of identical N-channel MOSFET
4.	It has higher packing density. Twice packaging density than P-channel MOSFET	Lower packaging density than N-channel MOSFETs
5.	Almost three times faster than P-channel MOSFET in switching applications	It is slower than N-channel MOSFET
6.	Because of positively charged contaminants, the N-channel MOSFET may turn on prematurely	It is not turn-ON prematurely

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TRANSISTOR BIASING AND THERMAL STABLIZATION [BJT]

What is Transistor Biasing?

* Transistor Biasing is the process of setting a transistor DC operating voltage & current conditions to the correct level so that any AC input signal can be amplified correctly by the transistor.

NEED FOR BIASING:

* The basic functionality of transistor is for Amplification purpose.
* When the weak signal is applied to the base of a transistor, then transistor has to strengthen that signal which is appeared at the output circuit.
* During Amplification only magnitude of signal should increase and there should be no change in the signal shape.
* The process of raising the strength of a weak signal without any change in its shape is known as Faithful Amplification.

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For proper amplification, following conditions must be satisfied,

1) The emitter-base function should be forward-biased
2) The collector-base function must be reverse biased
3) There should be proper zero Signal collector current.

* Zero Signal collector current is the collector current that is known there is no input signal to a transistor.
* Ideally, there should be no collector current in this situation but, in practice, there is some current even when there is no input because of reverse-biased collector base junction that provides reverse saturation current.

* The proper flow of zero signal coll. collector current and the maintenance of proper collector-emitter voltage during the transmission of signal is known as "Transistor Biasing".

OPERATING POINT:

* In order to produce distortion-free output in amplifier circuits, the supply voltages and resistances in the circuit must be suitably chosen.
* These voltages and circuits resistances establish a set of dc voltage V_{CEQ} and current I_{CQ} to operate the transistor in Active region.

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Definition - The Specific point where dc voltage V_{CE} and current I_{CQ} is obtained to operate the transistor in active region is called operating point or Quiescent point or Q-point.

* The biasing process is to provide proper supply voltages, resistances for obtaining the desired Q-point.

* The Q-point specifies the collector current I_C and collector to emitter voltage V_{CE} that exist when no input signal is applied.

TRANSISTOR LOAD LINE ANALYSIS:

* The load line analysis of transistor means for the given value of collector-emitter voltage, we find the value of collector current.

* This can be done by plotting the output characteristics and then determine the collector current I_C with respect to collector-emitter voltage V_{CE}.

* Load line analysis can be done in two ways,

1. DC load line
2. AC load line.

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DC LOAD LINE:

Definition: The load line which is drawn on the characteristic curve when no signal is given to the input is called as DC load line.

* The DC load line represents the derivable combinations of the collector current and the collector - emitter voltage.

* Consider the fixed bias circuit as shown below.

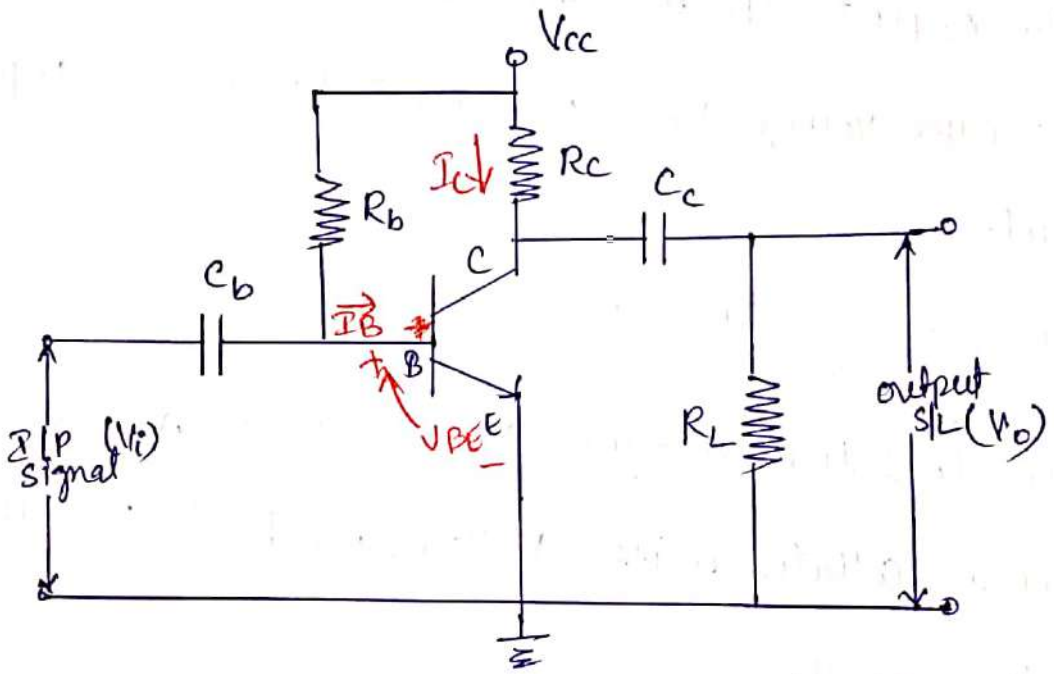

FIG: FIXED-BIAS CIRCUIT

* Apply KVL to the output circuit

$$V_{cc} = I_C R_C + V_{CE} \rightarrow (1)$$

$$V_{CE} = V_{cc} - I_C R_C$$

* The collector - emitter voltage is maximum when the collector current $I_C = 0$ then

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then $V_{CE} = V_{cc} - (0) \times R_c$

$\boxed{V_{CE} = V_{cc}}$ → This is the first point

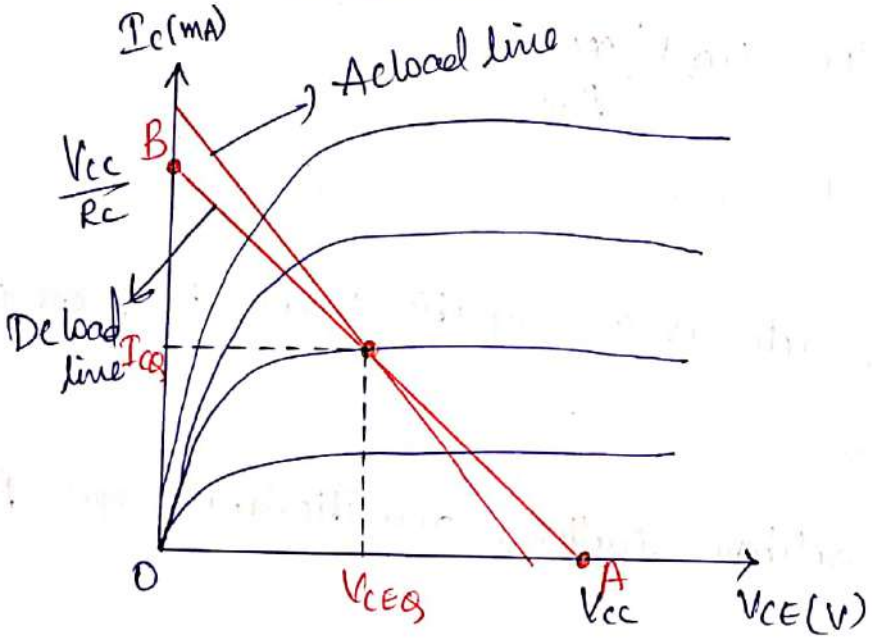
* The collector current I_c becomes maximum when the collector emitter voltage $V_{CE} = 0$ then,

$$V_{CE} = V_{cc} - I_c R_c$$

$$0 = V_{cc} - I_c R_c$$

$$I_c R_c = V_{cc}$$

$\boxed{I_c = \frac{V_{cc}}{R_c}}$ → This is the second point.



point A is $(V_{cc}, 0)$ ∴ Co-ordinates are (V_{CE}, I_c)

point B is $(0, \frac{V_{cc}}{R_c})$

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AC LOAD LINE:

* When an AC signal is applied to an amplifier, the Q-point moves up and down.
* The line along which the Q-point moves up and down is known as AC load line.
* The AC load line Intersects DC load line at point 'Q'.
* To draw the ac load line V_{CE} maximum and I_C maximum are required.

$$V_{CE} = V_{CEQ} + I_{CQ} R_{ac} \qquad [\because R_{ac} = R_c || R_L]$$

$$I_C = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$$

How to choose the operating on the DC-load line?

* The transistor acts as an amplifier when it is operated in Active Region.
* In order to achieve faithful amplification proper point is required.
* The following cases describes how to choose the operating point.

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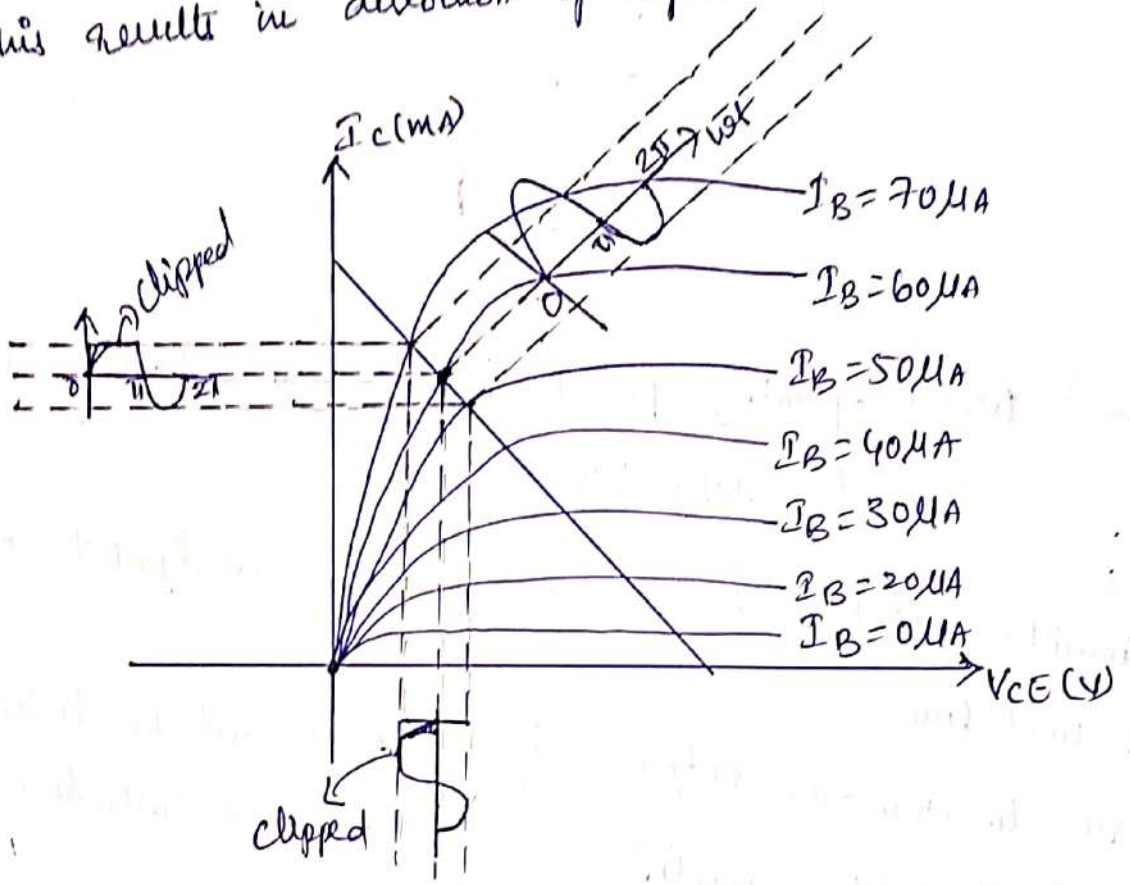
CASE:1 When operating point is near the Saturation Region

* Consider point A which is very near to the Saturation Region, even though the base current is varying sinusoidally, the output voltage and current is clipped at positive peaks.
* This results in distortion of signal.



CASE:2 When operating point is near the cut-off Region

* Consider point P which is very near to the cut-off Region. The output signal is clipped at the negative peak.
* Hence this point is also not an operating point.

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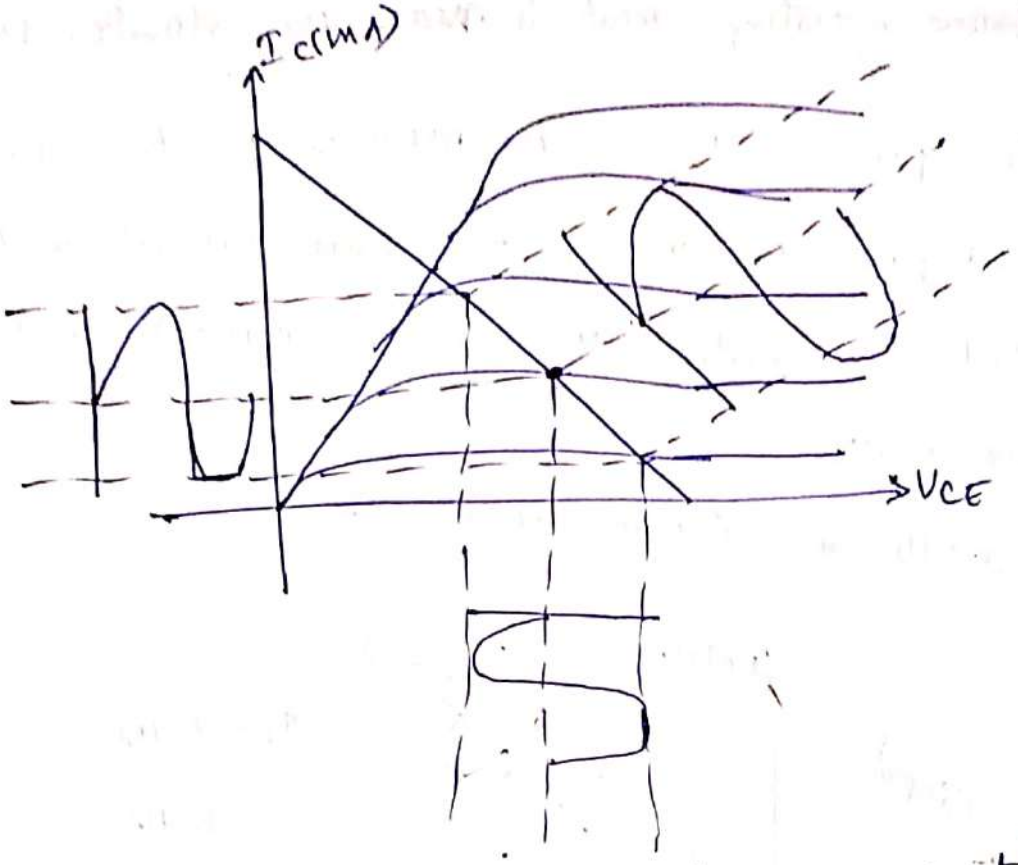
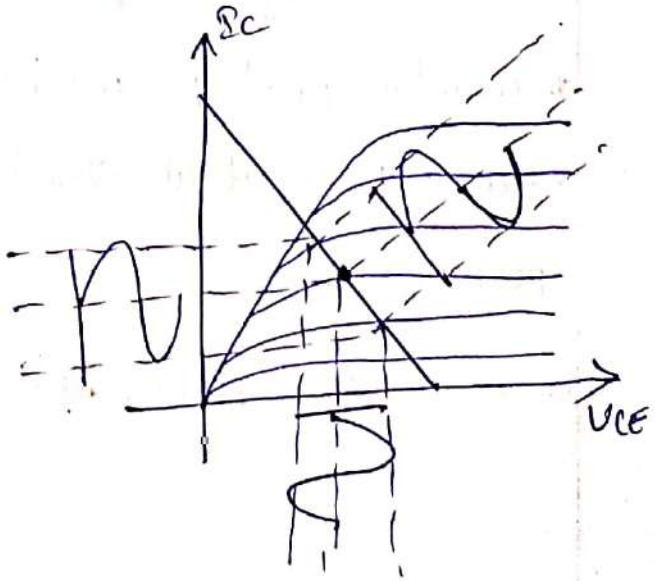


CASE: 3 When operating point is at the center of the Active Region.

* Consider point Q which is at the midpoint of DC-load line.
* Due to this the output signal will not be distorted.
* A good amplifier amplifies signals without introducing distortion.
* So operating point is always choosen at the midpoint of dc load line.



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* Therefore to stabilise the Q-point, I_C should be constant. 5

2. INDIVIDUAL VARIATIONS:

* The value of β (Current gain) and Base to emitter Voltage V_{BE} are not similar for any two transistors

($\because V_\gamma = 0.3\,V$ for Ge and $V_\gamma = 0.7$ for Si)

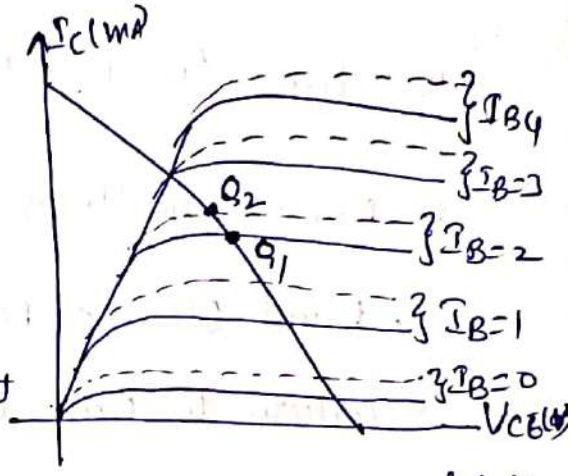

Fig: Collector characteristics for two same type of transistors

* The figure shows the collector characteristics of two transistors of same type. Even though the base current I_B is maintained as constant, 'β' is different.

* Due to this the Q-point changes from Q_1 to Q_2 because of this amplification is unfaithful.

* Therefore, even I_B is constant, the operating point is not stable. So I_B should be allowed to change so as to maintain I_C and V_{CE} as constant as 'β' changes.

* So, the main problem which affects the operating point is temperature.

* Hence operating point should be made independent of the temperature so as to achieve stability.

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BJT BIASING METHODS:

* For the transistor to act as an amplifier it must be operated in active region.
* The method of applying external voltages to operate the transistor in active region is known as Biasing.

* Biasing methods are
  1. Fixed Bias (or) Base Resistor method.
  2. Collector to Base bias (or) Collector feedback bias.
  3. Self bias (or) Emitter bias (or) Voltage-divider bias

FACTORS AFFECTING THE OPERATING POINT:

* The main factor that affect the operating point is the temperature.
* The operating shifts due to change in temperature.
* This leads to unfaithful amplification.

1. Temperature Dependence of I_C:

* The collector current is given by $I_C = \beta I_B + (1+\beta) I_{CBO}$
* As temperature increases the values of β, V_{BE}, I_{CBO} gets affected.
* I_{CBO} gets doubled for every 10°c rise in temperature
* V_{BE} decreases by 2.5mV for every 1° rise in temperature.

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STABILIZATION:

* The process of making the operating point independent of temperature changes & variations in transistor parameters is known as "Stabilization".

* Due to this the biasing circuit should be stablized.

* There are two methods to stabilize the Q-point.

1) Stabilization techniques

2) Compensation techniques.

Stabilization techniques: In this technique, resistive biasing circuits are used to vary I_B. By varying I_B the collector current I_c is maintained as constant.

Compensation techniques: In this technique, sensitive devices like diodes, transistors, thermistors are used to keep operating point as constant.

* To measure the stability of a biasing circuits, Stability factors are defined.

* There 3 Stability factor parameters (S, S', S'').

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1. STABILITY FACTOR (S):

Definition: The Ratio of change in collector current (I_C) with respect to collector-base leakage current (I_{CO}) at constant values of V_{BE} and β is called as stability factor 'S'.

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{\Delta I_C}{\Delta I_{CO}} \Big|_{V_{BE}/\beta \text{ are constant.}}$$

$$I_C = \beta I_B + (1+\beta) I_{CO} \rightarrow (1)$$

differentiate eq(1) w.r.t I_C

$$\frac{\partial}{\partial I_C}(I_C) = \beta \cdot \frac{\partial I_B}{\partial I_C} + (1+\beta)\frac{\partial (I_{CO})}{\partial I_C}$$

$$1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta)\left(\frac{1}{S}\right) \qquad \left(\because S = \frac{\partial I_C}{\partial I_{CO}}\right)$$

$$(1+\beta)\frac{1}{S} = 1 - \beta \cdot \frac{\partial I_B}{\partial I_C}$$

$$\frac{1}{S} = \frac{1 - \beta \cdot \frac{\partial I_B}{\partial I_C}}{1+\beta}$$

$$\boxed{S = \frac{1+\beta}{1 - \beta \cdot \frac{\partial I_B}{\partial I_C}}}$$

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2. STABILITY FACTOR (S'):

Definition: The rate of change of collector current I_C with respect to V_{BE} at constant I_{CO} and β is called as stability factor S'.

$$S' = \frac{\partial I_C}{\partial V_{BE}} = \frac{\Delta I_C}{\Delta V_{BE}} \Big|_{I_{CO}, \beta \text{ constant}}$$

3. STABILITY FACTOR (S''):

Definition: The rate of change of collector current I_C with respect to β at constant values of I_{CO} & V_{BE} is called as stability factor S''.

$$S'' = \frac{\partial I_C}{\partial \beta} = \frac{\Delta I_C}{\Delta \beta} \Big|_{I_{CO}, V_{BE} \text{ constant}}$$

* The stability factors S, S', S'' determines the stability of a circuit. If the values S, S', S'' are large, the circuit is highly unstable else the circuit is highly stable.

* To determine the operating point,

1. Find the I_{CQ}
2. Find V_{CEQ}

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BIASING TECHNIQUES :

1. FIXED BIAS (OR) BASE RESISTOR BIAS:

* The Circuit for Fixed bias Circuit is as shown below.

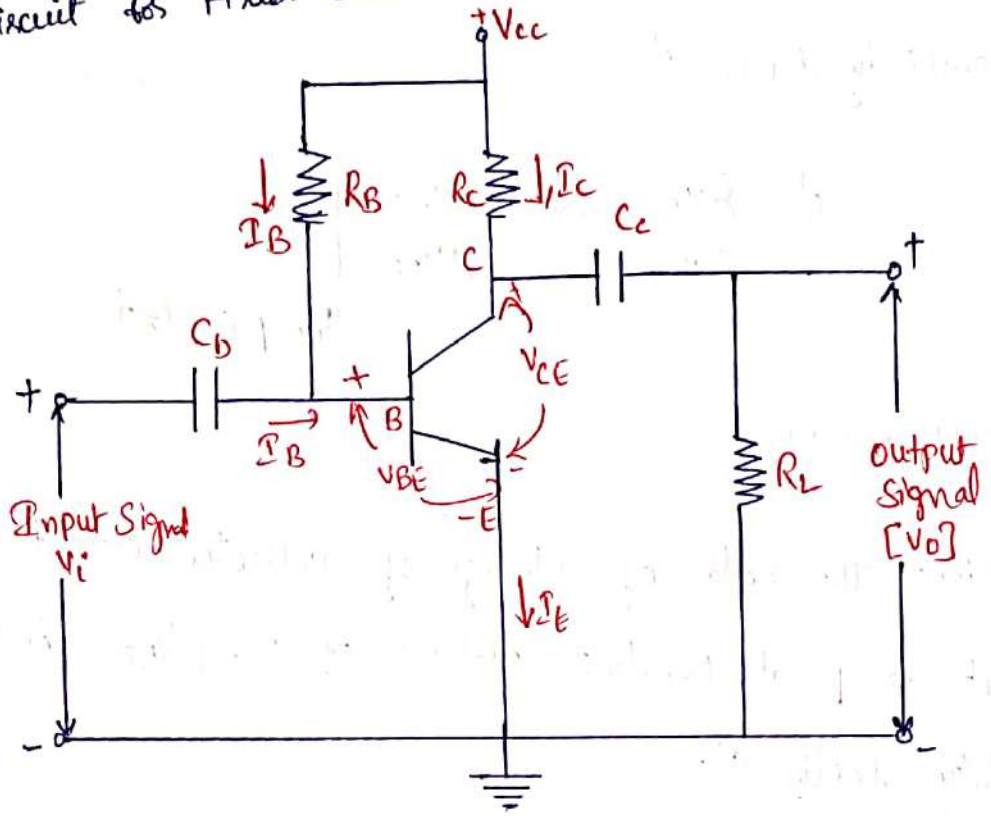

FIG: FIXED BIAS CIRCUIT.

* Consider a fixed bias circuit as shown above, Here the Resistor RB provides fixed bias voltage to the base.

Let C_b = Base Capacitor

C_c = Collector Capacitor

R_B = Base resistor

R_L = Load Resistor

R_c = Collector Resistor

V_i = I/p Signal

V_o = o/p Signal

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* In this method a high resistance R_B is connected between positive terminal of supply voltage V_{cc} and base of transistor.

* Here, the required zero signal base current (I_{CBO}) flows through R_B which is provided by V_{cc}.

* From figure, the base to emitter junction (V_{BE}) is forward biased, because the base is positive with respect to emitter.

* Hence by proper selection of R_B, the required zero signal base current ($I_C = \beta I_B$) can be made to flow.

DC ANALYSIS:

* The DC equivalent circuit for biasing circuits is obtained by eliminating Ac components and Ac supply i/p i.e., Capacitors & i/p.

* Then the fixed bias circuit will be as shown,

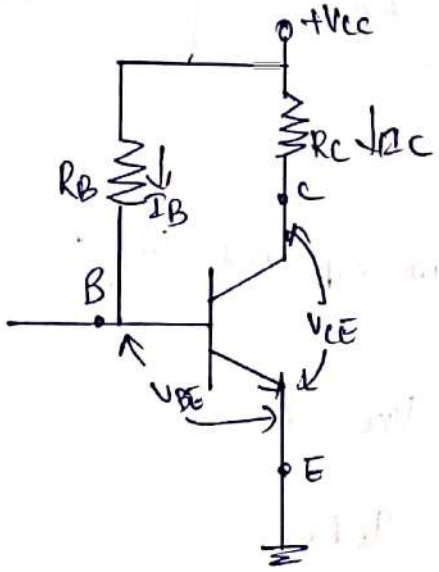

FIG: DC EQUIVALENT CIRCUIT FOR FIXED BIAS.

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To obtain I_{CQ} :

Apply KVL to Input Side, we get

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$V_{CC} = I_B R_B - V_{BE}$$

$$I_B R_B = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \rightarrow (1)$$

We know that $I_C = \beta I_B \rightarrow (2)$

Substitute eq (1) in eq (2)

$$I_C = \beta \left[\frac{V_{CC} - V_{BE}}{R_B} \right]$$

$$\therefore I_{CQ} = \frac{\beta (V_{CC} - V_{BE})}{R_B}$$

To obtain V_{CEQ} :

Apply KVL to the o/p side, we get

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C$$

$$\therefore V_{CEQ} = V_{CC} - I_C R_C$$

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STABILITY FACTOR(S) :-

We know that $I_c = \beta I_B + (1+\beta) I_{CO} \rightarrow (3)$

differentiate eq (3) with respect to I_c

$$\frac{d}{dI_C}(I_c) = \beta \cdot \frac{d}{dI_C}(I_B) + (1+\beta)\frac{d}{dI_C}(I_{CO})$$

Here I_B is independent of I_C $\left(\frac{dI_B}{dI_C} = 0\right)$

$$1 = \beta(0) + (1+\beta)\cdot\frac{dI_{CO}}{dI_C} \qquad \left[\because \frac{d}{da}(x) = 1\right]$$

$$1 = 0 + (1+\beta)\cdot\frac{dI_{CO}}{dI_C}$$

$$\frac{dI_{CO}}{dI_C} = \frac{1}{1+\beta}$$

$$\frac{1}{S} = \frac{1}{1+\beta} \qquad \left(\because S = \frac{dI_c}{dI_{CO}}\right.$$

$$\boxed{S = 1+\beta}$$

* If $\beta = 100$ then $S = 101$. This shows that I_c changes 101 times as much as any changes in I_{CO}.
* This increase in current causes thermal runaway and thus transistor damages.
* Here Stability factor is high so that Q-point is more unstable.

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STABILITY FACTOR (S):

We know that $I_C = \beta I_B + (1+\beta) I_{CO} \rightarrow (1)$

From eq (1) $I_B = \dfrac{V_{CC} - V_{BE}}{R_B} \rightarrow (2)$

Sub eq (2) in eq (1)

$$I_C = \beta\left[\frac{V_{CC} - V_{BE}}{R_B}\right] + (1+\beta) I_{CO}$$

$$I_C = \frac{\beta V_{CC}}{R_B} - \frac{\beta V_{BE}}{R_B} + (1+\beta) I_{CO} \rightarrow (3)$$

differentiate eq (3) w.r.t I_C

$$\frac{d}{dI_C}(I_C) = \frac{\beta}{R_B}\frac{d}{dI_C}(V_{CC}) - \frac{\beta}{R_B}\frac{d}{dI_C}(V_{BE}) + 1+\beta \cdot \frac{d}{dI_C}(I_{CO})$$

$$1 = 0 - \frac{\beta}{R_B}\frac{dV_{BE}}{dI_C} + (1+\beta)(0)$$

$\left[\because S' = \dfrac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\beta \text{ (constant)}}$

$$1 = -\frac{\beta}{R_B}\frac{dV_{BE}}{dI_C}$$

$$\frac{dV_{BE}}{dI_C} = -\frac{R_B}{\beta}$$

$$\frac{dI_C}{dV_{BE}} = -\frac{\beta}{R_B}$$

$$\boxed{S' = -\frac{\beta}{R_B}}$$

Stability factor (S'')

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

differentiate w.r.t β

$$\frac{dI_C}{d\beta} = I_B \cdot \frac{d}{d\beta}(\beta) + \frac{d}{d\beta}\left[(1+\beta) I_{CO}\right]$$

$$\frac{dI_C}{d\beta} = I_B + \frac{d}{d\beta}\left[I_{CO} + \beta I_{CO}\right]$$

$$\frac{dI_C}{d\beta} = I_B + I_{CO} \qquad \left(\because I_C = \beta I_B,\ I_B = \frac{I_C}{\beta}\right.$$

$\left.I_{CO}$ is negligible I_{CO} is very

$$\frac{dI_C}{d\beta} = \frac{I_C}{\beta} \qquad \therefore \boxed{S'' = I_C/\beta}$$

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ADVANTAGES :

1. This is a simple circuit with less number of components.
2. The operating point can be fixed anywhere in the active Region of the characteristics by simply changing the values of R_B. Thus it provides the maximum flexibility in design.

DISADVANTAGES:

1. operating point depends on temperature.
2. When the transistor is replaced by another with different value of β, the operating point shifts.

2. COLLECTOR TO BASE BIAS (OR) BIASING WITH FEEDBACK RESISTOR:

* A CE amplifier using collector to base bias circuit is as shown below

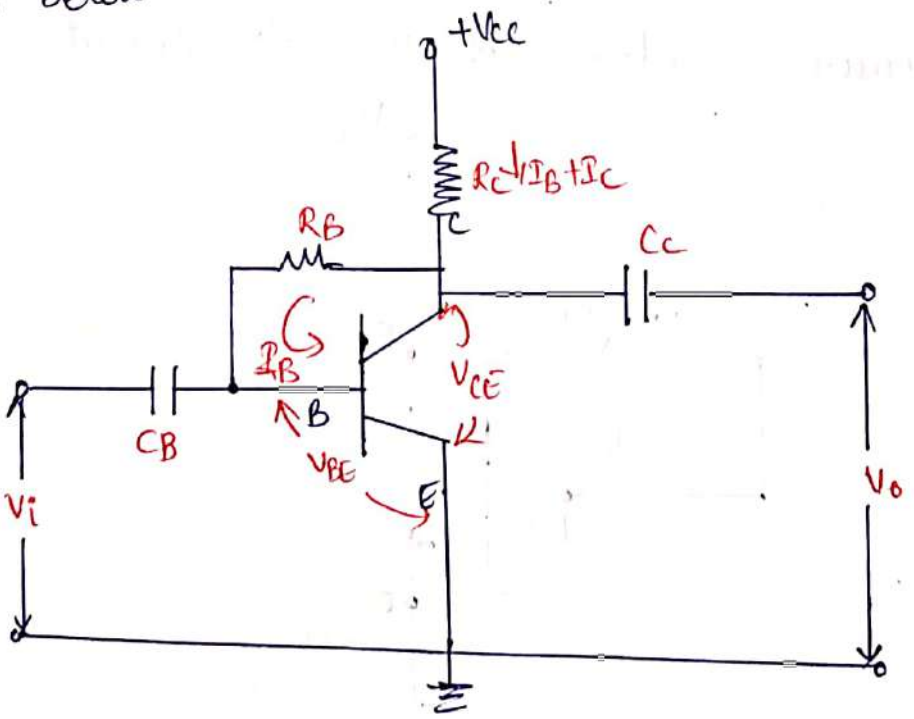

FIG: COLLECTOR TO BASE BIAS CIRCUIT

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* In this method, the biasing circuit resistor is connected in between the collector and the base of the transistor.

* The biasing Resistor R_B provides more stability.

* If the collector current I_C tends to increase due to either increase in temperature & the transistor is replaced with a higher β.

* Due to this, voltage drop across R_C increases as a result V_{CE} and I_B reduces. This decrease in I_B controls I_C.

* Thus greater stability is obtained. So the Collector to base bias circuit is more stable compared to fixed bias circuit.

DC ANALYSIS:

* To obtain DC equivalent circuit the ac components and supply sources are eliminated then the circuit will be as follows.

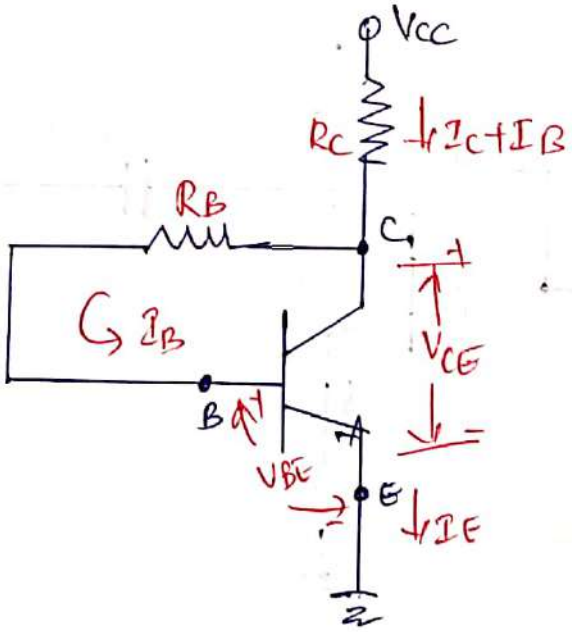

FIG: DC EQUIVALENT CIRCUIT

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$$\therefore I_{CQ} = \frac{\beta(V_{CC} - V_{BE})}{(1+\beta)R_C + R_B}$$

To obtain V_{CEQ} :

Apply KVL to the output circuit.

$$V_{CC} - (I_C + I_B)R_C - V_{CE} = 0$$

$$V_{CC} - I_C R_C - I_B R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - (I_C + I_B)R_C$$

$$\therefore V_{CEQ} = V_{CC} - (I_C + I_B)R_C$$

STABILITY FACTOR(S):

* The stability factor S, is given by $S = \frac{1+\beta}{1-\beta\left[\frac{dI_B}{dI_C}\right]}$ → (1)

$$V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} = 0$$

$$V_{CC} = I_C R_C + I_B R_C + I_B R_B + V_{BE}$$

$$V_{CC} = I_C R_C + I_B(R_C + R_B) + V_{BE}$$

Differentiate above equation with respect to I_C

$$\frac{d}{dI_C}(V_{CC}) = \frac{d}{dI_C}(I_C R_C) + \frac{d}{dI_C}(I_B(R_C + R_B)) + \frac{d}{dI_C}(V_{BE})$$

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To obtain I_{CQ} :

Apply KVL to the i/p circuit

$$V_{CC} - (I_B + I_C) R_C + I_B R_B - V_{BE} = 0$$

$$V_{CC} = (I_B + I_C) R_C + I_B R_B + V_{BE}$$

$$V_{CC} = I_B R_C + I_C R_C + I_B R_B + V_{BE}$$

$$V_{CC} - I_C R_C - V_{BE} = I_B R_C + I_B R_B$$

$$I_B (R_C + R_B) = V_{CC} - I_C R_C - V_{BE}$$

$$I_B = \frac{V_{CC} - I_C R_C - V_{BE}}{R_C + R_B}$$

$$I_B (R_C + R_B) = V_{CC} - (\beta I_B) R_C - V_{BE} \qquad (\because I_C = \beta I_B)$$

$$I_B (R_C + R_B) + \beta I_B R_C = V_{CC} - V_{BE}$$

$$I_B (R_C + R_B + \beta R_C) = V_{CC} - V_{BE}$$

$$I_B (R_B + (1+\beta) R_C) = V_{CC} - V_{BE}$$

$$I_B = \frac{V_{CC} - V_{BE}}{(1+\beta) R_C + R_B} \Rightarrow$$

$\therefore I_C = \beta I_B$

Sub I_B in above equation

$$I_C = \frac{\beta (V_{CC} - V_{BE})}{(1+\beta) R_C + R_B}$$

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STABILITY FACTOR (S'):

The Stability factor $S' = \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO}/\beta \text{ Constant}}$

We know that $I_{C_B} = \frac{\beta(V_{CC} - V_{BE} - I_C R_C)}{R_C + R_B}$

$$I_C = \frac{\beta V_{CC}}{R_C + R_B} - \frac{\beta V_{BE}}{R_C + R_B} - \frac{\beta I_C R_C}{R_C + R_B}$$

differentiating above equation w.r.t I_C

$$\frac{d}{dI_C}(I_C) = \frac{\beta}{R_C + R_B}\frac{d}{dI_C}(V_{CC}) - \frac{\beta}{R_C + R_B}\frac{d}{dI_C}(V_{BE}) - \frac{\beta R_C}{R_C + R_B}\frac{d}{dI_C}(I_C)$$

$$1 = 0 - \frac{\beta}{R_C + R_B}\frac{dV_{BE}}{dI_C} - \frac{\beta R_C}{R_C + R_B}$$

$$\frac{-\beta}{R_C + R_B}\frac{dV_{BE}}{dI_C} = 1 + \frac{\beta R_C}{R_C + R_B}$$

$$\frac{dV_{BE}}{dI_C} = -\left[1 + \frac{\beta R_C}{R_C + R_B}\right]\frac{R_C + R_B}{\beta}$$

$$\frac{dV_{BE}}{dI_C} = -\left[\frac{R_C + R_B + \beta R_C}{R_C + R_B}\right]\frac{(R_C + R_B)}{\beta}$$

$$\frac{dV_{BE}}{dI_C} = -\left[\frac{(1+\beta)R_C + R_B}{\beta}\right]$$

$$\frac{dI_C}{dV_{BE}} = \frac{-\beta}{(1+\beta)R_C + R_B}$$

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$$0 = 1 \cdot R_C + \frac{dI_B}{dI_C}(R_C + R_B) + 0$$

$$0 = R_C + \frac{dI_B}{dI_C}(R_C + R_B)$$

$$(R_C + R_B)\frac{dI_B}{dI_C} = -R_C$$

$$\frac{dI_B}{dI_C} = \frac{-R_C}{R_C + R_B}$$

Sub $\frac{dI_B}{dI_C}$ value in eq (1)

$$S = \frac{1+\beta}{1-\beta\left[\frac{-R_C}{R_C+R_B}\right]}$$

$$\boxed{S = \frac{1+\beta}{1+\beta\left[\frac{R_C}{R_C+R_B}\right]}}$$

* Here the Stability factor S can be small by making R_C as large & R_B as small.

* Hence here the Stability factor is smaller than the value obtained by fixed bias circuit.

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$$S = \frac{-\beta}{R_B + (R_C + R_B)}$$

$$\boxed{S' = \frac{-\beta}{R_B + (1+\beta)R_C}}$$

STABILITY FACTOR (S'') :

* The Stability factor $S'' = \left.\frac{dI_C}{d\beta}\right|_{I_{CO}, V_{BE}}$ are constant

$$I_{CQ} = \frac{\beta[V_{CC} - V_{BE} - I_C R_C]}{R_C + R_B}$$

different

$$I_{CQ} = \frac{\beta V_{CC}}{R_C + R_B} - \frac{\beta V_{BE}}{R_C + R_B} - \frac{\beta I_C R_C}{R_C + R_B}$$

differentiate above equation with respect to β.

$$\frac{\partial I_{CQ}}{\partial \beta} = \frac{V_{CC}}{R_C + R_B}\frac{\partial}{\partial \beta}(\beta) - \frac{\partial}{\partial \beta}(\beta)\frac{V_{BE}}{R_C + R_B} - \frac{\partial}{\partial \beta}(\beta I_C)\frac{R_C}{R_C + R_B}$$

$$\frac{\partial I_C}{\partial \beta} = \frac{V_{CC}}{R_C + R_B} - \frac{V_{BE}}{R_C + R_B} - \frac{R_C}{R_C + R_B}\left[\frac{\partial}{\partial \beta}(\beta) I_C + \beta \cdot \frac{\partial I_C}{\partial \beta}\right]$$

$$\left[\because UV = u \cdot \frac{dv}{dx} + v \cdot \frac{du}{dx}\right)$$

$$\frac{\partial I_C}{\partial \beta} = \frac{V_{CC}}{R_C + R_B} - \frac{V_{BE}}{R_C + R_B} - \frac{R_C}{R_C + R_B} \cdot I_C + \frac{\beta \cdot R_C}{R_C + R_B} \cdot \frac{\partial I_C}{\partial \beta}$$

$$\frac{\partial I_C}{\partial \beta} + \frac{\beta \cdot R_C}{R_C + R_B} \cdot \frac{\partial I_C}{\partial \beta} = \frac{V_{CC} - V_{BE} - R_C I_C}{R_C + R_B}$$

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$$\frac{\partial I_C}{\partial \beta}\left(1+\frac{\beta R_C}{R_C+R_B}\right) = \frac{V_{CC}-V_{BE}-I_C R_C}{R_C+R_B}$$

$$\frac{\partial I_C}{\partial \beta}\left(\frac{R_C+R_B+\beta R_C}{R_C+R_B}\right) = \frac{V_{CC}-V_{BE}-I_C R_C}{R_C+R_B}$$

$$\frac{\partial I_C}{\partial \beta}\{(1+\beta)R_C+R_B) = V_{CC}-V_{BE}-I_C R_C$$

$$\frac{\partial I_C}{\partial \beta} = \frac{V_{CC}-V_{BE}-I_C R_C}{(1+\beta)R_C+R_B}$$

$$\therefore S'' = \frac{V_{CC}-V_{BE}-I_C R_C}{(1+\beta)R_C+R_B}$$

ADVANTAGES:

1. The collector current becomes independent of β when $\beta R_C >> R_B$.
2. The feedback from collector to base via R_B increases the stability of the circuit.
3. The gain of amplifier due to feedback is smaller than without feedback.

* If R_C is small, stablization does not improve over that fixed bias circuit.

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* Due to decrease in V_{BE}, the base current I_B and collector current I_C reduces.

* Therefore we can say that the collector current I_C reduces and negative feed back exists in the emitter bias circuit.

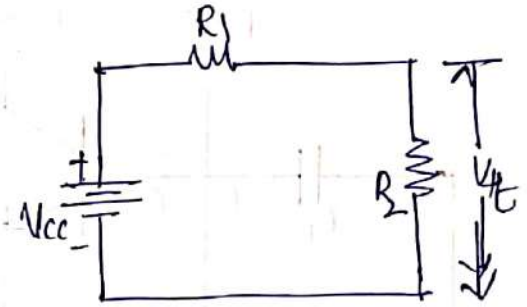
DC Analysis

* The Input circuit can be redrawn as thevenins equivalent circuit.

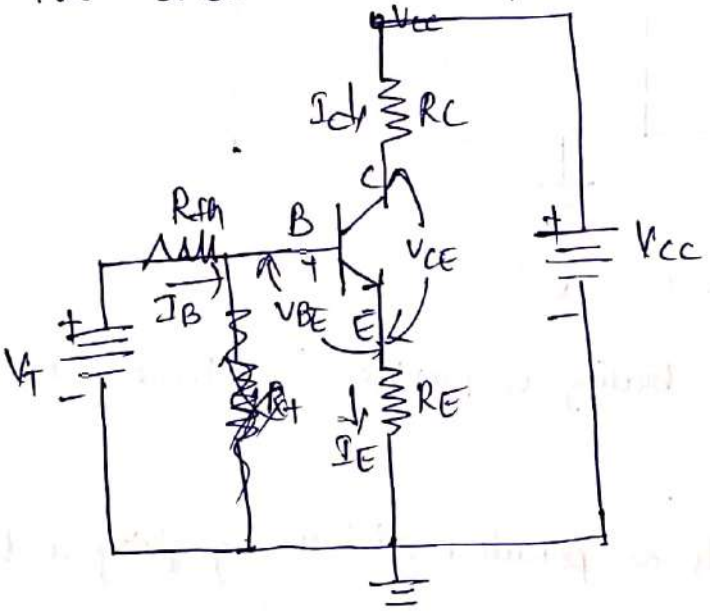
$$R_{th} = R_1 \| R_2$$

$$V_T = V_{R_2}$$

$$= \frac{V_{CC} R_2}{R_1 + R_2}$$



then the circuit will be,



Apply KVL to the i/p circuit:

$$V_T = I_B \cdot R_{th} + V_{BE} + I_E R_E$$

$$V_T = I_B R_{th} + V_{BE} + (I_C + I_B) R_E \quad (\because I_E = I_B + I_C)$$

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VOLTAGE DIVIDER BIAS (OR) EMITTER BIAS:

* It is the simple circuit which maintains the operating point stable.
* The self bias also called as Emitter bias (or) emitter resistor and potential divider circuit.
* The below figure shows the Voltage divider bias circuit.

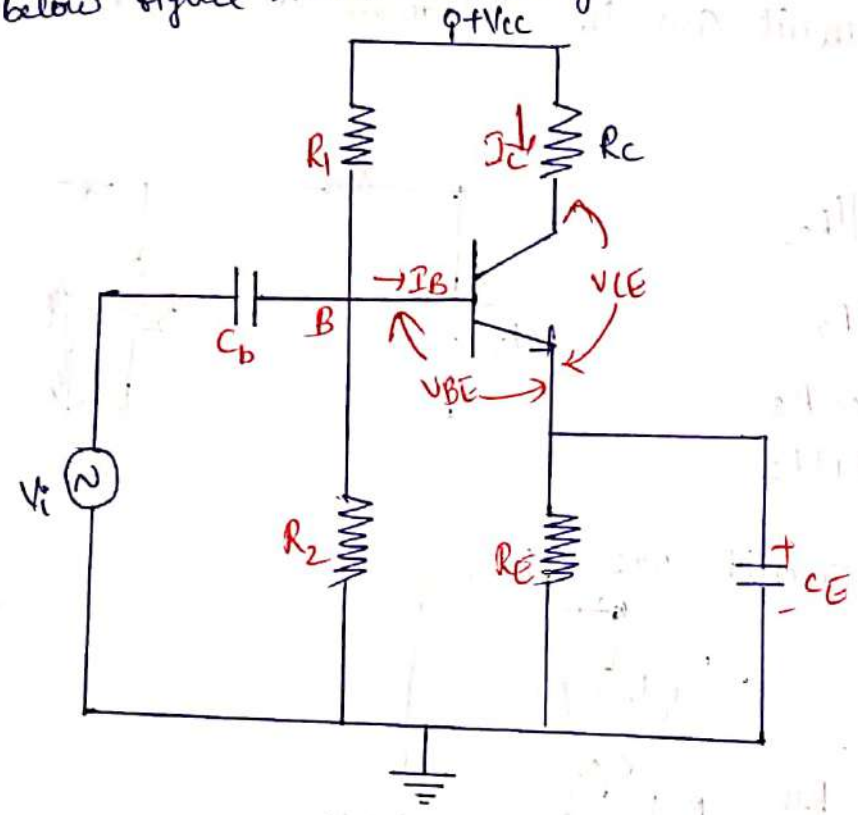

FIG: VOLTAGE DIVIDER BIAS CIRCUIT

* In this method, the biasing is provided by three resistors R_1 R_2 & R_E.
* The Resistor R_1 & R_2 acts as potential divider by giving a fixed voltage to base.
* The collector current increases due to change in temperature (or) β, the emitter current I_E also increases and the voltage drop across R_E increases which reduces V_{BE}.

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STABILITY FACTOR(S):

The stability factor $S = \dfrac{1+\beta}{1-\beta\left[\frac{dI_B}{dI_C}\right]}$ → (1)

$$V_T = I_B[R_{th}+R_E] + I_C R_E$$

differentiate above equation w.r.t I_C

$$\frac{d}{dI_C}(V_T) = \frac{d}{dI_C}[I_B](R_{th}+R_E) + \frac{d}{dI_C}(I_C R_E)$$

$$0 = \frac{dI_B}{dI_C}(R_{th}+R_E) + R_E$$

$$\frac{dI_B}{dI_C}(R_{th}+R_E) = -R_E$$

$$\frac{dI_B}{dI_C} = \frac{-R_E}{R_{th}+R_E} \rightarrow (2)$$

Substitute eq (2) in eq (1)

$$S = \frac{1+\beta}{1-\beta\left[\frac{-R_E}{R_{th}+R_E}\right]}$$

$$S = \frac{1+\beta}{1+\beta\frac{R_E}{R_{th}+R_E}}$$

$$S = \frac{1+\beta}{\frac{R_{th}+R_E+\beta R_E}{R_{th}+R_E}}$$

$$S = \frac{(1+\beta)(R_{th}+R_E)}{R_{th}+(1+\beta)R_E}$$

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$$V_T = I_B R_{th} + V_{BE} + I_C R_E + I_B R_E$$

$$V_T = I_B [R_{th} + R_E] + V_{BE} + I_C R_E$$

$$V_T - V_{BE} = I_B [R_{th} + R_E] + I_C R_E$$

$$V_T - V_{BE} = I_B [R_{th} + R_E] + \beta I_B R_E \qquad (\because I_C = \beta I_B)$$

$$V_T - V_{BE} = I_B [R_{th} + R_E + \beta R_E]$$

$$V_T - V_{BE} = I_B [R_{th} + (1+\beta) R_E]$$

$$I_B = \frac{V_T - V_{BE}}{R_{th} + (1+\beta) R_E}$$

$\because I_C = \beta I_B$

$$\boxed{I_{C_Q} = \frac{\beta (V_T - V_{BE})}{R_{th} + (1+\beta) R_E}}$$

Apply KVL to o/p circuit

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\boxed{V_{CE_Q} = V_{CC} - I_C R_C - I_E R_E}$$

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$$S = \frac{(1+\beta)\left(1+\frac{R_{th}}{R_E}\right)}{}$$

Divide numerator and denominator w.r.t R_E

$$S = \frac{(1+\beta)(R_{th}+R_E)/R_E}{R_{th}+(1+\beta)R_E/R_E}$$

$$S = \frac{(1+\beta)\left(\frac{R_{th}}{R_E}+\frac{R_E}{R_E}\right)}{\frac{R_{th}}{R_E}+\frac{(1+\beta)R_E}{R_E}}$$

$$S = \frac{(1+\beta)\left(1+\frac{R_{th}}{R_E}\right)}{(1+\beta)+\frac{R_{th}}{R_E}}$$

If $\frac{R_{th}}{R_E} << 1$

$$S = \frac{1+\beta}{1+\beta}$$

$$\boxed{S = 1}$$

* stability factor 'S' for voltage divider (&) self bias is less when compared to other biasing circuit.

* So voltage divider bias is most commonly used biasing circuit.

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STABILITY FACTOR (S') :-

$$V_T = I_B \cdot R_{th} + V_{BE} + I_E R_E \qquad (\because I_E = I_B + I_C)$$

$$V_T = I_B \cdot R_{th} + V_{BE} + (I_C + I_B) R_E$$

$$V_T = \frac{I_C}{\beta} \cdot R_{th} + V_{BE} + \left(I_C + \frac{I_C}{\beta}\right) R_E \qquad \left(\because I_C = \beta I_B,\ I_B = \frac{I_C}{\beta}\right)$$

Differentiate above eq w.r.t V_{BE}

$$\frac{\partial}{\partial V_{BE}}(V_T) = \frac{\partial}{\partial V_{BE}}\left(\frac{I_C}{\beta}\right) R_{th} + \frac{\partial V_{BE}}{\partial V_{BE}} + \frac{\partial}{\partial V_{BE}}\left(I_C + \frac{I_C}{\beta}\right) R_E$$

$$0 = \frac{\partial I_C}{\partial V_{BE}} \times \frac{R_{th}}{\beta} + 1 + \frac{\partial I_C}{\partial V_{BE}} \times R_E + \frac{\partial I_C}{\partial V_{BE}} \times \frac{R_E}{\beta}$$

$$0 = \frac{\partial I_C}{\partial V_{BE}}\left[\frac{R_{th}}{\beta} + R_E + \frac{R_E}{\beta}\right) + 1$$

$$\frac{\partial I_C}{\partial V_{BE}}\left[\frac{R_{th}}{\beta} + \frac{R_E}{\beta} + R_E\right) = -1$$

$$S'\left[\frac{R_{th} + R_E + \beta R_E}{\beta}\right] = -1$$

$$S'\left[\frac{R_{th} + (1+\beta) R_E}{\beta}\right] = -1$$

$$\boxed{S' = \frac{-\beta}{R_{th} + (1+\beta) R_E}}$$

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STABILITY FACTOR (S'') :

$$V_T = I_B R_{th} + V_{BE} + (I_C + I_B) R_E$$

$$V_T = I_B R_{th}$$

differentiating above equation w.r.t β

$$\frac{d}{d\beta}(V_T) = \frac{d}{d\beta}(I_B) R_{th} + \frac{d}{d\beta}(V_{BE}) + \frac{d}{d\beta}(I_C + I_B) R_E$$

$$0 = \frac{dI_B}{d\beta} R_{th} + 0 + \frac{dI_C}{d\beta} R_E + \frac{dI_B}{d\beta} R_E$$

$$0 = \frac{d}{d\beta}\left(\frac{I_C}{\beta}\right) R_{th} + 0 + \frac{d}{d\beta}(I_C) R_E + \frac{d}{d\beta}\left(\frac{I_C}{\beta}\right) R_E$$

$$0 = \frac{dI_C}{d\beta} * \frac{R_{th}}{\beta} + 0 + \frac{dI_C}{d\beta} R_E + \frac{dI_C}{d\beta} \frac{R_E}{\beta}$$

$$0 = S'' * R_T + \frac{dI_C}{d\beta}\left[\frac{R_{th}}{\beta} + R_E + \frac{R_E}{\beta}\right]$$

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BIAS COMPENSATION TECHNIQUES:

* The biasing circuit provides stability of operating point due to the variations in transistor parameters such as I_{CO}, V_{BE} and β
* The stabilization techniques uses resistive biasing circuits which permit I_B to vary so as to keep I_C as constant.
* In otherhand, the compensation techniques uses temperature sensitive devices such as diodes, transistors, thermistors and sensitors etc. to maintain operating point stable.
* Sometimes for excellent bias and stabilization, both stabilization as well as compensation techniques are used.
* The following are some compensation techniques.

1. Diode compensation due to instability due to V_{BE} variations
2. Diode compensation due to instability due to I_{CO} variations
3. Thermistor compensation
4. Sensitor compensation

1. Diode compensation for Instability due to V_{BE} Variations:

* For Ge transistor, the changes in I_{CO} with temperature contribute more serious problem than Si transistor.
* In otherhand, in a Silicon transistor, the changes in V_{BE} with temperature changes collector current (I_C).

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* The below figure shows the circuit for self bias stabilization technique with diode compensation for V_{BE}.

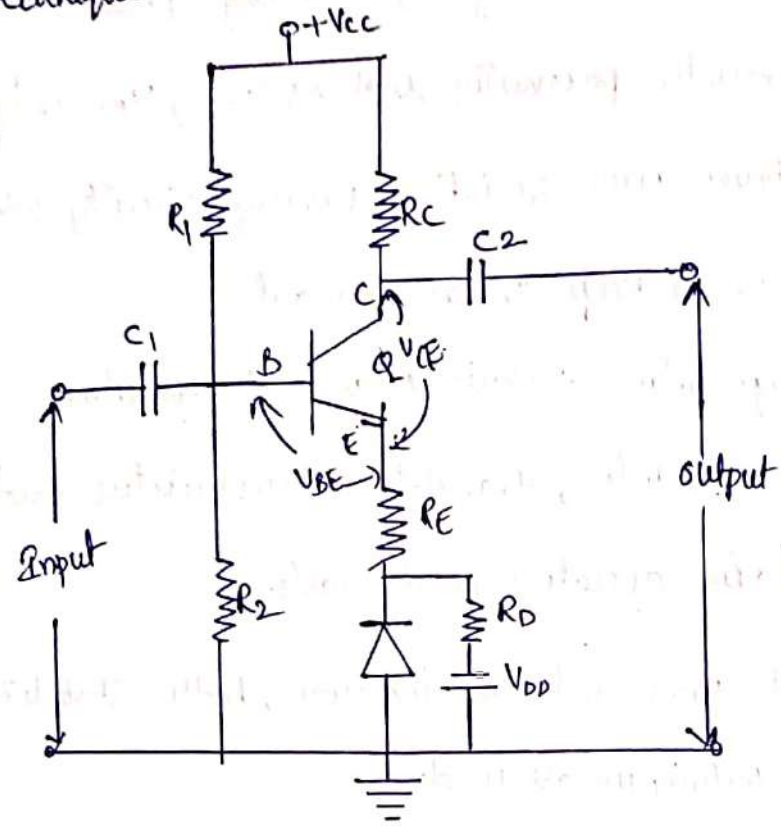

FIG: SELFBIAS WITH STABILIZATION AND COMPENSATION

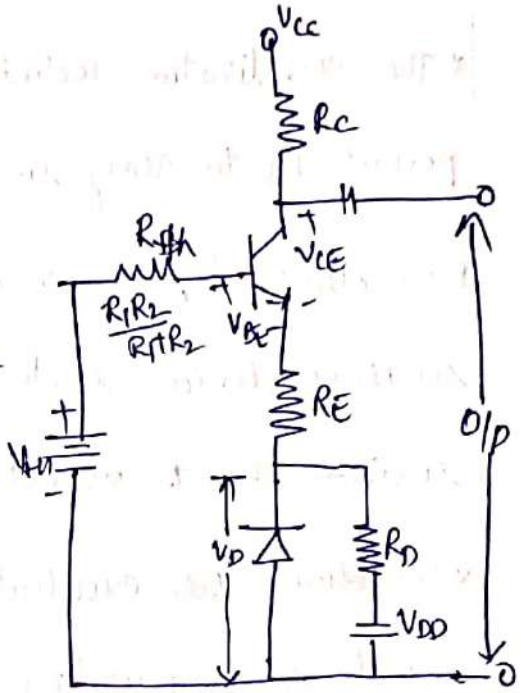

FIG: THEVENINS EQUIVALENT CIRCUIT

* The diode 'D' used here is of the same material and type as the transistor.

* Hence the diode voltage V_D across the diode has same temperature coefficient (-2.5 mV/°C) as V_{BE} of the transistor. Hence the diode D is in forward bias.

Apply KVL to base circuit

$$-V_{th} + I_B R_{BB} + V_{BE} + I_E R_E - V_D = 0$$

$$V_{th} = I_B R_{BB} + V_{BE} + I_E R_E - V_D \Rightarrow$$

$$V_{th} - V_{BE} + V_D = I_B R_{BB} + (I_B + I_C) R_E \quad (\because I_E = I_B + I_C)$$

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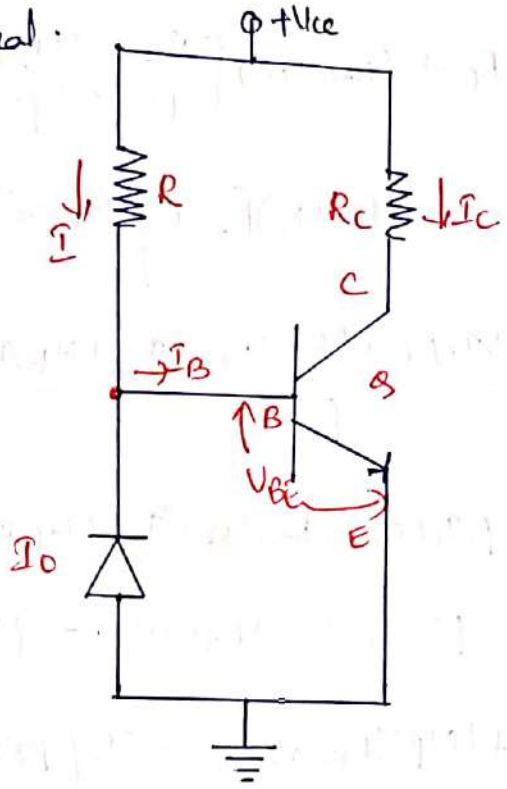
* So collector current I_C remains constant inspite of variations in V_{BE}.

Diode Compensation for Instability due to I_{CO} variations:

* Consider the transistor amplifier circuit with diode 'D' used for compensation of variations in I_{CO}.
* The diode D and the transistor are of the same type and same material.



* From the circuit it is clear that the diode D is connected in Reverse bias condition.
* So only Reverse saturation current will flow through the diode.
* The Reverse saturation current I_O of the diode will increase with temperature as that of collector leakage current (I_{CO}).

From circuit $I = \frac{V_{CC} - V_{BE}}{R} = \frac{V_{CC}}{R}$ = Constant

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But $I_C = \beta I_B + (1+\beta) I_{CO}$

$$\beta I_B = I_C - (1+\beta) I_{CO}$$

$$I_B = \frac{I_C}{\beta} - \frac{(1+\beta)}{\beta} I_{CO}$$

$$V_{th} - V_{BE} + V_D = I_B R_{th} + I_B R_E + I_C R_E$$

$$V_{th} - V_{BE} + V_D = I_B (R_{th} + R_E) + I_C R_E$$

$$V_{th} - V_{BE} + V_D = I_C R_E + (R_{th} + R_E) \left[\frac{I_C}{\beta} - \frac{(1+\beta)}{\beta} I_{CO} \right]$$

$$V_{th} - V_{BE} + V_D = I_C R_E + (R_{th} + R_E) \left[\frac{I_C - (1+\beta) I_{CO}}{\beta} \right]$$

$$V_{th} - V_{BE} + V_D = \frac{\beta I_C R_E + (R_{th} + R_E)(I_C - (1+\beta) I_{CO})}{\beta}$$

$$\beta (V_{th} - V_{BE} + V_D) = \beta I_C R_E + (R_{th} + R_E)(I_C - (1+\beta) I_{CO})$$

$$\beta (V_{th} - V_{BE} + V_D) = \beta I_C R_E + I_C (R_{th} + R_E) - (1+\beta) I_{CO} (R_{th} + R_E)$$

$$\beta (V_{th} - V_{BE} + V_D) + (1+\beta)(R_{th} + R_E) I_{CO} = I_C [\beta R_E + R_{th} + R_E]$$

$$\beta (V_{th} - V_{BE} + V_D) + (1+\beta)(R_{th} + R_E) I_{CO} = I_C [R_{th} + (1+\beta) R_E]$$

$$I_C = \frac{\beta (V_{th} - V_{BE} + V_D) + (1+\beta)(R_{th} + R_E) I_{CO}}{R_{th} + (1+\beta) R_E} \rightarrow (2)$$

* Since variation in V_{BE} with temperature is same as the variation in V_D with temperature.

* Hence the quantity $(V_{BE} - V_D)$ remains remains constant from eq (2).

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* The diode D is reverse biased by V_{BE}. So the current through the diode is reverse saturation current.

$$I_B = I - I_0$$

But $I_C = \beta I_B + (1+\beta) I_{CO}$

$$I_C = \beta(I - I_0) + (1+\beta) I_{CO}$$

$$I_C = \beta I - \beta I_0 + \beta I_{CO} \quad (\because \beta >> 1)$$

Here $I_0 \approx I_{CO}$

$$I_C = \beta I - \beta I_0 + \beta I_0$$

$$I_C = \beta I$$

$$I_C = \beta * \frac{V_{CC}}{R}$$

* From the above equation I_C is almost constant.

* Hence the collector current I_C remains constant.

3 THERMISTOR COMPENSATION:

* This method employs temperature sensitive resistive elements i.e., thermistors are used rather than diodes and transistors.

* Thermistors are "negative temperature coefficient devices in which its resistance decreases exponentially with increase in temperature.

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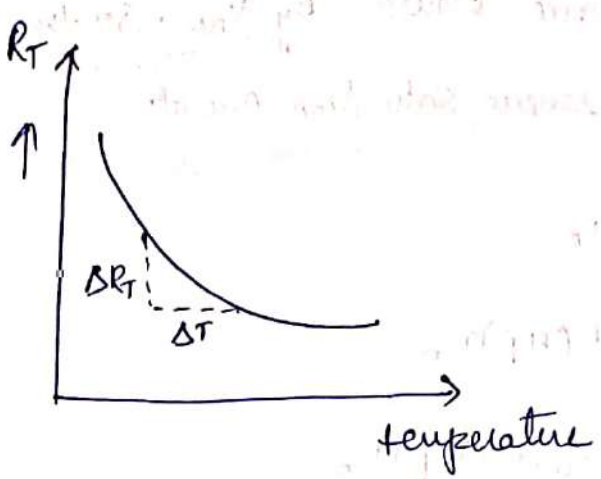

⇒ Slope of the curve is $\frac{\partial R_T}{\partial T}$

* Where $\frac{\partial R_T}{\partial T}$ is the temperature coefficient of thermistor.

* The below figure shows the thermistor compensation technique.

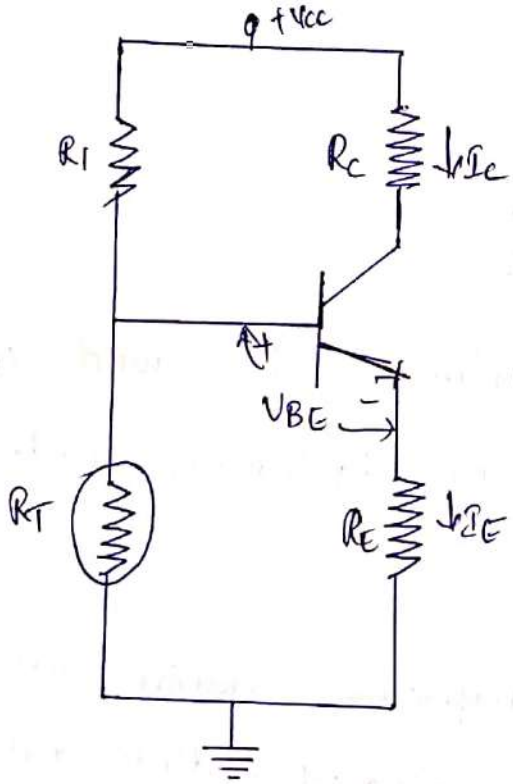

Fig: THERMISTOR COMPENSATION TECHNIQUE

* When temperature increases, the negative temperature coefficient device R_T decreases.

* Hence the voltage drop across R_T reduces (V_{BE}). The decrease in V_{BE} reduces I_B

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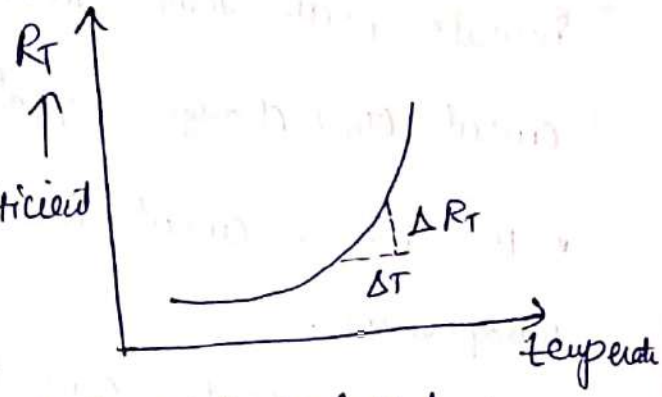
* As a result the collector current I_C is maintained as constant.

SENISTOR COMPENSATION :

* The Senistor is a positive temperature coefficient, its resistance increases exponentially with increase in temperature.

* The slope of this curve = $\frac{\partial R_T}{\partial T}$

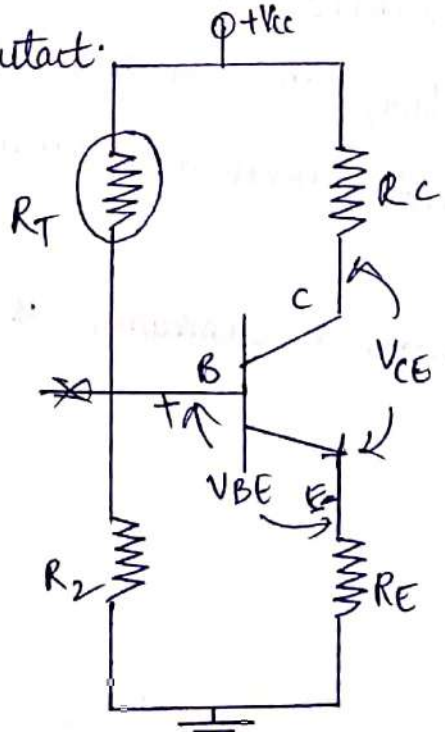
* Where $\frac{\partial R_T}{\partial T}$ is the temperature coefficient for senistor and the slope is positive.



* Consider a self bias circuit in which R_1 is replaced by R_T.

* As temperature increases, R_T increases which decreases the current flowing through R_2, which reduces the voltage drop across it.

* As voltage drop across R_2 decreases, I_B reduces and I_C is maintained constant.



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THERMAL RUNAWAY:

* The collector current for CE circuit is given by,

$$I_C = \beta I_B + (1+\beta) I_{CO}$$

* The three variables i.e., β, I_B, I_{CO} in above equation increases with temperature. In particular the reverse saturation current (I_{CO}) changes greatly with temperature.

* The leakage current (I_{CO}) doubles for every $10^{\circ}C$ raise in temperature.

* Due to collector current (I_C) the collector-base junction temperature increases, as temperature increases I_{CO} increases.

* As I_{CO} increases I_C further increases, as a result the temperature across collector-base junction increases.

* This process is cumulative and it is referred as "Self heating".

* the excess of heat produced at the collector-base junction may even burn and destroy the transistor.

* This situation is called thermal runaway of transistor.

* The condition for thermal runaway is $V_{CE} < \frac{V_{CC}}{2}$

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THERMAL RESISTANCE:

* Transistor is a temperature dependent device.
* In order to keep the temperature within the limits, the heat generated must be dissipated to the surroundings.
* Most of the heat within the transistor is produced at the collector junction.
* If the temperature exceeds the limit, junction is destroyed.
* For silicon transistor, the temperature is in the range 150°c to 225°c.
* For Germanium transistor, the temperature is 60°c to 100°c.
* Let T_A°c be the Ambient temperature i.e., temperature of surrounding air.

T_J°c be the temperature of Collector - base junction.

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Small signal Low frequency Transistor Amplifier Models

Amplifier:- An amplifier is a circuit, it can be used to increase the magnitude of the input current (or) voltage at the output without changing the shape of the signal.

Two port Network:-

"Transistor operates with reasonable linearity for small signals, so the operation of transistor in the active region can be represented by small signal linear models.

* The small signal h-parameter model can be used for low frequency analysis of BJT.

Two port Network and Network parameters:-

* A transistor can be treated as two-port network.
* The terminal behaviour of any two port network can be specified by terminal voltages V_1 and V_2 at port 1 and 2 similarly currents I_1 and I_2 at port 1 & 2.
* from this four variables (V_1, V_2, I_1, I_2), two variables are selected as independent variables and remaining two variables are expressed in terms of independent variables.

A two port Network is shown below.

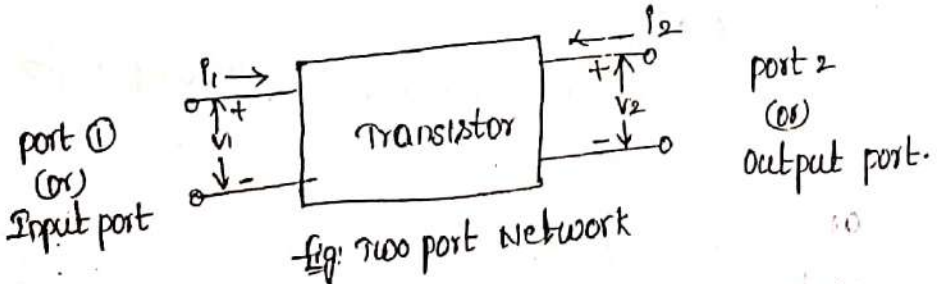

fig: Two port Network

* port ① is also termed as Input port and Port ② is also called as output port.

The two port Network parameters are shown below

(i) Z- parameters (or) Impedance parameters
(ii) Y- parameters (or) Admitance parameters
(iii) h- parameters (or) Hybrid parameters.

Z-parameters (or) Impedance parameters:-

In Z-parameters I_1 and I_2 are independent parameters. The voltages V_1 and V_2 are represented as

$$V_1 = Z_{11} I_1 + Z_{12} I_2 \longrightarrow (1)$$

$$V_2 = Z_{21} I_1 + Z_{22} I_2 \longrightarrow (2)$$

These four impedance parameters $Z_{11}, Z_{22}, Z_{12}, Z_{21}$ are defined as follows.

$$Z_{11} = \left[\frac{V_1}{I_1}\right] \text{ with } I_2 = 0.$$

Z_{11} = Input impedance with output port is open circuited.

$$Z_{22} = \left[\frac{V_2}{I_2}\right] \text{ with } I_1 = 0.$$

Z_{22} = output impedance with input port is open circuited.

$$Z_{12} = \left[\frac{V_1}{I_2}\right] \text{ with } I_1 = 0.$$

Z_{12} = Reverse transfer impedance with input port is open circuited.

$$Z_{21} = \left[\frac{V_2}{I_1}\right] \text{ with } I_2 = 0$$

Z_{21} = forward transfer impedance with output port is open circuited.

Y-parameters (or) Admittance parameters :-

Here, V_1 and V_2 are taken as independent variables. The currents I_1 and I_2 are given by $I_1 = Y_{11} V_1 + Y_{12} V_2 \longrightarrow (1)$

$$I_2 = Y_{21} V_1 + Y_{22} V_2 \longrightarrow (2)$$

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Y_{11}, Y_{12}, Y_{21} and Y_{22} are short-circuit admittance parameters. (2)

$$Y_{11} = \left[\frac{I_1}{V_1}\right] \text{ with } V_2 = 0$$

= Input admittance with port 2 short circuited.

$$Y_{22} = \left[\frac{I_2}{V_2}\right] \text{ with } V_1 = 0$$

= output admittance with port 1 short circuited.

$$Y_{12} = \left[\frac{I_1}{V_2}\right] \text{ with } V_1 = 0$$

= Reverse transfer admittance with port 1 short circuited.

$$Y_{21} = \left[\frac{I_2}{V_1}\right] \text{ with } V_2 = 0$$

= forward transfer admittance with port 2 short circuited.

Hybrid parameters (or) h-parameters:-

If the input current I_1 and output voltage V_2 are taken as independent variables, the input voltage V_1 and output current I_2 can be written as

$$V_1 = h_{11} I_1 + h_{12} V_2$$

$$I_2 = h_{21} I_1 + h_{22} V_2$$

The four hybrid parameters h_{11}, h_{12}, h_{21}, h_{22} are defined as follows.

$$h_{11} = \left[\frac{V_1}{I_1}\right] \text{ with } V_2 = 0 \text{ ; units are ohms } (\Omega)$$

= Input impedance with output port short circuited.

$$h_{22} = \left[\frac{I_2}{V_2}\right] \text{ with } I_1 = 0 \text{ ; units are mhos } \mho \text{ or } \Omega^{-1}$$

$$h_{12} = \left[\frac{V_1}{V_2}\right] \text{ with } I_1 = 0 \text{; Dimension less.}$$

= Reverse voltage transfer Ratio with input port open circuited.

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$h_{21} = \left[\frac{I_2}{I_1}\right]$ with $V_2 = 0$; Dimension Less

= forward current gain with output port short circuited.

As the dimensions are different ie., they are hybrid in nature, these parameters are called as hybrid parameters.

* An alternative Subscript notation recommended by IEEE is commonly used:

$i = 11$ = Input; $o = 22$ = output

$f = 21$ = forward Transfer; $r = 12$ = Reverse transfer.

Notations used in Transistor circuits:-

*When h-parameters are applied to transistors, it is a common practice to add a second subscript to designate the type of configuration considered - 'e' for common emitter, 'b' for common base & 'c' for common collector.

* for a common emitter (CE) configuration

$h_{ie} = h_{11e}$ = short circuit input impedance.

$h_{oe} = h_{22e}$ = open circuit output admittance.

$h_{re} = h_{12e}$ = open circuit reverse voltage transfer Ratio.

$h_{fe} = h_{21e}$ = short circuit forward current gain.

The four parameters $h_{11}, h_{12}, h_{21}, h_{22}$ are real numbers and the voltages and currents V_1, V_2 and I_1, I_2 are functions of time

The hybrid model for two-port Networks:-

Based on the definition of hybrid parameters the mathematical model for two-port networks known as h-parameter model can be developed.

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The H-parameter equations are

$$V_1 = h_i I_1 + h_r V_2 \longrightarrow (1)$$

$$I_2 = h_f I_1 + h_o V_2 \longrightarrow (2)$$

* The model must satisfy the above equations. This can be designed by applying Kirchoff's voltage law at input loop and Kirchoff's current law at the output node.

* The input circuit should have dependent voltage generator and output circuit contains a dependent current generator.

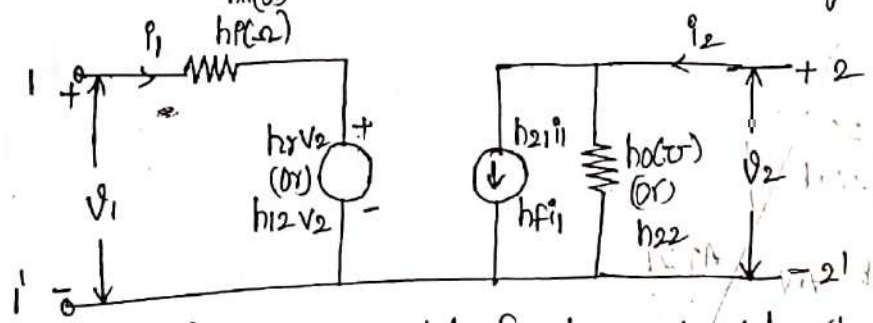

fig: Hybrid model for two port network.

Transistor Hybrid model:-

* Many transistor models have been proposed each model has particular advantage and disadvantage.

* The use of h-parameters to describe a transistor have following advantages:

(i) h-parameters are real numbers upto radio frequencies

(ii) They are easy to measure.

(iii) They can be determined from the transistor static characteristics.

(iv) easily convertable from one configuration to other.

(v) They are convinent to use in circuit analysis and design.

(vi) Readily supplied by manufacturers.

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In order to derive the hybrid model for a transistor, let us consider the common-emitter configuration as shown below

*from figure the variables are i_B, i_C, $V_B(V_{BE})$ and $V_C(V_{CE})$.

*In hybrid parameters ie., H-parameters, input current and output voltage are independent variables

So i_B, V_C are independent variables.

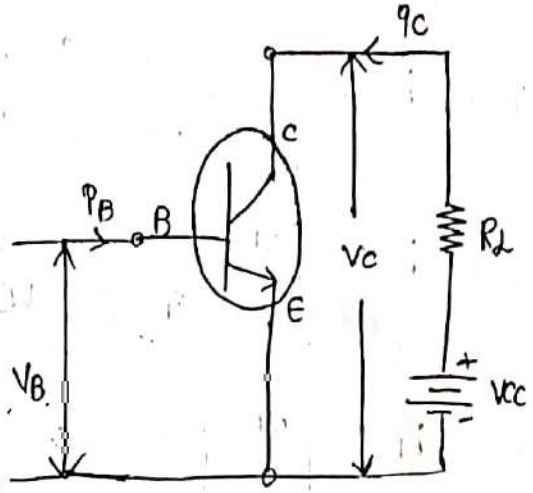

fig: CE transistor circuit

$\therefore V_B$ is the function of i_B and V_C and i_C is the function of i_B and V_C.

Then;

$$V_B = f_1(i_B, V_C) \longrightarrow (1)$$

$$i_C = f_2(i_B, V_C) \longrightarrow (2).$$

By considering Taylor's series expansion around the Q-point I_B, V_C and neglecting higher order terms the following equations are obtained.

$$\Delta V_B = \left[\frac{\partial f_1}{\partial i_B}\right]_{V_C} \Delta i_B + \left[\frac{\partial f_1}{\partial V_C}\right]_{i_B} \Delta V_C \longrightarrow (3)$$

$$\Delta i_C = \left[\frac{\partial f_2}{\partial i_B}\right]_{V_C} \Delta i_B + \left[\frac{\partial f_2}{\partial V_C}\right]_{i_B} \Delta V_C \longrightarrow (4)$$

where $\Delta V_B, \Delta V_C, \Delta i_B, \Delta i_C$ represents the small-signal base and collector voltages and currents. they can be represented by v_b, v_c, i_b, i_c.

Hence eqn (3) and (4) can be written as

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$$V_b = h_{ie} i_b + h_{re} V_c$$

$$i_c = h_{fe} i_b + h_{oe} V_c$$

where $h_{ie} = \left[\frac{\partial f_1}{\partial i_B}\right]_{V_c} = \left[\frac{\partial V_B}{\partial i_B}\right]_{V_c} \approx \left[\frac{\Delta V_B}{\Delta i_B}\right]_{V_c} = \left[\frac{V_b}{i_b}\right]_{V_c}$

$$h_{re} = \left[\frac{\partial f_1}{\partial V_c}\right]_{i_B} = \left[\frac{\partial V_B}{\partial V_C}\right]_{i_B} \approx \left[\frac{\Delta V_B}{\Delta V_c}\right]_{i_B} = \left[\frac{V_B}{V_c}\right]_{i_B}$$

$$h_{fe} = \left[\frac{\partial f_2}{\partial I_B}\right]_{V_c} = \left[\frac{\partial i_c}{\partial i_B}\right]_{V_c} \approx \left[\frac{\Delta i_c}{\Delta i_B}\right]_{V_c} = \left[\frac{i_c}{i_B}\right]_{V_c}$$

$$h_{oe} = \left[\frac{\partial f_2}{\partial V_c}\right]_{i_B} = \left[\frac{\partial i_c}{\partial V_c}\right]_{i_B} \approx \left[\frac{\Delta i_c}{\Delta V_c}\right]_{i_B} = \left[\frac{i_c}{V_C}\right]_{i_B}$$

The above equations define the h-parameters for the CE configuration.

Hybrid model and equations for common emitter configuration:

*In CE configuration, the independent variables for h-parameters are input current (i_b) and output voltage (V_c).

* The h-parameters are h_{ie}, h_{oe}, h_{re} h_{fe}

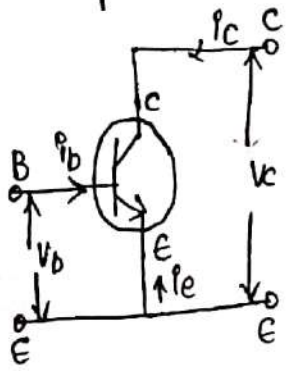

fig: CE configuration

$$V_b = h_{ie} i_b + h_{re} V_c$$

$$i_c = h_{fe} i_b + h_{oe} V_c$$

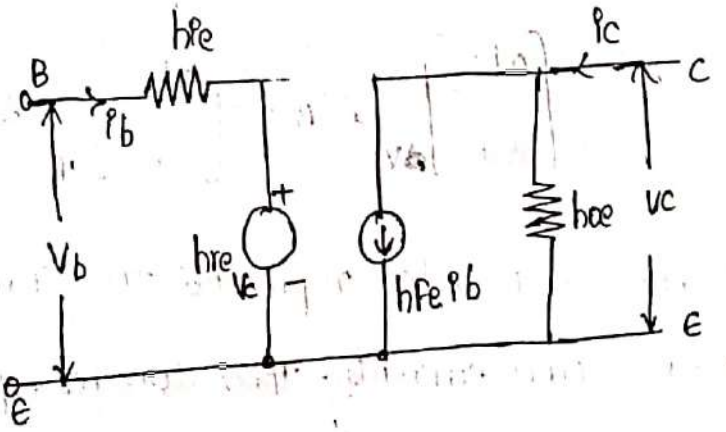

fig: Hybrid model for CE Configuration.

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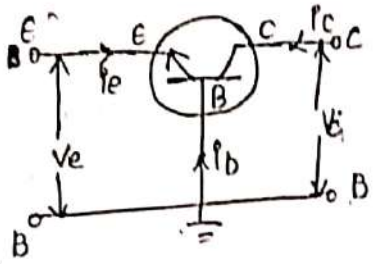
Hybrid model for CB configuration

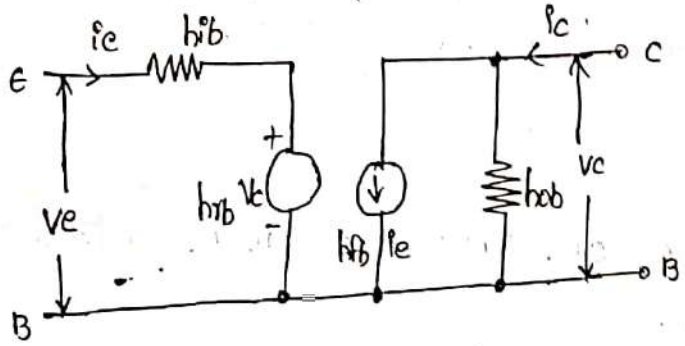
*In CB configuration, the independent variables are input current (i_e) and output voltage (V_c).

$$\therefore V_e = h_{ib} i_e + h_{rb} V_c$$

$$i_c = h_{fb} i_e + h_{ob} V_c$$



The equivalent hybrid model is shown below.



Hybrid model for CC configuration :-

*In CC configuration, the independent variables are input current (i_b), output voltage (V_e).

$$\therefore V_b = h_{ic} i_b + h_{rc} V_e$$

$$i_e = h_{fc} i_b + h_{oc} V_e$$

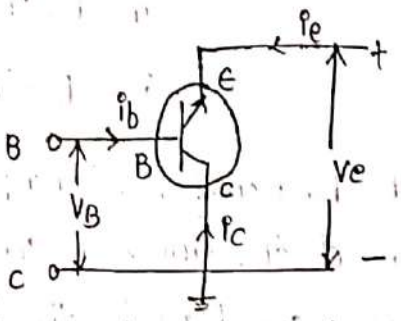


fig: CC-Configuration.

The hybrid model for CC-Configuration is shown below.

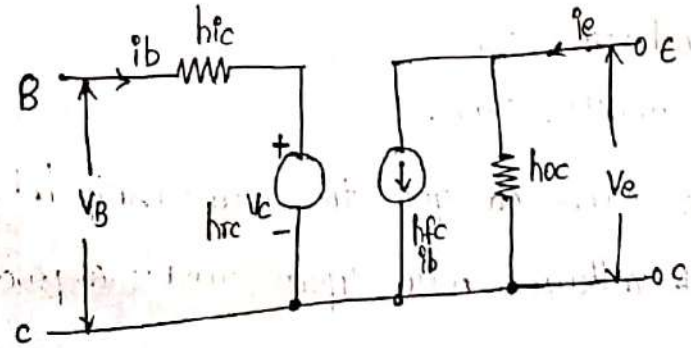


fig: Hybrid model for CC-Configuration.

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Typical h-parameter values of transistor

parameter	CC	CC	CB
h_i	1100Ω	1100Ω	22Ω
h_r	2.5×10^{-4}	1	3×10^{-4}
h_f	50	−51	−0.98
h_o	25μA/V	25μA/V	0.49μA/V

Determination of h-parameters from Transistor characteristics:-

*The function relationships of any configuration can be considered by taking independent variables.

*for example, the functional relationship of CE configuration is shown below.

$$V_b = f_1(i_b, V_c)$$

$$i_c = f_2(i_b, V_c)$$

* Such functional relationships can be represented by the characteristic curves of the transistor. There are two families of curves that are usually specified by the transistor.

The two curves are

1. Input characteristics curve
2. output characteristics curve.

* The output characteristics curve is gives the relationship between output current and output voltage with input current as parameter.

* The input characteristics curve gives the relationship between input voltage and input current with output voltage as parameter.

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The input and output characteristics of CE configuration is shown below.

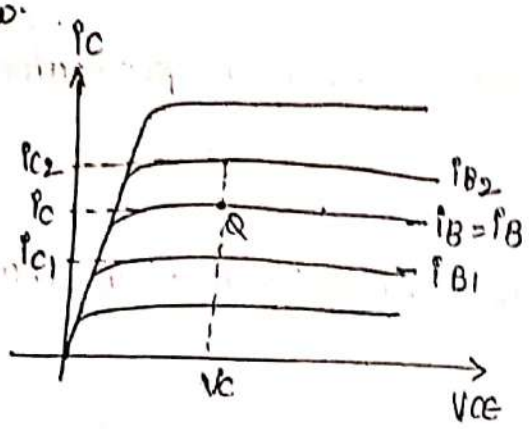

fig: output characteristics of CE configuration.

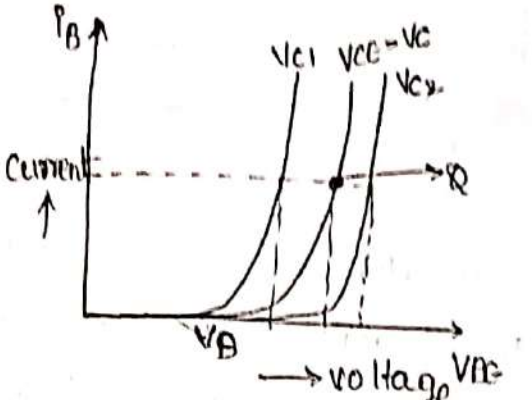

fig: Input characteristics of CE configuration.

parameter "hfe" :-

The parameter hfe is defined as ratio of change in collector current to the change in base current, with Vc is kept as constant.

$$hfe = \left[\frac{\partial I_C}{\partial I_B}\right]_{V_C} = \frac{I_{C2} - I_{C1}}{I_{B2} - I_{B1}}$$

This parameter can be calculated by considering output characteristics curve of CE configuration.

* The parameter hfe is the most important small signal parameter of the transistor. In CE configuration current transfer ratio is also represented as β.

β' = hfe for small signal

β' = hFE for Large signal.

parameter "hoe" :-

By Definition hoe is

$$hoe = \left[\frac{\partial I_C}{\partial V_C}\right]_{I_B} = \left[\frac{\Delta I_C}{\Delta V_C}\right]_{I_B} = \left[\frac{I_{C2} - I_{C1}}{V_{C2} - V_{C1}}\right]$$

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* The slope of the output characteristics at the operating point gives the value of hoe.
* This parameters can be calculated by considering the output characteristics of ce configuration.

parameter hfe:=

'hfe' is defined as the ratio of change in base voltage to the change in base current with Vc as constant.

$$hfe = \left[\frac{\partial V_B}{\partial i_B}\right]_{V_C} = \left[\frac{\Delta V_B}{\Delta i_B}\right]_{V_C}$$

$$hfe = \left[\frac{V_{B_2} - V_{B_1}}{i_{B_2} - i_{B_1}}\right]$$

* The slope of input characteristics at Q-point gives the value of 'hfe'.
* this parameter can be calculated by considering input characteristics

parameter hre:=

'hre' is defined as the ratio of change in base voltage to the change in collector voltage with I_B as constant.

$$hre = \left[\frac{\partial V_B}{\partial V_C}\right]_{I_B} = \left[\frac{\Delta V_B}{\Delta V_C}\right]_{I_B} = \frac{V_{B_2} - V_{B_1}}{V_{C_2} - V_{C_1}}$$

* A vertical line on the input characteristics of ce configuration represents the constant base current.

* This parameter can be calculated by considering input characteristics of ce configuration.

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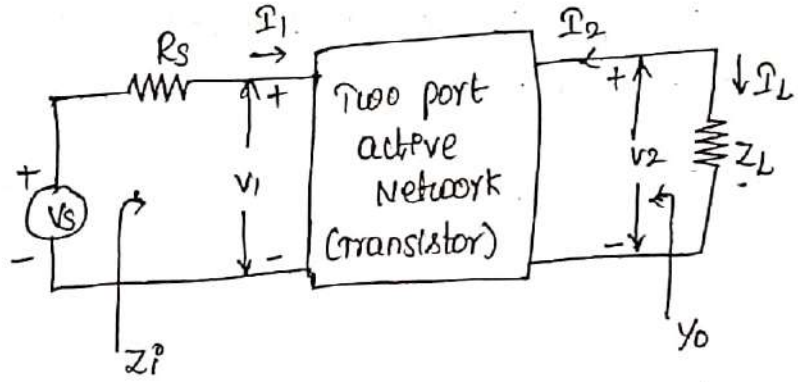
Analyses of CB, CE and CC configuration using h-parameters:-

*A transistor amplifier can be constructed by connecting an external load and signal source as indicated in below figure.



fig(a): Basic Amplifier circuit.

* The equivalent hybrid model for the above circuit is shown in below fig(b). This circuit is valid for any type of load whether it is pure resistance & impedance (or) another transistor.

* It is assumed that h-parameters remain constant over the operating range and input is sinusoidal.

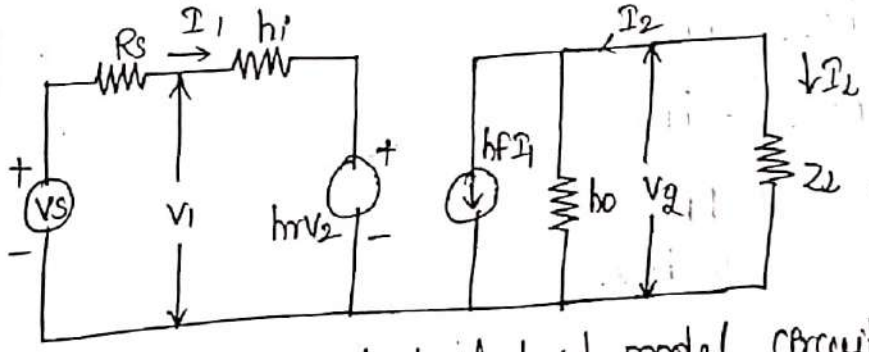


fig: Equivalent hybrid model circuit for two-port device.

four parameters can be derived from above equation

1. current gain (AI)
2. Input Impedance (Z_i)
3. voltage gain (AV)
4. output admittance (Y_o).

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from above circuit,

$$I_2 = h_f I_1 + h_o V_2 \longrightarrow$$

Current gain (A_I):- It is also known as current amplification, current gain of a transistor amplifier is defined as the ratio of output current to the input current.

$$A_I = \frac{I_L}{I_1} = \frac{-I_2}{I_1} \longrightarrow (1)$$

from above circuit

$$I_2 = h_f I_1 + h_o V_2 \longrightarrow (2)$$

w.k.t $V_2 = I_L Z_L = -I_2 \cdot Z_L \longrightarrow (3)$

substituting eq (3) in (2)

$$I_2 = h_f I_1 + h_o (-I_2 Z_L)$$

$$I_2 = h_f I_1 - h_o I_2 Z_L$$

$$I_2 + I_2 h_o Z_L = h_f I_1$$

$$I_2 [1 + h_o Z_L] = h_f I_1$$

$$\frac{I_2}{I_1} = \frac{h_f}{1 + h_o Z_L}$$

$$A_I = \frac{-I_2}{I_1} = \frac{-h_f}{1 + h_o Z_L}$$

$$\boxed{A_I = \frac{-h_f}{1 + h_o Z_L}}$$

Input Impedance (Z_i):- from the circuit, R_s is the signal source resistance. The impedance by looking into the input terminals of the amplifier. $Z_i = \frac{V_1}{I_1} \longrightarrow (1)$

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from the circuit

$$V_1 = h_i^o I_1 + h_r V_2$$

$$Z_i = \frac{h_i I_1 + h_r V_2}{I_1} \qquad \left(Z_i = \frac{V_1}{I_1}\right)$$

$$Z_i^o = h_i^o + h_r \cdot \frac{V_2}{I_1} \cdot \longrightarrow (2)$$

we know that $V_2 = -I_2 Z_L$ and $A_I = \frac{-I_2}{I_1}$

$$V_2 = A_I I_1 Z_L \longrightarrow (3)$$

Substituting eqn (3) in (2)

$$Z_i^o = h_i + h_r \frac{A_I I_1 Z_L}{I_1}$$

$$Z_i^o = h_i + h_r A_I Z_L \longrightarrow (4)$$

$$Z_i^o = h_i + h_r \left[\frac{-h_f}{1+h_o Z_L}\right] \cdot Z_L \qquad \left[\because A_I = \frac{-h_f}{1+h_o Z_L}\right]$$

$$= h_i - \frac{h_f \cdot h_r \cdot Z_L}{Z_L\left[\frac{1}{Z_L} + h_o\right]}$$

$$Z_i^o = h_i - \frac{h_f \cdot h_r}{h_o + \frac{1}{Z_L}} \qquad \left[\because \frac{1}{Z_L} = Y_L\right]$$

$$\boxed{Z_i^o = h_i - \frac{h_f \cdot h_r}{h_o + Y_L}}$$

Voltage gain (A_V):- It is also known as "voltage Amplification factor".

It is defined as ratio of output voltage 'V_2' to the input voltage V_1.

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$$A_V = \frac{V_2}{V_1}$$

$$A_V = \frac{-I_2 \cdot Z_L}{V_1} \qquad \left[\because V_2 = -I_2 Z_L\right]$$

$$A_V = \frac{A_I I_1 Z_L}{V_1} \qquad \left[A_I = \frac{-I_2}{I_1}\right]$$

$$\boxed{A_V = \frac{A_I Z_L}{Z_i}} \qquad \left(\because Z_i = \frac{I_1}{V_1}\right]$$

Output Admittance (Y_o):- Y_o is obtained by making V_s to zero and Z_L to infinity.

$$Y_o = \frac{I_2}{V_2} \quad \text{with } V_s = 0 \text{ \& } R_L = \infty$$

from the circuit $I_2 = h_f I_1 + h_o V_2$

dividing by V_2 on both sides

$$\frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_o \frac{V_2}{V_2}$$

$$\frac{I_2}{V_2} = h_f \frac{I_1}{V_2} + h_o \longrightarrow (1)$$

with $V_s = 0$, by applying KVL to i/p ckt,

$$R_s I_1 + h_i I_1 + h_r V_2 = 0$$

$$I_1 (R_s + h_i) + h_r V_2$$

$$\therefore I_1 (R_s + h_i) = -h_r V_2$$

$$\frac{I_1}{V_2} = \frac{-h_r}{R_s + h_i} \longrightarrow (2)$$

Substituting (2) in (1)

$$\frac{I_2}{V_2} = \frac{-h_f h_r}{R_s + h_i} + h_o$$

$$\boxed{Y_o = h_o - \frac{h_f h_r}{R_s + h_i}}$$

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Voltage Gain (Avs) with source Resistance (Rs):-

*Overall voltage gain $A_{VS} = \frac{V_2}{V_S} = \frac{V_2}{V_1} \cdot \frac{V_1}{V_S} = A_V \frac{V_1}{V_S}$ → (1)

*The equivalent input circuit using Thevenins Theorem is shown below.

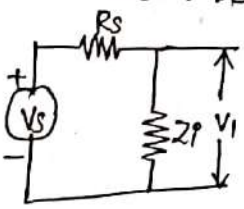


fig: Equivalent i/p ckt

from the input circuit

$$V_1 = \frac{V_S Z_i}{R_S + Z_i}$$

$$\frac{V_1}{V_S} = \frac{Z_i}{Z_i + R_S} \rightarrow (2)$$

Substituting eq (2) in (1)

$$A_{VS} = A_V \left[\frac{Z_i}{Z_i + R_S}\right]$$

we know that $A_V = \frac{A_I Z_L}{Z_i}$

$$A_{VS} = \frac{A_I Z_L Z_i}{Z_i (Z_i + R_S)}$$

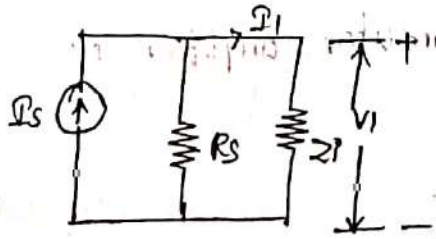
$$\boxed{A_{VS} = \frac{A_I Z_L}{Z_i + R_S}}$$

If $R_S = 0$, then $A_{VS} = \frac{A_I Z_L}{Z_i} = A_V$

where A_V is the voltage gain of ideal voltage source.

Current Amplification (A_{IS}) by taking source Resistance (R_S) into account:-

The modified input circuit using Nortons Theorem is shown below.



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over all current gain $A_{IS} = \frac{-I_2}{I_S} = \frac{-I_2}{I_1} \times \frac{I_1}{I_S}$

$$A_{IS} = A_I \frac{I_1}{I_S} \rightarrow (1)$$

from figure $I_1 = I_S \cdot \frac{R_S}{R_S + Z_i'}$

$$\frac{I_1}{I_S} = \frac{R_S}{R_S + Z_i'} \rightarrow (2)$$

Substitute eq(2) in (1)

$$\boxed{A_{IS} = A_I \cdot \frac{R_S}{R_S + Z_i'}}$$

If $R_S = \infty$ then ~~$A_{IS} = \frac{A_I \infty}{\infty + Z_i'}$~~ $= A_{IS} = A_I$

operating power Gain(Ap):-

from hybrid model, the average power delivered to the load is

$$P_2 = |V_2||I_L| \cos\theta$$

where θ = phase angle between V_2 and I_2.

assume the Load as Resistive Load. so $Z_L = R_L$.

$$A_p = \text{power gain} = \frac{P_2}{P_1} = \frac{-V_2 I_2}{V_1 I_1} = A_V \cdot A_I \qquad \left(A_V = \frac{A_I Z_L}{R_S}\right)$$

$$A_p = A_I \cdot \frac{A_I R_L}{R_i'}$$

$$\boxed{A_p = A_I^2 \left[\frac{R_L}{R_i'}\right]}$$

The small signal analysis of transistor amplifier is

① $A_I = \frac{-h_f}{1 + h_o Z_L}$

② $Z_i' = h_i - \frac{h_f h_r}{Y_L + h_o}$

③ $Y_o = h_o - \frac{h_f h_r}{h_i' + R_S}$

④ $A_V = \frac{A_I Z_L}{Z_I}$

⑤ $A_{VS} = \frac{A_V Z_i'}{Z_i' + R_S}$

⑥ $A_{IS} = \frac{A_I R_S}{Z_i' + R_S} \Rightarrow A_{VS} \cdot \frac{R_S}{Z_L}$

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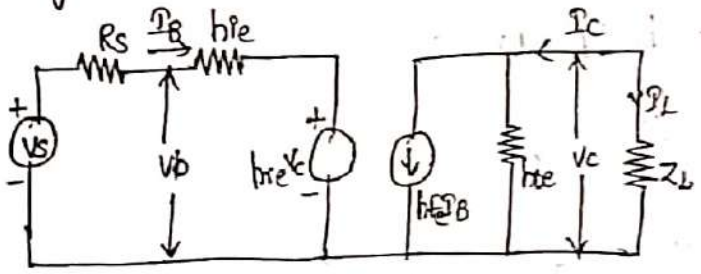
Analysis of CE transistor using H-parameters:-

The analysis of CE configuration using H-parameters is shown below.

*The equivalent hybrid model for CE configuration is shown below.



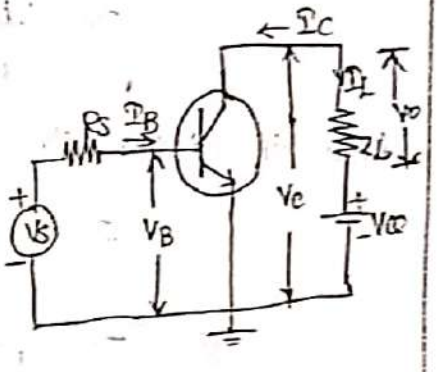


fig: Hybrid Model for CE Amplifier.

Current gain:- (A_I)

The current gain of an amplifier is defined as ratio of output current to the input current.

$$A_I = \frac{I_L}{I_B} = \frac{-I_C}{I_B} \longrightarrow (1)$$

from above circuit

$$I_C = h_{fe} I_B + h_{oe} V_C \longrightarrow (2)$$

from circuit $V_C = I_L Z_L = -I_C \cdot Z_L$

$$I_C = h_{fe} I_B + h_{oe}(-I_C Z_L)$$

$$I_C [1 + h_{oe} Z_L] = h_{fe} I_B$$

$$\frac{I_C}{I_B} = \frac{h_{fe}}{[1 + h_{oe} Z_L]}$$

$$\boxed{A_I = \frac{-I_C}{I_B} = \frac{-h_{fe}}{1 + h_{oe} Z_L}}$$

If $Z_L = 0$ then $\boxed{A_I = -h_{fe}}$.

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Input Impedance (Z_i):-

It is defined as the ratio of input voltage to the input current.

$$Z_i = \frac{V_b}{I_B}$$

from the input circuit $V_b = h_{ie} I_B + h_{re} V_c$

$$Z_i = \frac{h_{ie} I_B + h_{re} V_c}{I_B} \rightarrow (1)$$

$$Z_i = h_{ie} + h_{re} \frac{V_c}{I_B} \rightarrow (2)$$

We know that $V_c = -I_c \cdot Z_L$ and $A_I = \frac{-I_c}{I_B}$.

$$V_c = A_I I_B Z_L \rightarrow (3)$$

Substitute eq (3) in (2)

$$Z_i = h_{ie} + h_{re} \frac{A_I I_B Z_L}{I_B}$$

$$Z_i = h_{ie} + h_{re} A_I Z_L \rightarrow (4)$$

$$Z_i = h_{ie} + h_{re} \left[\frac{-h_{fe}}{1 + h_{oe} Z_L}\right] Z_L \quad \left(A_I = \frac{-h_{fe}}{1 + h_{oe} Z_L}\right)$$

$$\boxed{Z_i = h_{ie} - \frac{h_{re} \cdot h_{fe}}{h_{oe} + Y_L}}$$

If $Z_L = 0 \Rightarrow Y_L = 1/Z_L = \infty$

$$\therefore \boxed{Z_i = h_{ie}}$$

Voltage gain (A_V):- Voltage gain of an amplifier is defined as the ratio of the output voltage to input voltage.

$$A_V = \frac{V_c}{V_B}$$

$$A_V = \frac{-I_c Z_L}{V_B} \quad \left(\because A_I = \frac{-I_c}{I_B}\right)$$

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$$A_I = \frac{A_I I_B Z_L}{V_B}$$

$$A_I = \frac{A_I Z_L}{[V_B/I_B]} \Rightarrow \frac{A_I Z_L}{Z_i}$$

Output Admittance (Y_o) :- ~~output admittance is defined as the ratio of output current to the input voltage.~~

$Y_o =$

*Output admittance is defined as the ratio of output current to the output voltage.

$$Y_o = \frac{I_C}{V_C}$$

$$I_C = h_{fe} I_B + h_{oe} V_C \longrightarrow (1)$$

Dividing above equation (1) by V_C

$$\frac{I_C}{V_C} = h_{fe}\left[\frac{I_B}{I_C}\right] + h_{oe} \longrightarrow (2)$$

with $V_s = 0$, applying KVL to input circuit

$$R_s I_B + h_{ie} I_B + h_{re} V_C = 0$$

$$I_B(R_s + h_{ie}) = -h_{re} V_C$$

$$\frac{I_B}{V_C} = \frac{-h_{re}}{R_s + h_{ie}} \longrightarrow (3)$$

Substitute eq'n (3) in (2)

$$\frac{I_C}{V_C} = h_{fe}\left[\frac{-h_{re}}{R_s + h_{ie}}\right] + h_{oe}$$

$$\boxed{Y_o = h_{oe} - \frac{h_{re} h_{fe}}{R_s + h_{ie}}}$$

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(*) Small Signal Model of FET's:-

JFET small Signal Model:-

JFET small signal model can be analysed by two methods

i) Low frequency Analysis

ii) High frequency Analysis.

Low frequency Analysis:-

The for Low frequency equivalent circuit of JFET is shown below.

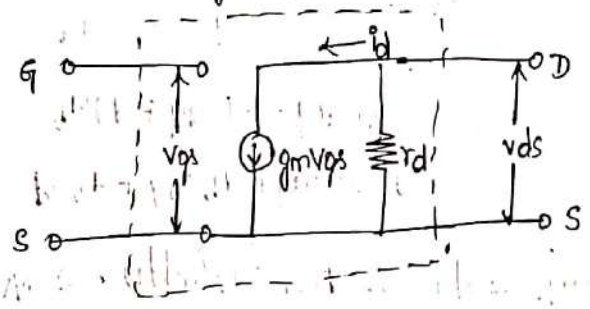

fig: equivalent circuit for JFET.

* The drain current (i_d) depends on gate to source voltage (V_{gs}) and transconductance (g_m).
* The product 'g_m' and 'V_{gs}' is represented as current source.
* The Drain current also depends on channel internal resistance 'r_d'.
* It is also referred as output impedance.
* The source - gate junction is always reverse biased, so it is represented as open circuit as shown in figure.
* The equivalent model must satisfy satisfy the below equation

$$i_d = V_{gs} \cdot g_m + \frac{V_{ds}}{r_d}$$

where V_{gs} → Gate to source voltage.

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Vds → Drain to source voltage.

g_m → Trans conductance.

High frequency Analysis:-

*At Low frequencies, the impedances are very High, as a result it offers negligable capacitances.

*At high frequencies, the capacitances at junction will affect the performance of circuit.

*,so the junction capacitances are included for High frequency analysis

*The high frequency equivalent circuit is shown below.

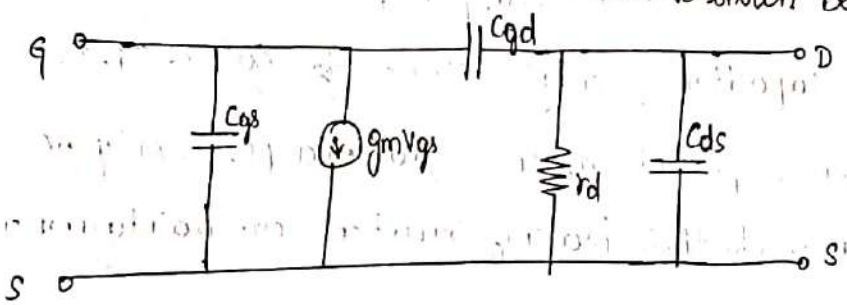

fig: High frequency equivalent circuit.

*from equivalent circuit, 'Cgs' represents gate-to-source junction capacitance which is also termed as barrier capacitance between gate to source.

* The capacitor Cgd represents the gate to Drain capacitance of channel.

* Due to this capacitances (Cgs, Cgd), the feedback exist between input and output circuit.

* Due to this feedback at high frequencies, the voltage amplification is declined.

FET common source (CS) Amplifier:-

In common source amplifier the input is applied between gate and source and output is taken from drain and

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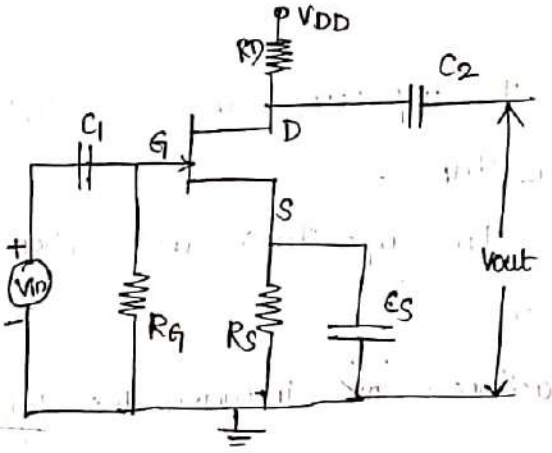
source.

* The circuit for common source (CS) Amplifier is shown below



where

C_1, C_2 – Coupling capacitors

C_S – Bypass capacitor

R_G – Gate Resistance

R_D – Drain Resistance

R_S – Source Resistance.

fig: Common source amplifier.

* from figure, Input capacitor C_i couples signal to gate of FET.

* It blocks DC-components present in the signal and passes only AC signal for amplification, because of this biasing conditions are maintained as constant.

* Bypass capacitor (C_S):- This capacitor is connected in parallel with Source Resistance (R_S) to provide low reactance path to the amplified AC signal. If it is not used the amplified ac signal passing through 'RS' will cause a voltage drop across it. This will reduce the output voltage, which reduces the gain of amplifier.

* output capacitor (C_2):-

* It couples the output of amplifier to Load (or) to the next stage of amplifier. It blocks dc and passes only ac part of amplified signal.

* for ac analysis all capacitors are short circuited.

* for bias/dc conditions all capacitors are open circuited.

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Analysis:-

All capacitors and dc supply voltages are short circuited and JFET low frequency equivalent circuit is shown below,

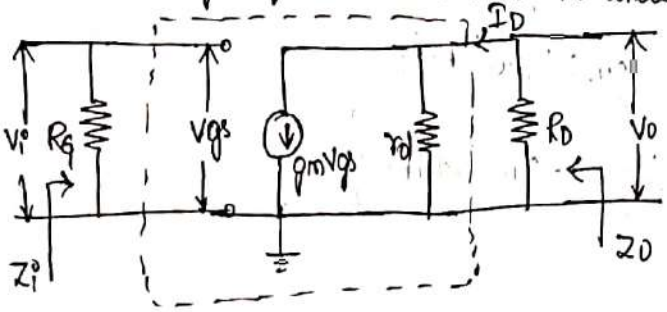


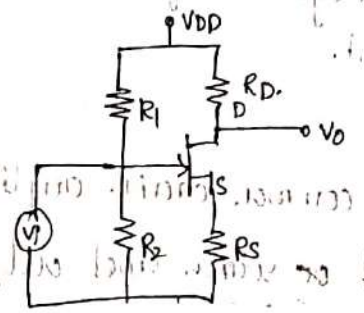
fig: Ac equivalent circuit of CS-FET with g_m as transconductance.

① Input Impedance:-

Input impedance $Z_i = R_G$

where $R_G = R_1 \| R_2$

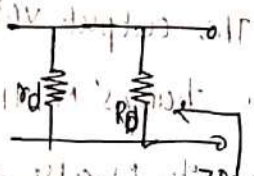
$$\therefore \boxed{Z_i = R_G = R_1 \| R_2}$$



② Output impedance:-

The output impedance Z_o is the impedance measured looking from output side with input voltage $V_i = 0$ ($V_{gs} = 0$)

* As a result $g_m V_{gs} = 0$.



* If $g_m V_{gs} = 0$, the current source is replaced by open circuit

$\therefore$ output impedance $Z_o = r_d \| R_D$

* If $r_d >> R_D$ then

output impedance $\boxed{Z_o \simeq R_D}$

Voltage gain (Av):-

voltage gain $A_v = \frac{V_o}{V_i}$ or $\frac{V_{ds}}{V_{gs}}$

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from fig. $V_o = -g_m V_{gs} [r_d || R_D]$

we know that $V_i = V_{gs}$

$$V_o = -g_m V_i [r_d || R_D]$$

$$A_V = \frac{V_o}{V_i} = -g_m (r_d || R_D)$$

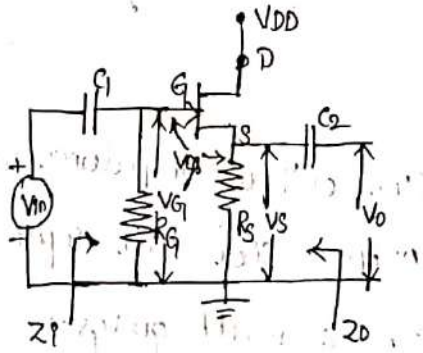
If $r_d >> R_D$ then $A_V = -g_m R_D$

The negative sign indicates 180° phase shift between input and output.

FET common Drain amplifier (CD):-

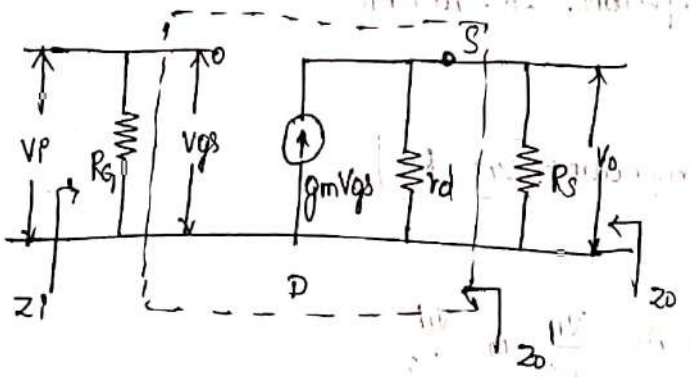
In common drain amplifier circuit, input is applied between gate and source and output is taken from source terminal

* when a signal is applied to JFET through C_1, V_G varies with signal.
* As V_{gs} is constant
* The output voltage at source V_s follows the changes in the input signal.
* so it is also called as source follower.



Here $V_S = V_G + V_{gs}$

The low-frequency equivalent circuit is shown below.



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Input Impedance (Z_i):-

Input impedance $\boxed{Z_i = R_G}$

output Impedance (Z_o):-

$$Z_o = Z_o' \,||\, R_S$$

where $Z_o' = \left.\frac{V_o}{I_d}\right|_{V_i=0}$

Applying KVL to outer loop

$$V_o = V_{gs} + V_e$$

when $V_i = 0 \Rightarrow V_{gs} = V_o$

$$I_d = g_m V_{gs} \Rightarrow g_m V_o = I_d$$

$$Z_o' = \frac{V_o}{I_d} = \frac{V_o}{g_m V_o} = \frac{1}{g_m}$$

$$Z_o = \frac{1}{g_m} \,||\, R_S \Rightarrow \frac{1/g_m \times R_S}{\frac{1}{g_m} + R_S} = \frac{R_S}{1 + g_m R_S}$$

Voltage Gain (A_V):-

voltage gain $A_V = \frac{V_o}{V_i}$

$V_o = -I_d (r_d \,||\, R_S)$ & $I_d = g_m V_{gs}$

$$V_o = -g_m V_{gs} (r_d \,||\, R_S) \longrightarrow (1)$$

w.k.t $V_i + V_{gs} = V_o$

$$V_i = -V_{gs} + V_o$$

$$= -V_{gs} - g_m V_{gs} (r_d \,||\, R_S)$$

$$V_i = -V_{gs} \left[1 + g_m (r_d \,||\, R_S)\right] \longrightarrow (2)$$

$$A_V = \frac{V_o}{V_i} = \frac{-g_m V_{gs} (r_d \,||\, R_S)}{-V_{gs} (1 + g_m (r_d \,||\, R_S))} \Rightarrow \frac{g_m (r_d \,||\, R_S)}{1 + g_m (r_d \,||\, R_S)}$$

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If $r_d >> R_S$ then $A_V = \frac{g_m R_S}{1 + g_m R_S}$

If $g_m R_S >> 1$ then $\boxed{A_V \simeq 1}$

*The positive sign on voltage gain indicates no phase shift (0° or 360°) between input and output

FET common Gate (CG) Amplifier:-

The circuit for common gate amplifier is shown below.

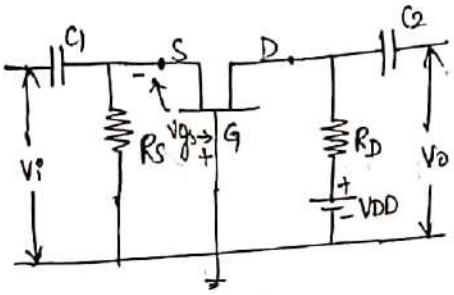

fig: CG Amplifier.

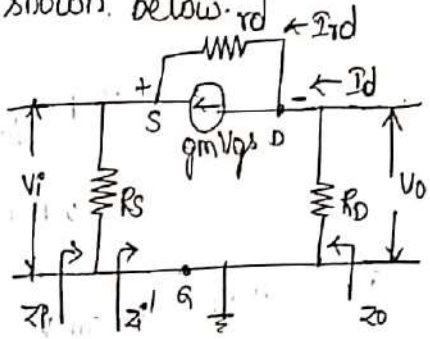

fig: equivalent circuit for CG Amplifier.

Voltage Gain:-

from equivalent circuit

$$V_i = -V_{gs}, \quad V_o = I_d R_D$$

$$V_{rd} = V_o - V_i \Rightarrow I_{rd} = \frac{V_o - V_i}{r_d}$$

Applying KVL to node 'D'

$$-I_D = I_{rd} + g_m V_{gs}$$

$$\frac{-V_o}{R_D} = \frac{V_o - V_i}{r_d} - g_m V_i$$

$$\frac{-V_o r_d}{R_D} = V_o - V_i - g_m r_d V_i$$

$$-V_o\left[1 + \frac{r_d}{R_D}\right] = -V_i\left[1 + g_m r_d\right]$$

$$A_V = \frac{V_o}{V_i} = \frac{(1 + g_m r_d) R_D}{R_D + r_d}$$

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Input Impedance:-

Input impedance $Z_i = R_S \| Z_i'$

$$Z_i' = \frac{r_d + R_D}{1 + g_m r_d}$$

$$Z_i = R_S \| \left[\frac{r_d + R_D}{1 + g_m r_d}\right]$$

$$Z_i = R_S \| \frac{1}{g_m}$$

$$A_v = \frac{V_o}{V_i} = \frac{(1 + g_m r_d) R_D}{R_D + r_d} \quad \text{--- (1)}$$

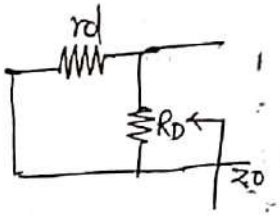
$$I \rightarrow \frac{V_o}{V_i \cdot R_D} = \frac{1 + g_m r_d}{R_D + r_d}$$

$$\frac{I}{V_i} = \frac{1 + g_m r_d}{R_D + r_d} \rightarrow \frac{1}{Z_i} = \frac{1 + g_m r_d}{r_d + R_D} \Rightarrow Z_i = \frac{r_d + R_D}{1 + g_m r_d}$$

If $r_d >> R_D$ and $g_m r_d >> 1$

Output Impedance:-

It is the impedance seen from the output terminals with input short circuited; $V_i = 0 \Rightarrow V_{gs} = 0$



$$Z_o = r_d \| R_D \Rightarrow \frac{r_d R_D}{r_d + R_D}$$

If $r_d >> R_D$ then $\boxed{Z_o = R_D}$

Generalized FET Amplifier:-

A Generalized FET amplifier can be used to analyse the CS, CG and CD amplifier circuits at Low frequencies.

* It consist of three independent signal sources
  - → V_i in series with gate
  - → V_s in series with source
  - → V_a in series with drain

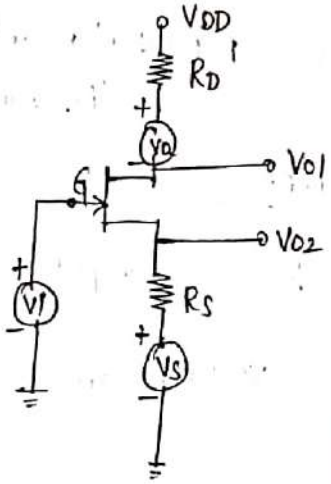
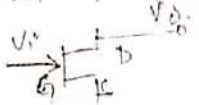
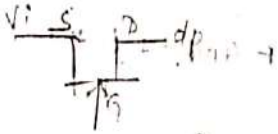


fig: Generalized FET amplifier

for CS Amplifier:-



* $V_s = 0$ and $V_a = 0$, the input signal is V_i and output is V_{o1} taken at drain



for CG amplifier:-

* $V_i = 0$ & $V_a = 0$, the signal is V_s with a source Resistance R_s and output is V_{o2} taken across source.

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For CD Amplifier (source-follower):-

* $V_S = 0$ and $V_a = 0$, $R_D = 0$, the signal voltage is V_i and output is V_{02} taken at the source.

* The thevenins equivalent circuits from Drain to ground and from source to ground of fet amplifiers consists of two generators in series
→ one with $-\mu$ times the gate signal voltage 'V_i' and second with $(\mu+1)$ times of ~~source~~volt source voltage V_S and the Resistance $r_d + (\mu+1) R_S$.

(where $\mu = g_m \cdot r_d$).

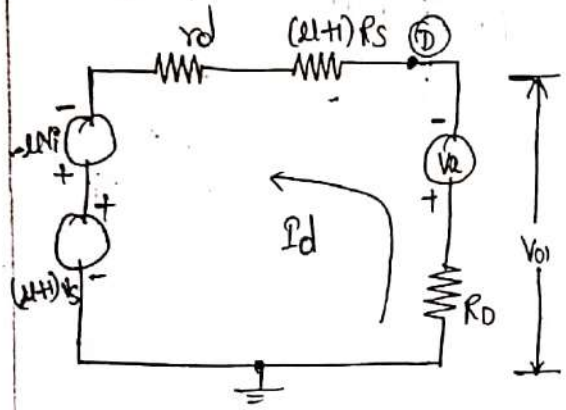

fig: Looking into the Drain

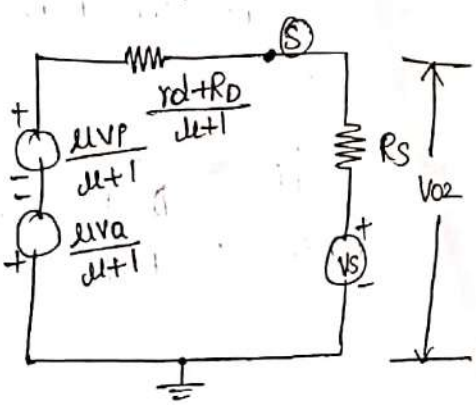

fig: Looking into the Source.

i) common source (CS) Amplifier

for CS-Amplifier $V_S = 0$, $V_a = 0$

input → V_i
output → V_{01}

voltage gain $A_V = \frac{V_{01}}{V_i} = \frac{-\mu R_D}{r_d + (\mu+1) R_S + R_D} = \frac{-g_m r_d \cdot R_D}{r_d + (g_m r_d + 1) R_S + R_D}$

Dividing above eq'n by r_d

$$A_V = \frac{-g_m R_D}{1 + g_m R_S + \frac{R_S + R_D}{r_d}}$$

If $r_d \gg (R_S + R_D)$

$$A_V = \frac{-g_m R_D}{1 + g_m R_S}$$

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Output Resistance (R_o):-

Looking into the drain

$$R_o = r_{ol} + (\mu+1) R_{S_1}$$

The net resistance R_o' taking 'R_D' into account

$$R_o' = R_o \| R_D$$

Thus the presence of R_S Reduces the voltage gain and increases the output Resistance.

Common Gate (CG) Amplifier:-

for CG Amplifier $V_i = 0$ & $V_a = 0$

Input → V_S

output → V_{o1}

$$A_V = \frac{V_{o1}}{V_S} = \frac{(\mu+1) R_D}{r_d + (\mu+1) R_S + R_D} = \frac{(g_m r_d + 1) R_D}{r_d + (g_m r_d + 1) R_S + R_D}$$

Dividing the above eq'n w.r.to r_{ol}

$$A_V = \frac{\left(g_m + \frac{1}{r_d}\right) R_D}{1 + g_m R_S + \left(\frac{R_S + R_D}{r_d}\right)}$$

If $g_m \gg \frac{1}{r_d}$ & $r_{ol} \gg (R_S + R_D)$

$$A_V = \frac{g_m R_D}{1 + g_m R_S}$$

* A_V is positive, there is no phase shift between input and output

* The amplification factor is approximately same as for CS amplifier with $R_S \neq 0$.

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(22)

Input Resistance (R_i'):- $R_i' = \frac{r_{od} + R_D}{\mu + 1}$

$R_i' = R_i' \| R_S \Rightarrow R_i' = \left(\frac{r_d + R_D}{g_m r_d + 1}\right) \| R_S$.

output Resistance. (R_o):-

$R_o = r_d + (\mu + 1) R_S$

$R_o' = R_o \| R_D \Rightarrow R_o' = [r_d + (g_m r_d + 1) R_S] \| R_D$

* The CG amplifier has low input Resistance and high output Resistance.

Common Drain (CD) Amplifier:-

for CD Amplifier $V_S = 0$ & $V_a = 0$ and $R_D = 0$ Input $\rightarrow V_i$ Output $\rightarrow V_{o2}$

voltage gain $A_V = \frac{V_{o2}}{V_i} = \frac{\mu R_S / (\mu + 1)}{r_d / (\mu + 1) + R_S} \Rightarrow \frac{\mu R_S}{r_d + (\mu + 1) R_S}$

$A_V = \frac{g_m r_d R_S}{r_d + (g_m r_d + 1) R_S}$

Divide above eq'n w.r.to r_d

$A_V = \frac{g_m R_S}{1 + (g_m R_S) + \frac{R_S}{r_d}}$

If $r_d \gg R_S$, then $A_V = \frac{g_m R_S}{1 + g_m R_S}$.

If $g_m R_S \gg 1$ then $A_V = 1$ but it is always less than '1'.

*The output impedance of source follower at lower frequencies with $R_D = 0$ $R_o = \frac{r_d}{\mu + 1} \Rightarrow \frac{r_d}{g_m r_d + 1}$

$\div r_d \Rightarrow \boxed{R_o = \frac{1}{g_m + \left(\frac{1}{r_d}\right)}}$ If r_d is greater then $R_o = 1/g_m$

$\boxed{R_o' = R_o \| R_S \Rightarrow \frac{1}{g_m} \| R_S}$.

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FORMULAES FOR EXACT ANALYSIS:

1. Current Gain $A_I = \frac{h_f}{1+h_o Z_L}$

2. Current gain with Source resistor

$$A_{IS} = \frac{A_I R_S}{Z_i + R_S}$$

3. Input Impedance $Z_i = h_i + h_r A_I R_L$

$$= h_i - \frac{h_f h_r}{h_o + Y_L}$$

4. Voltage gain $A_V = \frac{A_I R_L}{Z_i}$

5. Voltage gain with Source resistance $A_{VS} = \frac{A_V R_i}{Z_i + R_S}$

$$A_{VS} = \frac{A_i R_L}{Z_i + R_S} = \frac{A_{is} R_L}{R_S}$$

6. Output Admittance $Y_o = h_o - \frac{h_f h_r}{h_i + R_S}$

$$Z_o = \frac{1}{Y_o} = \frac{h_i + R_S}{h_o(h_i + R_S) - h_f h_r}$$

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CONVERSION TABLE FOR H - PARAMETERS

	CB	CC
CE	$h_{ie} = \frac{h_{ib}}{1+h_{fb}}$ $h_{fe} = \frac{-h_{fb}}{1+h_{fb}}$ $h_{re} = \frac{h_{ib}h_{ob}}{1+h_{fb}} - h_{rb}$ $h_{oe} = \frac{h_{ob}}{1+h_{fb}}$	$h_{ie} = h_{ic}$ $h_{fe} = -(1+h_{fc})$ $h_{re} = 1 - h_{rc}$ $h_{oe} = h_{oc}$
	CE	CC
CB	$h_{ib} = \frac{h_{ie}}{1+h_{fe}}$ $h_{rb} = \frac{h_{ie}h_{oe}}{1+h_{fe}} - h_{re}$ $h_{fb} = \frac{-h_{fe}}{1+h_{fe}}$ $h_{ob} = \frac{h_{oe}}{1+h_{fe}}$	$h_{ib} = \frac{-h_{ic}}{h_{fc}}$ $h_{ib} = h_{fc} - \frac{h_{ic}h_{oc}}{h_{fc}} - 1$ $h_{fb} = -\frac{1+h_{fc}}{h_{fc}}$ $h_{ob} = -\frac{h_{oc}}{h_{fc}}$

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	CE	CB
CC	$h_{ic} = h_{ie}$	$h_{ic} = \frac{h_{ib}}{1+h_{fb}}$
	$h_{rc} = 1 - h_{re} \approx 1$	$h_{rc} = 1$
	$h_{fc} = -(1+h_{fe})$	$h_{fc} = \frac{-1}{1+h_{fb}}$
	$h_{oc} = h_{oe}$	$h_{oc} = \frac{h_{ob}}{1+h_{fb}}$

FORMULAES FOR APPROXIMATE ANALYSIS

CE CONFIGURATION

1) $A_I = -h_{fe}$

2) $R_i = h_{ie}$

3) $A_V = \frac{A_I R_L}{R_i}$

4) $Y_o = 0$ & $R_o = \infty$

CB CONFIGURATION

1) $A_I = \frac{h_{fe}}{1+h_{fe}} = -h_{fb}$

2) $R_i = \frac{h_{ie}}{1+h_{fe}} = h_{ib}$

3) $A_V = \frac{h_{fe} R_L}{h_{ie}}$

4) $R_o = \infty$ $Y_o = 0$

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FOR CC CONFIGURATION

1) $A_I = 1 + h_{fe}$

2) $R_i = h_{ie} + (1 + h_{fe}) R_L$

3) $A_V = 1$

4) $R_O = \frac{R_S + h_{ie}}{1 + h_{fe}}$

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PROBLEMS

1- A CE Amplifier is driven by a voltage source of internal resistance $R_S = 800\Omega$ and the load impedance is a Resistance $R_L = 1000\Omega$. The h-parameters are $h_{ie} = 1K\Omega$, $h_{re} = 2\times10^{-4}$, $h_{fe} = 50$ and $h_{oe} = 25\mu A/V$. Compute the current gain, input resistance, voltage gain A_V and output resistance R_o using exact analysis and using Approximate analysis?

Sol

Given data $R_S = 800\Omega$

Load Impedance is $R_L = 1000\Omega$

H-parameters $h_{ie} = 1K\Omega$

$h_{re} = 2\times10^{-4}$

$h_{fe} = 50$

$h_{oe} = 25\mu A/V$

find Current gain $A_I = ?$

Input Resistance $R_i = ?$

Voltage Gain $A_V = ?$

output Resistance $R_o = ?$

EXACT ANALYSIS :

Current gain $\boxed{A_I = \frac{-h_{fe}}{1 + h_{oe} R_L}}$

$$A_I = \frac{50}{1 + 25\times1000\times10^{-6}} = \frac{50}{1 + 25\times10^{-3}}$$

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$$A_I = \frac{-50}{1.0250}$$

$$\boxed{A_I = -48.78}$$

2. Input Resistance $R_i = h_{ie} - \frac{h_{fe} h_{re}}{h_{oe} + \frac{1}{R_L}}$

$$R_i = 1000 - \frac{50 \times 2 \times 10^{-4}}{25 \times 10^{-6} + \frac{1}{1000}}$$

$$= 1000 - \frac{100 \times 10^{-4}}{25 \times 10^{-6} + 10^{-3}}$$

$$= 1000 - 9.7561$$

$$\boxed{R_i = 990.2439\ \Omega}$$

3. Voltage Gain $A_V = \frac{A_I R_L}{R_i}$

$$= (-48.78) \times \frac{1000}{990.243}$$

$$= (-48.78) \times 1.00985$$

$$= -(48.78) \times 1.00985$$

$$\boxed{A_V = -49.26}$$

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3. $A_V = \frac{-h_{fe} R_L}{h_{ie}}$

$= -\frac{50 \times 1000}{1000}$

$\boxed{A_V = -50}$

4. $R_O = \infty$

2. A voltage source with Internal Resistance $R_S = 900\Omega$ drives a CE amplifier using load resistance $R_L = 2000\Omega$. The CE H-parameters are $h_{ie} = 1200\Omega$, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 60$, $h_{oe} = 25\mu A/V$. Compute the current gain A_I, the input impedance R_I, voltage gain A_V, and output resistance R_O using approximate analysis and exact analysis?

Sol

Given data

Internal Resistance $R_S = 900\Omega$

Load Resistance $R_L = 2000\Omega$

Given CE H-parameters

$h_{ie} = 1200\Omega$

$h_{re} = 2 \times 10^{-4}$

$h_{fe} = 60$

$h_{oe} = 25\mu A/V$

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4. Output Resistance R_o = ?

$$Y_o = h_{oc} - \frac{h_{fc}h_{rc}}{h_{ie}+R_s}$$

$$= 25\times10^{-6} - \frac{50 * 2\times10^{-4}}{1000 + 800}$$

$$= 10^{-4}\left[25\times10^{-2} - \frac{100}{1800}\right]$$

$$= 10^{-4} * 0.1944$$

$$Y_o = 1.944 \times 10^{-5} \text{ mhos}$$

$$R_o = \frac{1}{Y_o} = \frac{1}{1.944\times10^{-5}}$$

$$= 0.5144 \times 10^{5}$$

$$\boxed{R_o = 51.44\ k\Omega}$$

APPROXIMATE ANALYSIS:

1) $A_I = -h_{fe}$

$$\boxed{A_I = -50}$$

2) $R_i = h_{ie}$

$$\boxed{R_i = 1k\Omega}$$

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$$A_V = 0.9898$$

4) $$R_o = \frac{1}{Y_o}$$

$$Y_o = h_{oc} - \frac{h_{fc} h_{rc}}{h_{ic} + R_S}$$

$$= 25 \times 10^{-6} - \frac{(-61)(1)}{(1200) + 800)}$$

$$= 25 \times 10^{-6} + 0.0290$$

$$Y_o = 0.0290 \text{ mhos}$$

$$R_o = \frac{1}{Y_o}$$

$$= \frac{1}{0.0290}$$

$$R_o = 34.4828 \Omega$$

APPROXIMATE ANALYSIS

1) Current gain $A_I = 1 + h_{fe}$

$$= 1 + 60$$

$$A_I = 61$$

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Find $A_I = ?$, $R_i = ?$, $A_V = ?$ $R_O = ?$

CONVERSION FORMULA

$h_{fc} = -(1+h_{fe}) = -(1+60) = -61$

$h_{rc} = 1$

$h_{fc} = h_{ic} = 1200\,\Omega$

$h_{oc} = h_{oe} = 25\,\mu A/V$

EXACT ANALYIS:

1) $A_I = \dfrac{-h_{fc}}{1+h_{oc}R_L}$

$= \left[\dfrac{-(-61)}{1+25\times10^{-6}\times2000}\right] = \dfrac{61}{1.0500}$

$\boxed{A_I = 58.095}$

2) $R_i = h_{ic} + h_{rc}A_I R_L$

$= 1200 + (1)*(58.095)*(2000)$

$= 117390\,\Omega$

$\boxed{R_i = 117.39\,K\Omega}$

3) $A_V = \dfrac{A_I R_L}{R_i}$

$= \dfrac{(58.095)*2000}{117.39\times10^3}$

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2. $R_i = h_{ie} + (1+h_{fe})R_L$

$= 1200 + (1+60)2000$

$= 12,3200$

$\boxed{R_i = 123.2\,k\Omega}$

3. Voltage Gain $A_V = 1$

4. Output resistance $R_o = \dfrac{h_{ie} + R_S}{1+h_{fe}}$

$= \dfrac{1200+900}{1+60}$

$\boxed{R_o = 34.426\,\Omega}$

3. FOR A CB transistor amplifier driven by a voltage source of internal resistance $R_S = 1200\,\Omega$, the load impedance is a resistor $R_L = 1000\,\Omega$. The h-parameters are $h_{ib} = 22\,\Omega$, $h_{rb} = 3\times10^{-4}$, $h_{fb} = -0.98$ and $h_{ob} = 0.5\,\mu A/V$. Compute the current gain A_I, the i/p impedance R_i, Voltage gain A_V, Overall Voltage gain A_{VS}, overall current gain A_{IS}, o/p impedance Z_o and power gain A_P using exact analysis and Approximate analysis?

Scanned by CamScanner

Sol

Given data $R_S = 1200\,\Omega$

$R_L = 1000\,\Omega$

$h_{ib} = 22\,\Omega$

$h_{rb} = 3\times10^{-4}$

$h_{fb} = -0.98$

$h_{ob} = 0.5\,\mu A/V$

$A_I = ?$ $R_i = ?$, $A_V = ?$ $A_{VS} = ?$

$A_{IS} = ?$ $Z_o = ?$ $A_P = ?$

EXACT ANALYSIS

1. $$A_I = \frac{-h_{fb}}{1+h_{ob}R_L}$$

$$= \frac{-(-0.98)}{1+0.25\times10^{-6}\times1000}$$

$$= \frac{0.98}{1.0005}$$

$$\boxed{A_I = 0.98}$$

2. $$R_i = h_{ib} + h_{rb}A_I R_L$$

$$= 22 + (3\times10^{-4})(0.98)(1000)$$

$$\boxed{R_i = 22.3\,\Omega}$$

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$$= 10^{-6}\left(0.5 - \frac{98\times 3}{22+1200}\right)$$

$$= 10^{-6}(0.5 - 0.2406)$$

$$\boxed{Y_o = 0.2594\times 10^{-6} \text{ mhos}}$$

$$R_o = \frac{1}{Y_o}$$

$$= \frac{1}{0.2594\times 10^{-6}}$$

$$\boxed{R_o = 3.8551\ M\Omega}$$

7) Power gain $A_p = A_v A_I$.

$$= 0.98 \times 43.946$$

$$\boxed{A_p = 43.06}$$

APPROXIMATE ANALYSIS:

Current gain $A_I = -h_{fb} = 0.98$

$$R_i = h_{ib} = 22\Omega$$

$$A_v = \frac{A_I R_L}{h_{ie}}$$

$\because h_{ie} = (1+h_{fe})h_{ib}$

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3) $A_V = \frac{A_I R_L}{R_i}$

$= \frac{0.98 \times 1000}{22.3}$

$\boxed{A_V = 43.946}$

4) Overall Voltage gain $A_{VS} = \frac{A_V R_i}{R_i + R_S}$

$= \frac{43.946 \times 22.3}{22.3 + 1200}$

$\boxed{A_{VS} = 0.802}$

5) Overall Current gain $A_{IS} = \frac{A_I R_S}{R_S + R_i}$

$= \frac{0.98 \times 1200}{1200 + 22.3}$

$\boxed{A_{IS} = 0.962}$

6) Output Admittance $Y_0 = h_{ob} - \frac{h_{fb} h_{rb}}{h_{ib} + R_S}$

$= 0.5 \times 10^{-6} - \frac{(0.98)(3 \times 10^{-4})}{22 + 1200}$

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$A_V = 64.54$

4. Output impedance $R_o = \infty$

5. Overall voltage gain $A_{VS} = \frac{A_V \cdot R_i}{R_i + R_S}$

$= \frac{64.54 * 22}{22 + 1200}$

$A_{VS} = 0.802$

6. Overall current gain $A_{IS} = \frac{A_I \cdot R_S}{R_i + R_S}$

$= \frac{0.98 \times 1200}{22 + 1200}$

$A_{IS} = 0.9624$

7. Power gain $A_p = A_V * A_I$

$= 64.54 * 0.98$

$A_p = 63.65$

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$$h_{fb} = \frac{-h_{fe}}{1+h_{fe}}$$

$$h_{fb}(1+h_{fe}) = -h_{fe}$$

$$h_{fb} + h_{fb}h_{fe} + h_{fe} = 0$$

$$h_{fb} + h_{fe}(1+h_{fb}) = 0$$

$$h_{fe} = \frac{-h_{fb}}{1+h_{fb}}$$

$$h_{fe} = \frac{-(-0.98)}{1-0.98} \cdot (\because \text{from given data } h_{fb} = 0.98)$$

$$h_{fe} = \frac{0.98}{0.020}$$

$$h_{fe} = 49$$

$$\therefore h_{ie} = (1+h_{fe})\, h_{ib}$$

$$= (1+49)\, 22$$

$$\boxed{h_{ie} = 1100\ \Omega}$$

$$A_V = \frac{h_{fe}}{h_{ie}} R_L$$

$$= \frac{49 \times 1000}{1100}$$

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1) Current gain $A_I = \frac{-h_{fb}}{1+h_{ob}R_L'}$

$$= \frac{-0.98}{1+(0.69\times10^{-6}\times6.46\times10^{3})}$$

$$\boxed{A_I = 0.977}$$

2) Input Impedance $R_i = h_{ib} + h_{rb} A_I R_L'$

$$= 24 + 2.9\times10^{-4} \times 0.977 \times 6.46\times10^{3}$$

$$= 24 + 1.8303$$

$$\boxed{R_i = 24.8303\ \Omega}$$

3) Voltage gain $A_V = \frac{A_I R_L'}{R_i}$

$$= \frac{(0.977)(6.46\times10^{3})}{25.83}$$

$$\boxed{A_V = 244.34}$$

4) Output resistance R_o:

$$Y_o = h_{ob} - \frac{h_{fb}h_{rb}}{h_{ib}+R_s'}$$

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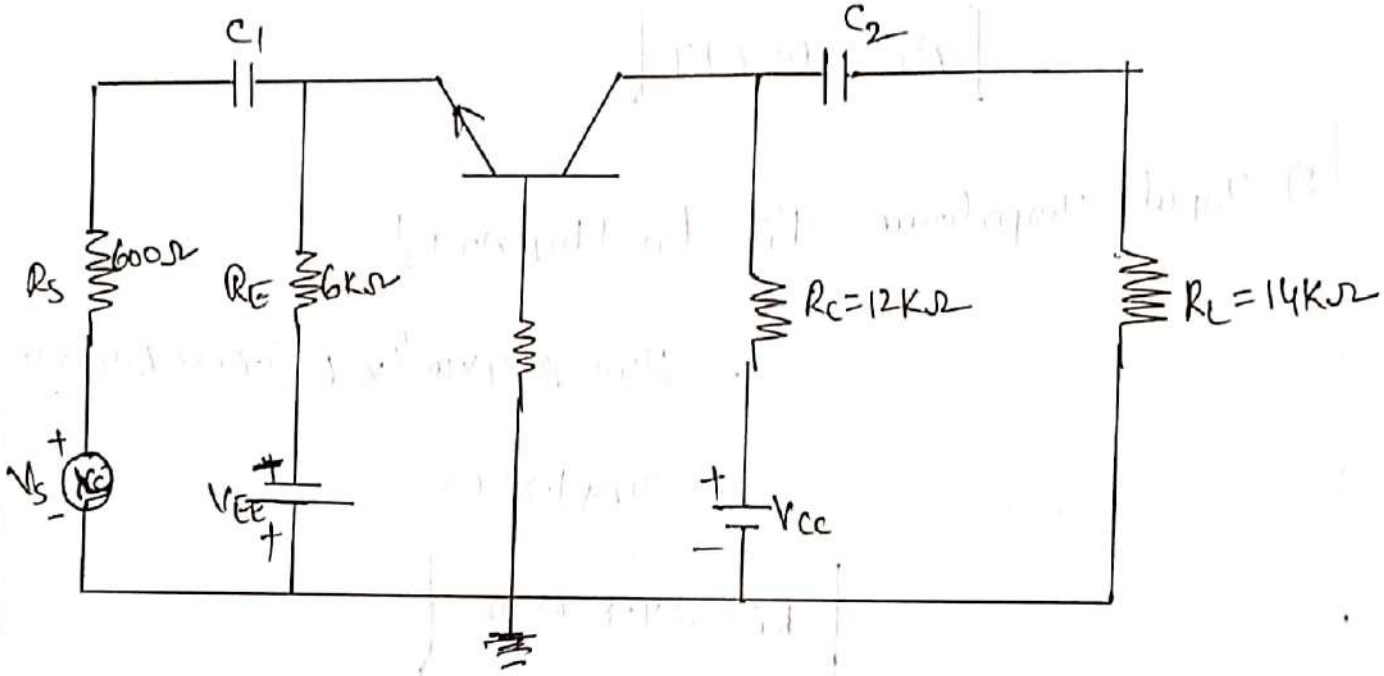
4. Calculate the values of I/p resistance, output resistance, 9
Current gain, voltage gain for the common base amplifier circuit shown in the figure. The transistor parameters are

$h_{ib} = 24\Omega$, $h_{fb} = 0.98$, $h_{ob} = 0.49\ \mu A/V$, $h_{rb} = 2.9 \times 10^{-4}$.



Sol

From the figure,

$R_S = 600\Omega$

$R_E = 6K\Omega$

$R_C = 12K\Omega$

$R_L = 14K\Omega$

Given data

$h_{ib} = 24\Omega$

$h_{fb} = 0.98$

$h_{ob} = 0.49\ \mu A/V$

$h_{rb} = 2.9 \times 10^{-4}$

Where load resistance is $R_C \| R_L$

$$R_L' = \frac{R_C R_L}{R_C + R_L}$$

$$\boxed{R_L' = 6.46K\Omega}$$

Source resistance is $R_S \| R_E$

$$R_S' = \frac{R_S R_E}{R_S + R_E}$$

$$R_S' = 545.45\Omega$$

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$$Y_0 = 0.49 \times 10^{-6} - \frac{(-0.98)(2.9 \times 10^{-4})}{24 + 545.45}$$

$$= 0.989 \times 10^{-6} \text{ mho}$$

$$R_0 = \frac{1}{Y_0}$$

$$= \frac{1}{0.989 \times 10^{-6}}$$

$$\boxed{R_0 = 1.011 \text{ M}\Omega}$$

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JFET Small-Signal Model :-

From the drain & transfer characteristics of the JFET & MOSFET the drain current of an FET is a function of drain to source voltage (V_{DS}) & Gate to source voltage (V_{GS}). Assuming varying currents & voltages for an FET

$$i_D = f(V_{GS}, V_{DS}) \rightarrow (1)$$

if both gate & drain voltages are varied, the change in drain current is given approximately by first two terms in the Taylor's series expansion as

$$\Delta i_D = \left(\frac{\partial i_D}{\partial V_{GS}}\right)_{V_{DS}} \Delta V_{GS} + \left(\frac{\partial i_D}{\partial V_{DS}}\right)_{V_{GS}} \Delta V_{DS} \rightarrow (2)$$

To derive for change of drain current, derivate

Two or more than two variables then use partial derivative.

From small signal notation as for BJT

$$\Delta i_d = i_d \; ; \; \Delta V_{GS} = V_{gs} \; ; \; \Delta V_{DS} = V_{ds}$$

So eq (2) can be written as $i_d = \frac{\partial i_D}{\partial V_{GS}}\Big|_{V_{DS}} V_{gs} + \frac{\partial i_D}{\partial V_{DS}}\Big|_{V_{GS}} V_{ds}$

from ohm's law $i_d = g_m V_{gs} + \frac{1}{r_d} V_{ds} \rightarrow (3)$ in small signal.

For complete differential multiply with ΔV_{GS} → partial & complete differential are used here

admittance/conductance or mutual conductance or trans conductance or CS forward transadmittance

where mutual conductance or transconductance of the FET is defined as

$$g_m = \left(\frac{\partial i_D}{\partial V_{GS}}\right)_{V_{DS}} \simeq \left(\frac{\Delta i_D}{\Delta V_{GS}}\right)_{V_{DS}} = \left(\frac{i_d}{V_{gs}}\right)_{V_{DS}} \rightarrow (4)$$

$\because \frac{\partial i_d}{\partial V_{DS}}$

$\frac{1}{r_d} = g_d$

The drain resistance of FET is defined as

$$r_d = \left(\frac{\partial V_{DS}}{\partial i_D}\right)_{V_{GS}} \simeq \left(\frac{\Delta V_{DS}}{\Delta i_D}\right)_{V_{GS}} = \left(\frac{V_{ds}}{i_d}\right)_{V_{GS}} \rightarrow (5)$$

The amplification factor μ for an FET may be defined as

$$\mu = \left(-\frac{\partial V_{DS}}{\partial V_{GS}}\right)_{I_D} = \left[-\frac{\Delta V_{DS}}{\Delta V_{GS}}\right]_{I_D} = \left[-\frac{V_{ds}}{V_{gs}}\right]_{i_d = 0}$$

The low frequency model of FET has a norton's output circuit with a dependent current generator whose magnitude is proportional to V_{gs}. The o/p resistance is r_d;

$\frac{1}{r_d} = g_d$ → drain resistance (or) dp resistance (or) Common source o/p conductance (or) transadmittance.

$\mu = \frac{\partial V_{DS}}{\partial i_D}\Big|_{V_{GS}} = \frac{\Delta V_{DS}}{\Delta i_D}\Big|_{V_{GS}} = \frac{V_{ds}}{i_d}\Big|_{V_{gs}}$

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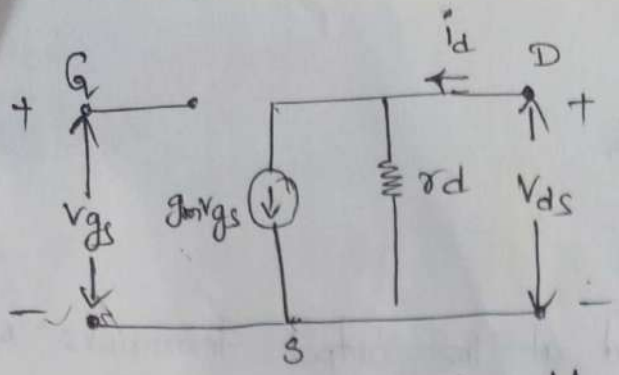
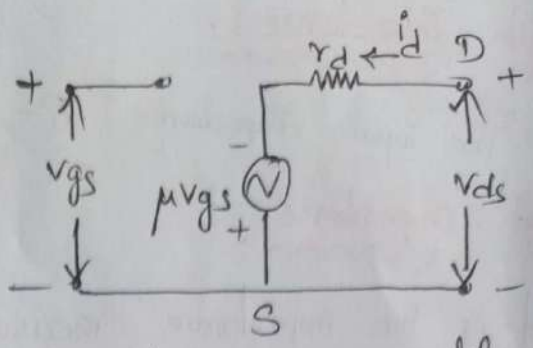
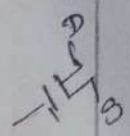


(a) Small signal current model



(b) Voltage - source model.



$g_m V_{gs}$ = V/g dependent current source

The small signal models for the common source FET can be used for analyzing the three basic FET amplifier configurations

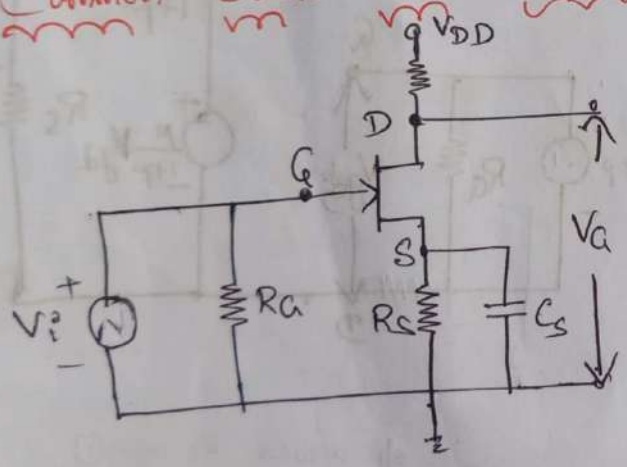
entire is depends on $g_m V_{gs} + \frac{1}{r_d} V_{ds}$

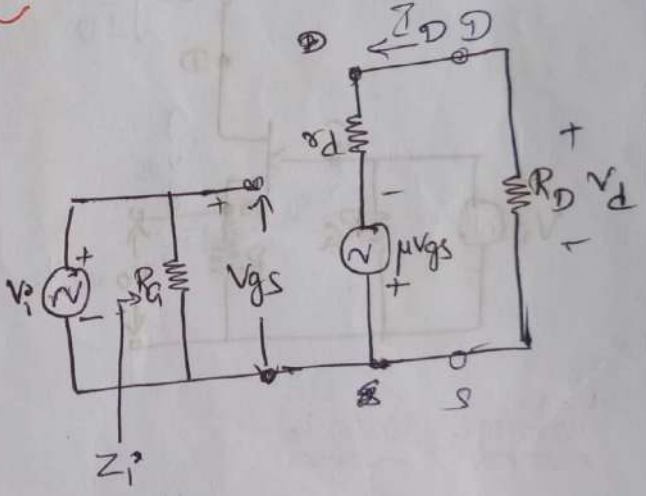
(i) Common Source (CS)

(ii) Common Drain (CD) or Source-follower

(iii) Common Gate (CG)

Common Source (CS) Amplifier:





Voltage gain:

Source resistor (R_S) is used to set the Q point but it is bypassed by C_S for mid-frequency operation.

$$V_o = \frac{-R_D}{R_D + r_d} \mu V_{gs}$$

where $V_{gs} = V_i$

$$A_V = \frac{V_o}{V_i} = \frac{-\mu R_D}{R_D + r_d}$$

Output impedance

$$A_V = \frac{V_{ds}}{V_{gs}} = \frac{V_{ds}}{V_i}$$

V_{ds} = applied voltage at o/p × resistance / Total resistance (by voltage division rule)

$$V_{ds} = \frac{-\mu V_{gs} R_D}{R_D + R_D}$$

$-\mu V_{gs}$ is opposite to i_d so (−) sign

$$A_V = \frac{V_o}{V_i} = \frac{\frac{-\mu R_D V_{gs}}{R_D + r_d}}{V_{gs}} \times \frac{1}{1} = \frac{-\mu R_D V_{gs}}{R_D + r_d} \times \frac{1}{V_{gs}}$$

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input impedance :

The input impedance $Z_i = R_G$

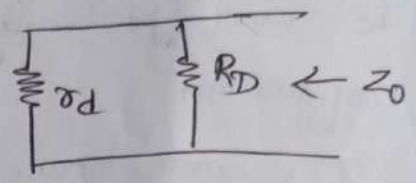
output impedance :

It is the impedance measured at the output terminals with input voltage $V_i = 0$; So $V_{gs} = 0$ & hence $\mu V_{gs} = 0$.

The equivalent circuit has an output impedance of $Z_o = r_d \| R_D$.

Normally r_d will be far greater than R_D ($r_d = 35\,k\Omega$ & $R_D = 5\,k\Omega$)

Hence $Z_o \simeq R_D$



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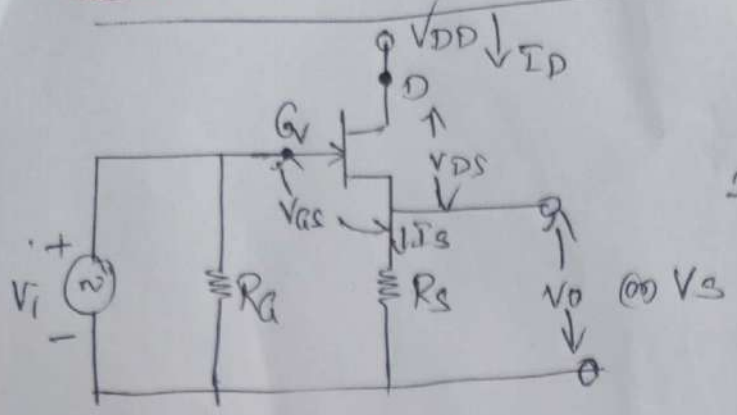
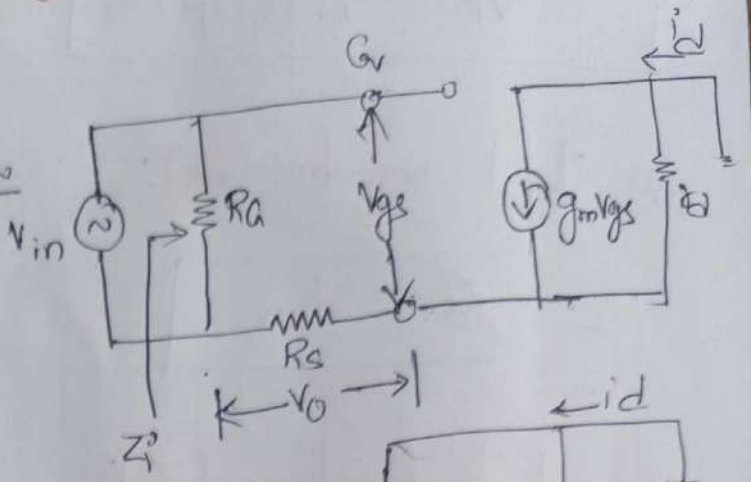
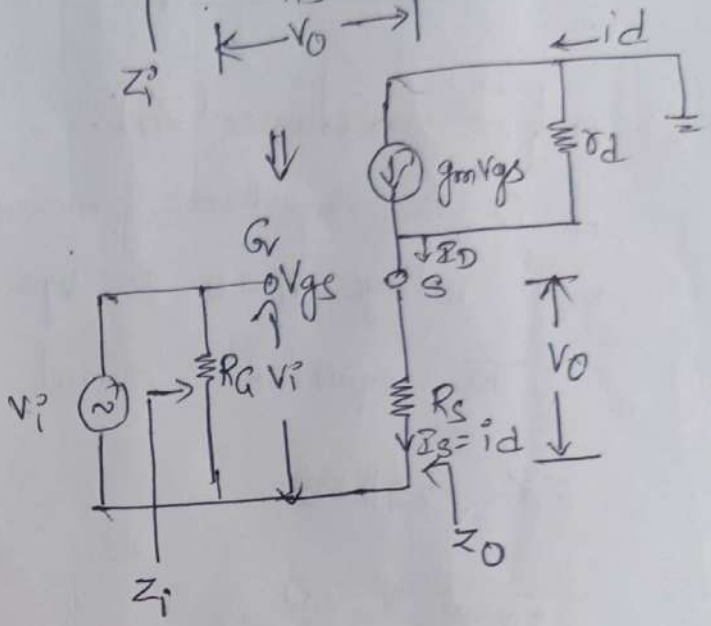
Common Drain (CD) Amplifier (or) Source follower







Voltage gain (Av):

Applying KVL at input side circuit

$$V_i = V_{gs} + i_d R_S$$

$$V_{gs} = V_i - i_d R_S \longrightarrow (1)$$

Applying KVL at output side circuit

$$0 = i_d R_S + (i_d - g_m V_{gs}) r_d$$

$$i_d R_S + i_d r_d - g_m V_{gs} r_d = 0$$

$$i_d R_S + i_d r_d - g_m (V_i - i_d R_S) r_d = 0$$

$$i_d R_S + i_d r_d - g_m V_i r_d + g_m i_d R_S r_d = 0$$

$$i_d R_S + i_d r_d - \mu V_i + \mu i_d R_S = 0$$

$$i_d (R_S + r_d + \mu R_S) = \mu V_i$$

$$i_d = \frac{\mu V_i}{R_S + r_d + \mu R_S}$$

$\because g_m r_d = \mu$

From the circuit:

$$V_o = i_d R_S$$

$$V_o = \frac{\mu V_i R_S}{R_S + r_d + \mu R_S}$$

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$$A_V = \frac{V_o}{V_i} = \frac{\mu R_S}{r_d + (1+\mu) R_S}$$

(2) Input impedance (Z_i):-

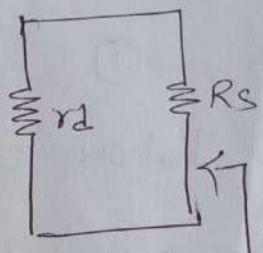
$$Z_i = R_G$$

(3) Output impedance (Z_o):-

If R_S the impedance measured at the output terminals with input voltage $V_i = 0$ so, $V_{gs} = 0$ & hence $\mu V_{gs} = 0$

The equivalent circuit has an output impedance of Z_o

$Z_o = r_d \| R_S$

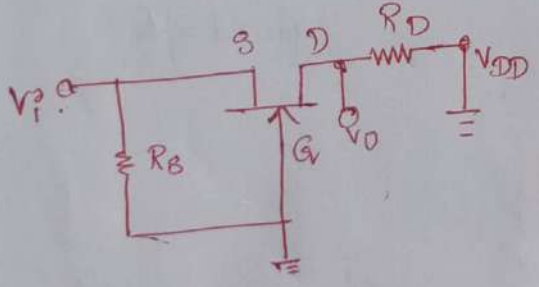


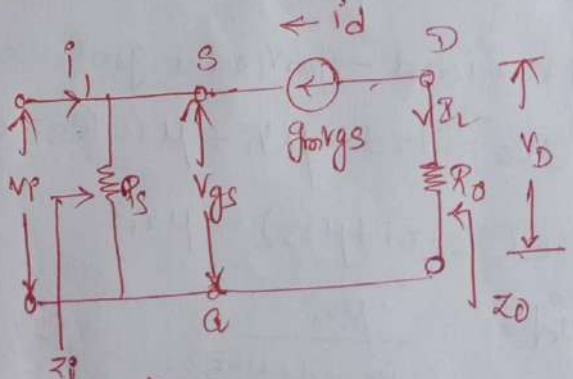
Z_o at $V_i = 0$

$$Z_o = r_d \| R_S$$

NOTE:- The common drain (or) source follower circuit is able to provide a very high input impedance and low output impedance and is used to act as a buffer amplifier

Common Gate (CG) Amplifier:-





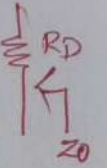
(1) Input impedance: $Z_i = \frac{V_i}{i_i} = \frac{V_{gs}}{-g_m V_{gs}} \Rightarrow Z_i = \frac{1}{g_m}$

but - sign is not consider in impedance

(2) Output impedance (Z_o):-

Z_o at $V_i = 0$ $V_{gs} = 0$

$$Z_o = R_D$$



(3) Voltage gain (A_V):-

$$A_V = \frac{V_o}{V_i} = \frac{-i_d R_D}{V_{gs}} = -\frac{g_m V_{gs} R_D}{V_{gs}} \Rightarrow A_V = g_m R_D$$

$V_o = -i_d R_D$ (or) $V_i = V_{gs}$

$i_d = g_m V_{gs}$

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(Q) A CE amplifier has the h-parameters given by $h_{ie} = 1000\,\Omega$, $h_{re} = 2\times10^{-4}$, $h_{fe} = 50$ & $h_{oe} = 25\,\mu$mho. If both the load & source resistances are 1kΩ, determine the (a) current gain and (b) voltage gain.

Given $R_S = 1k\Omega$ and $R_L = 1k\Omega$

$h_{ie} = 1000\Omega$, $h_{re} = 2\times10^{-4}$, $h_{fe} = 50$ & $h_{oe} = 25\,\mu$mho.

(a) Current gain $A_i = \dfrac{h_{fe}}{1+h_{oe}R_L} = \dfrac{50}{1+25\times10^{-6}\times1\times10^{3}} = -48.78$

(b) Voltage gain $A_v = \dfrac{-h_{fe}}{\left[h_{oe}+\frac{1}{R_L}\right]Z_{in}} = \dfrac{-50}{(25\times10^{-6}+1\times10^{-3})\times 990.24} = -49.26$

$\boxed{A_v = -49.26}$

The output voltage is 180° out of phase to the input signal with a gain of 49.26

$\therefore Z_{in} = h_{ie} - \dfrac{h_{re}h_{fe}}{h_{oe}+\frac{1}{R_L}}$ ⇒

$Z_{in} = 1000 - \dfrac{2\times10^{-4}\times50}{25\times10^{-6}\times1\times10^{-3}} = 990.24\,\Omega$

→ A CE amplifier is driven by a voltage source of internal resistance $R_S = 800\Omega$, and the load impedance is a resistance $R_L = 1000\Omega$. The h-parameters are $h_{ie} = 1k\Omega$, $h_{re} = 2\times10^{-4}$, $h_{fe} = 50$ & $h_{oe} = 25\,\mu A/V$. Compute the current gain A_I, input resistance R_i, voltage gain A_v and output resistance R_o using exact analysis & using approximate analysis.

Solution:

Exact analysis

(1) Current gain $A_i = \dfrac{-h_{fe}}{1+h_{oe}R_L} = \dfrac{-50}{1+25\times10^{-6}\times10^{3}} = -48.78$

(2) Input resistance $R_i = h_{ie} - \dfrac{h_{fe}h_{re}}{h_{oe}+\frac{1}{R_L}} = 1000 - \dfrac{50\times2\times10^{-4}}{25\times10^{-6}+1/1000} = 990.24\,\Omega$

(3) Voltage gain $A_v = \dfrac{A_i R_L'}{R_i} = (-48.78)\times\dfrac{1000}{990.24} = -49.26$

(4) Output resistance R_o :-

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Output resistance R_O :-

$$R_O = \frac{1}{Y_O}$$

$$Y_O = h_{oe} - \frac{h_{fe} h_{re}}{h_{ie} + R_s}$$

$$= 25 \times 10^{-6} - \frac{50 \times 2 \times 10^{-4}}{1000 + 800}$$

$$Y_O = 1.94 \times 10^{-5} \text{ mho}$$

$$\boxed{R_O = 1/Y_O = 51.42 \text{ k}\Omega}$$

Approximate analysis:-

$$A_i = -h_{fe} = -50$$

$$R_i = h_{ie} = 1 \text{k}\Omega$$

$$A_V = \frac{-h_{fe} R_L}{h_{ie}} = \frac{-50 \times 1000}{1000} = -50$$

$$R_O = \infty$$

→ A CB Amplifier is driven by a voltage source of internal resistance $R_s = 1\text{k}\Omega$, The load impedance is $R_L = 1\text{k}\Omega$. The transistor parameters are $h_{ib} = 22\Omega$, $h_{fb} = -0.98$, $h_{rb} = 2.9 \times 10^{-4}$, $h_{ob} = 0.5\mu\text{A/V}$. Compute current gain, voltage gain, input and output impedance of the amplifier.

Given values

$R_s = 1\text{k}\Omega$, $R_L = 1\text{k}\Omega$

$h_{ib} = 22\Omega$ $h_{fb} = -0.98$

$h_{rb} = 2.9 \times 10^{-4}$ $h_{ob} = 0.5\mu\text{A/V}$ → $h_{rb} = 3 \times 10^{-4}$

Calculate A_i, A_v, R_i & R_O

① A_I (Current gain) $= \frac{-h_{fb}}{1 + h_{ob} R_L} = \frac{-(-0.98)}{1 + 0.5 \times 10^{-6} \times 1000} = 0.98$ → $\boxed{A_I = 0.98}$

② Input impedance $R_i = h_{ib} + h_{rb} A_i R_L$

$= 22 + (2.9 \times 10^{-4}) \times 0.98 \times 1000$

$= 22.28\ \Omega$

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Voltage gain :- $A_v = \frac{A_i R_L}{R_i} = \frac{0.98 \times 1000}{22.3\ \Omega} = 43.946$

Current output admittance :- $Y_o = h_{ob} - \frac{h_{fb} h_{rb}}{h_{ib} + R_s} = 0.5 \times 10^{-6} - \frac{(-0.98)(0.9 \times 10^{-4})}{22 + 1000}$

$= 0.7405 \times 10^{-6}$ mhos 7.7808×10^{-7}

$R_o = \frac{1}{Y_o} = 1.28597\ M\Omega$

Approximate Analysis :-

1) Current gain $A_i = -h_{fb} = 0.98$

2) R_i or Z_i $= R_i = h_{ib} = 22\ \Omega$

3) $A_v = \frac{h_{fe} R_L}{h_{ie}} = h_{fb} = \frac{-h_{fe}}{1 + h_{fe}}$ rearranging this equation

$h_{fe} = \frac{-h_{fb}}{1 + h_{fb}}$

$h_{fe} = \frac{-(-0.98)}{1 - 0.98} = 49$

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