UNIT-1
JUNCTION DIODE CHARACTERISTICS

To understand the working of p-n junction diode it is necessary to know the basics of materials (P-type & N-type) and also to understand the how diodes, Transistors, Thyristors and Integrated circuits work, it is necessary to know the basic physics behind the behaviour of Semi-conductor material (Semi-conductor is one of type of Material).

Introduction :-

- The Matter which occupies the Space may be 3 types are Solid, Liquid (or) Gaseous.
- Infact, according to the modern Electron theory, matter is composed of the three fundamental particles, which are invisible to bare Eyes.

These are : particles

- Neutron → uncharged (i.e Electrically neutral in nature processing no charge)
- proton → positively charged ion
- Electron → Negatively charged → Mass of electron is very light almost $\frac{1}{1840}$th the mass of neutron (9.107×10^{-31} kg)

Mass of Neutron & proton is same i.e., 1.675×10^{-27} kg

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ATOM :-

* The atoms have a planetary type of structure according to Bohr model.
* All protons and neutrons are bound together at the centre of an atom - which called "Nucleus", while all the Electrons are moving round the Nucleus.
  So, Nucleus can thought of as a central sun, about which electrons revolve in a particular fashion like the planets.

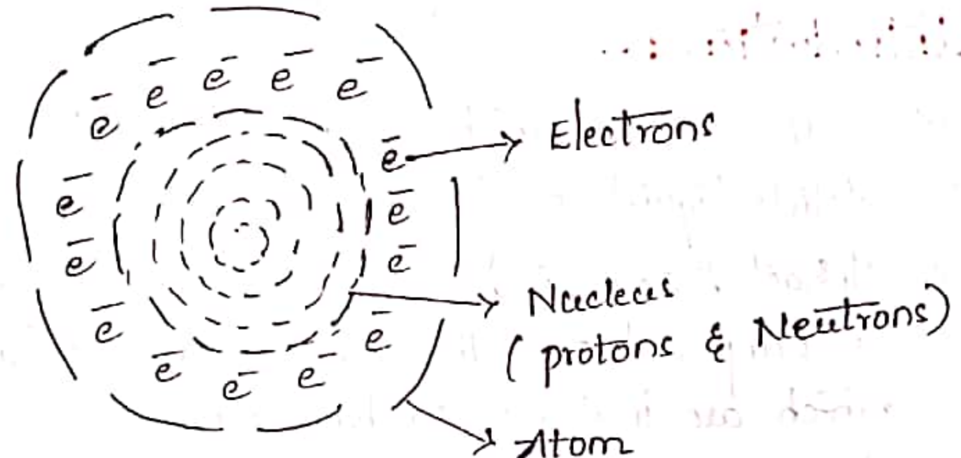
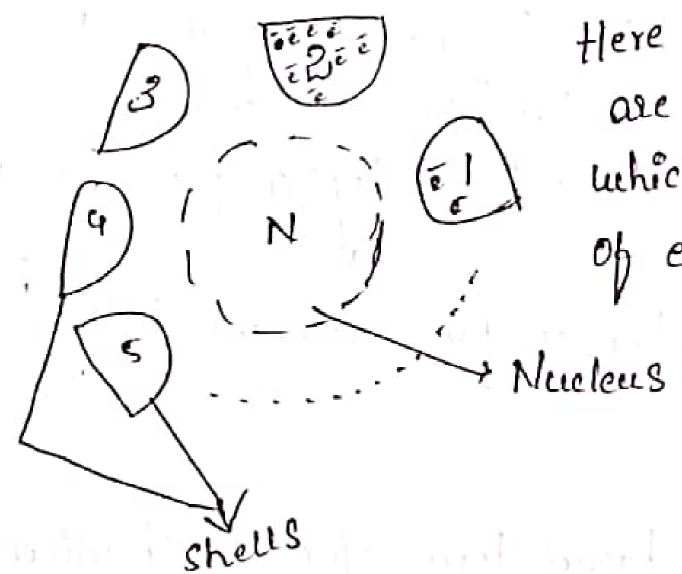


Fig: Structure of an "Atom"

* Atom : Number of electrons = Number of protons
* Atomic Number : Number of protons/electrons in a atom
* Atomic Weight : Total number of protons & Neutrons in Nucleus
* Electrons are moving around over a Nucleus in the form of shells.
* Each shells are having some number of electrons.
* Shell having maximum of "$2n^2$" electrons where, 'n' is a number of shell.
  i.e 1st shell → $2n^2 = 2(1)^2 = 2$ electrons
  2nd shell → $2n^2 = 2(2)^2 = 8$ electrons etc.



Here 1, 2, 3 ..... are shells around nucleus which are having group of electrons.

* Each shell has an Energy level associated with it.

Valence shell & Valence electron :-

The closer of an electron is to the Nucleus, stronger force of attraction, because of closest to the nucleus, while the shell which is farthest (far) from the nucleus is having week force of attraction and the electrons are very loosely bound to the Nucleus. Such electron in the outermost shell are responsible for the electrical & chemical characteristics of an atom.

"The outermost shell is called "Valence shell" and the electrons in the shell are called as "Valence electrons".

* Valence electrons in outermost shell are having "highest Energy level"!

Nucleus
Lowest Energy Shell → Shell - 1
Shell - 2
Shell - N
Energy level increases from 1st to highest shells.
Valence shell (outermost shell of that nucleus)
Valence electrons

fig: concept of Energy level

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Free electron :-

The electron which is not subjected to the "force of attraction" of the nucleus is called "free electron". Such free electrons are basically responsible to the "flow of current".

" More the number of free electrons better is the conductivity of the metal ".

Materials :-

Material is a broad term for a chemical substance (or) mixture of substances that constitute a thing.

** Energy band Theory :-

Shell nearer to Nucleus → having Low energy level

Shell farthest (far) to nucleus → Highest Energy level.

* Due to high energy levels of electrons in outermost shell, electrons can be easily extracted from outermost shell to another orbit of an atom.
* The Valence electrons are shared by forming a bond with the valence electrons of an adjacent atom. Such bonds are called "Covalent bond".
* Now, the valence electrons posses highest energy level when such electrons forms the covalent bonds, due to coupling between the valence electrons, the energy levels associated with the valence electrons merge into each other, this merging forms an "Energy band".

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Energy band :- It describes the ranges/level of Energy bands. The electrons in same orbit exhibits different energy levels. The grouping of this different Energy levels is called "Energy band.

Types of Energy bands :-

1. Valence band
2. Conduction band
3. forbidden band or gap.

Valence band : Energy band formed due to merging of Energy levels associated with the valence electrons is "Valence band".

Conduction band : Energy band formed due to merging of Energy-levels associated with the free-electrons is called "conduction-band".

forbidden band : Energy band which is separating the Conduction band and Valence band is called "forbidden band".

→ In order to push an electron from valence band to conduction band the applied external energy in the form of light/heat must be equal to the forbidden gap.

Energy band diagram :-

Energy

Conduction Band

Valence Band

2nd Band

1st Band

→ forbidden Energy gap (EG)

Edge of nucleus

* Energy associated with forbidden band is called as "Energy gap (Eg) it is measured in the unit electron volt

$1 eV = 1.6 \times 10^{-19} J$

The Graphical representation of the energy band in a solid is called "Energy band diagram".

* For any given type of material the forbidden Energy gap may be large, small (or) Non-exisistent.
* Based on width of forbidden energy gap, the materials are classified into 3-types.

Classification of Materials :-

1. Conductors
2. Insulators
3. Semiconductors

1. **Conductors** :- These are having Large no. of free electrons Exist at room temparature. So E_G (forbidden energy gap) does not Exist. Conduction and Valence bands are Overlapped.

   Ex: Copper, Aluminium, Silver

2. **Insulators** :- No free Electrons. The gap of energy is Very high b/w conduction & Valence band nearly 7ev.

   Ex: Wood, glass, Mica

3. **Semiconductors** :- having few number of free electrons the gap is 1 ev b/w both bands.

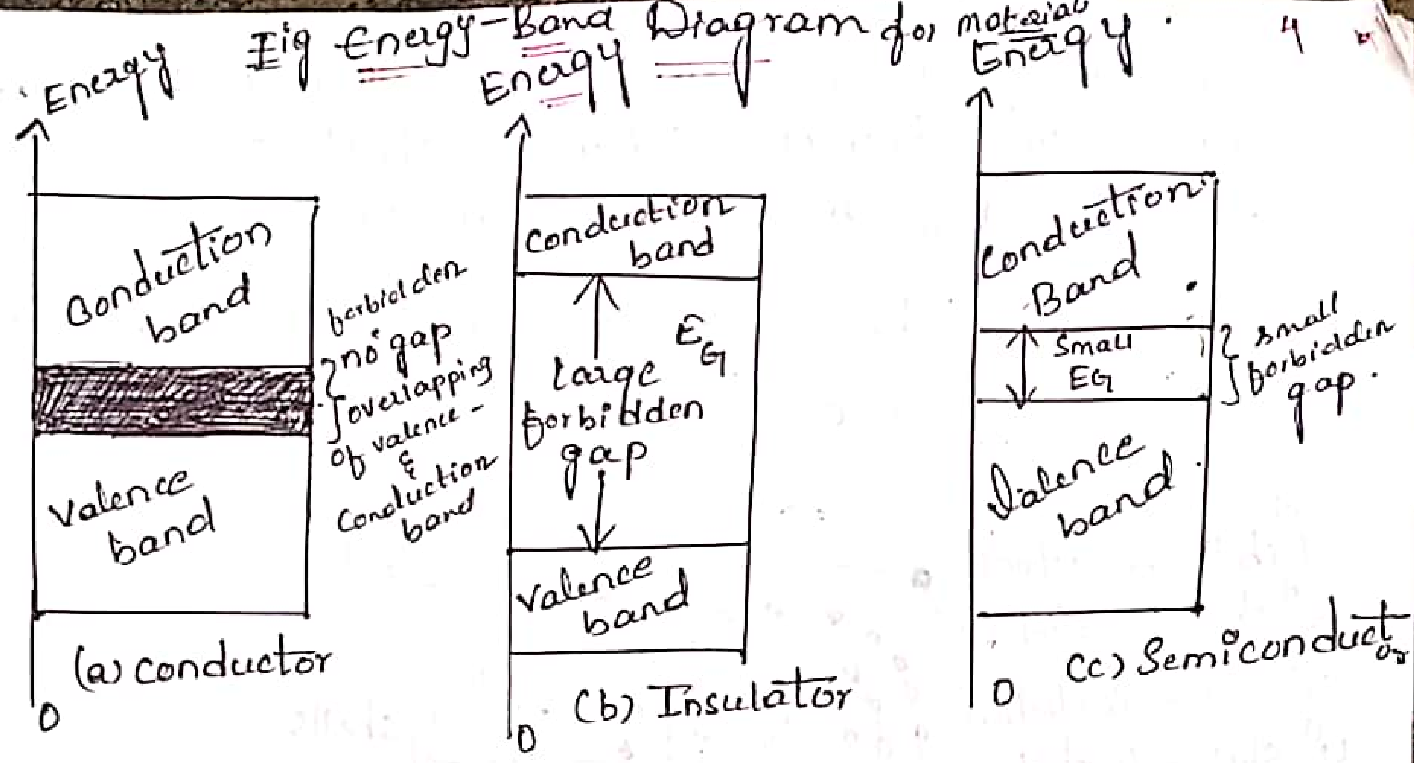
   Ex :- Ge, Si

The charge on a single electron is 1.6×10^{-19} Coulomb So, One electron volt is defined as the energy required by an electron to fall through a potential of one volt.

$$1ev = 1.6 \times 10^{-19} (C) \times 1 (V)$$

$$1ev = 1.6 \times 10^{-19} J$$

Fig Energy-Band Diagram for material



- In our Syllabus, having Semiconductor material we need to know in depth of Semiconductors.)'

** Semiconductors :-

* It is an important category of materials, which are neither insulators nor conductors.
* The forbidden gap in such material is Very Narrow as shown in above figure, nearly gap is "1 ev".
* In such materials (Semiconductors), the energy provided by the heat at room temparature is sufficient to lift the electrons from the Valence band to conduction band. so at room temparature Semiconductors are Capable of conduction. but at 0°K or absolute zero (−273°C), all the Semiconductors are acts as Insulators. Here forbidden gap is depends on temparature.

approx. 1.12 ev at room temp 300°K (27+273)

for Si & Ge
$$E_G = 1.21 - 3.6 \times 10^{-4} \times T \text{ ev } (Si)$$
$$E_G = 0.785 - 2.23 \times 10^{-4} \times T \text{ ev } (Ge)$$
at room temp 0.72 ev

∴ 'T' is Absolute temperature in °K

* Si, Ge are widely used Semiconductor materials in electronic devices.

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* Among Silicon & Germanium, Silicon is most widely used why because, Silicon is stable while dependent of temparature than Germanium i.e

The Germanium has a Nucleus with 32 protons and 32 electrons i.e.
The electrons are distributed as follows :

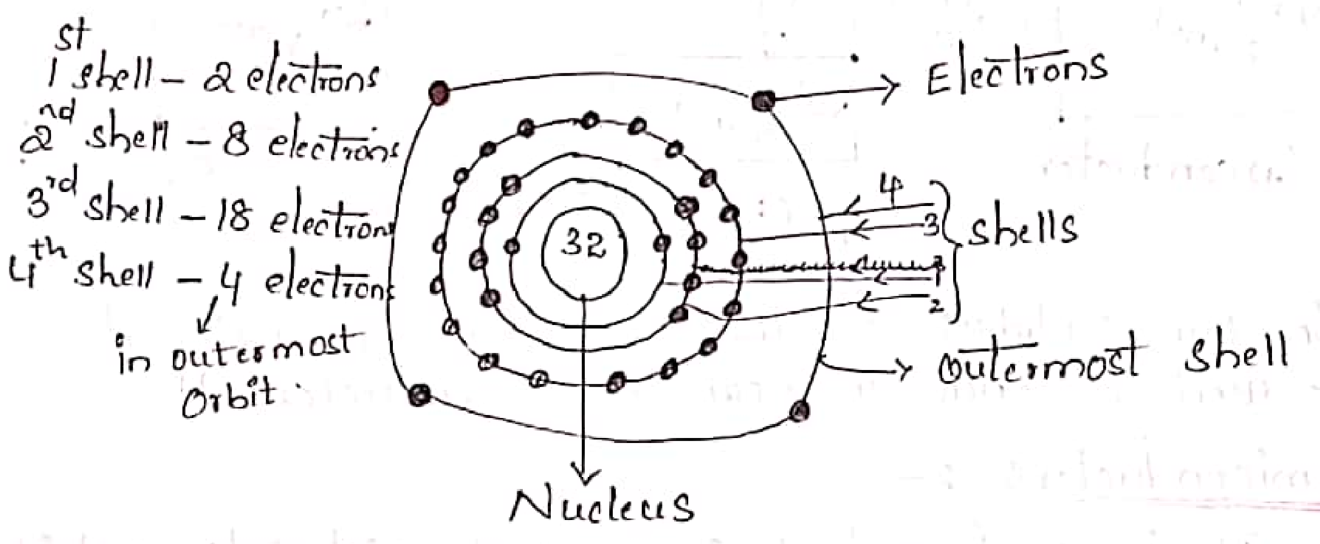

fig : Germanium atom

* The Silicon has Nucleus with 14 protons and 14 Electrons.

2 electrons – 1st shell/orbit.
8 electrons – 2nd shell/orbit.
4 electrons – outer most orbit.

+14
2nd shell (8e)
1st shell (2e)
Nucleus
electrons
outermost shell [3rd shell]

fig : Silicon atom (4 electrons).

* Looking at the Structure of Silicon & Ge atom, it can be seen that Valence shell (outer most shell) of silicon is 3rd shell, while Valence shell of "germanium" is 4th shell. Hence Valence electrons of Ge are at larger distance from Nucleus than Valence electrons of Silicon.

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hence Valence electrons $\bar{e}$ of Ge are more loosely bound to the Nucleus than those of Silicon. Thus Valence electrons of Ge can easily escape from the atom, due to Very small additional Energy imparted to them. So at high temparature, Ge becomes unstable than Silicon. So, we mostly prefer "Si" than "Ge" Semiconductor material.

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Classification of Semi-conductors :-

2 types
1. Intrinsic Semiconductors
2. Extrinsic Semiconductors

1. Intrinsic Semiconductors :-

* A Sample of Semiconductor in its purest form is called an "Intrinsic Semiconductor".
* Impurity content is Very very small
* for understanding the conduction in an Intrinsic Semiconductor let us study the Crystalline structure of an Intrinsic Semiconductor.

Crystal structure of Intrinsic Semiconductor :-

Consider an atomic structure of an intrinsic Semiconductor like silicon. An outermost shell of an intrinsic Semiconductor of silicon has 4 electrons. each of these 4 electrons form a bond with another Valence electron of the neighbouring atoms. This is nothing but sharing of electrons. Such bonds are called "Covalent bonds". The atoms align themselves to form a 3Dimensional uniform pattern called a "Crystal".

But 3D structure is very difficult to represent pictorially. Hence the symbolic 2D structure is used to represent a 3D crystal form as shown figure below.

* The Covalent bonds are represented by a pair of dotted lines encircling the two electrons forming the covalent bond.

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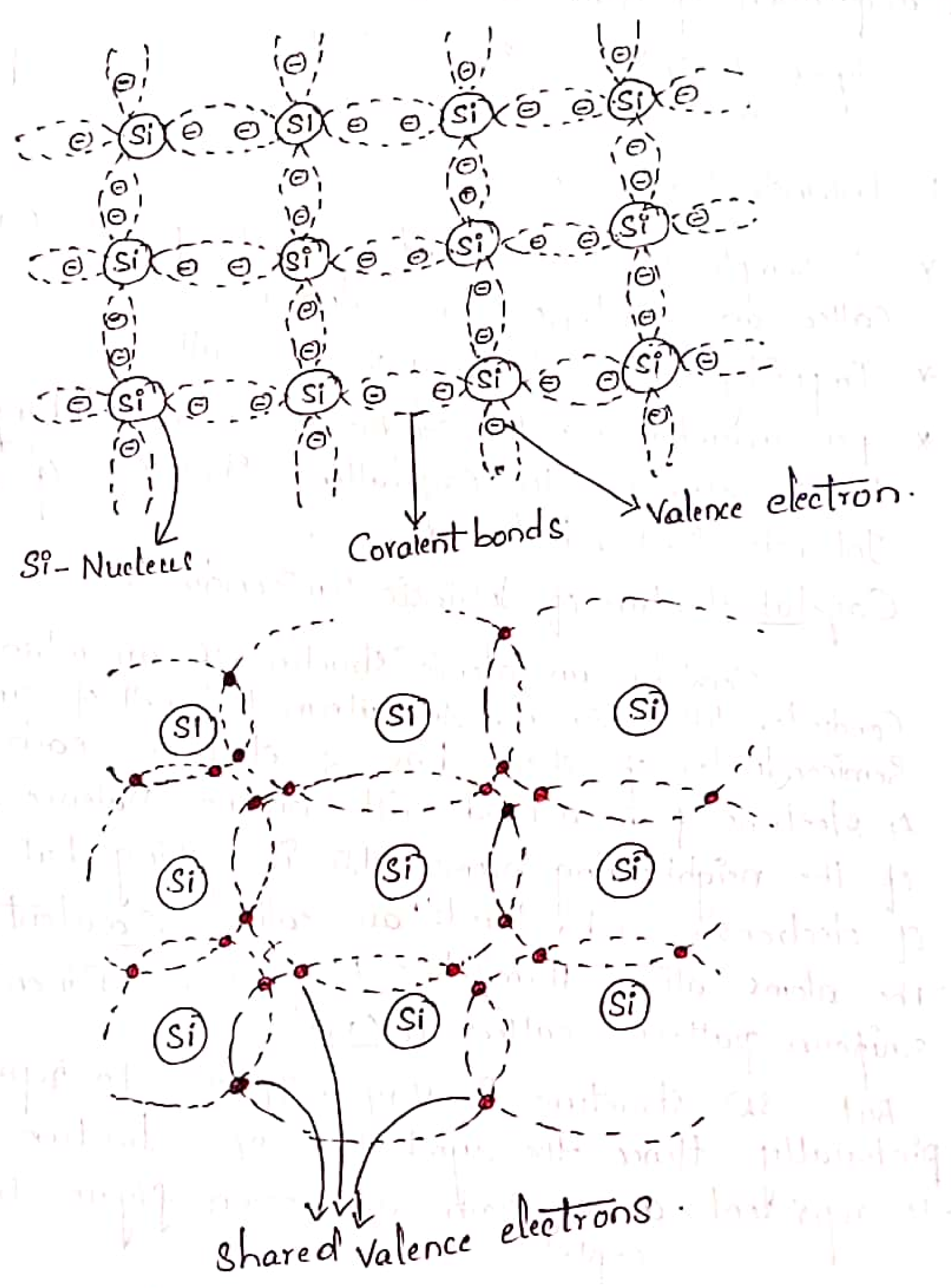

fig (a) & (b) : Two Dimensional representation of Silicon crystal.

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* In figure (b), we observe sharing of valence electrons and both the electrons are shared by the two atoms. Hence the outermost shell of valence electrons of all the atoms is completely filled, and valence electrons are tightly bound to the parent atom. "No-free electrons are available at absolute zero temparature.
* Hence such an Intrinsic Semiconductor behaves as a "perfect insulator" at "zero temparature."

At room temperature, behaviour of Intrinsic Semiconductor :-

* Intrinsic Semiconductors behaves as a perfect insulator at absolute zero temperature.
* At room temparature, Number of valence electrons absorb the thermal energy, due to which they break the covalent bond and drift (moves) to the conduction band. Such electrons become free to move in the crystal as shown in fig below.

Electron-hole pair → [diagram: Si, Si, hole, free electron] ← Due to Thermal Energy break covalent bond Creates holes.

* Energy required to break the Covalent bonds is 0.72 eV for germanium } at room temperature
  1.1 eV for Silicon

* Once the electrons are dislodged from the covalent bonds & then they become free, such free electrons wander in a random fashion in a crystal.
* When a valence electron drift from valence to conduction band breaking a covalent bond, a vacancy is created in the broken covalent bond. such vacancy is called a hole. whenever electron becomes free, the corresponding holes gets generated.
* So free-electrons and holes (→ positively charged) get generated & in pairs. such generation of electron-hole pair due to thermal energy is called "Thermal generation".

Electron-hole pair

Si

Conduction-band (Electron)

E_G

Valence band (Hole)

Electron-hole pair

fig(b)

fig: (a) Electron-hole pair in crystal structure of silicon.
(b) Energy-band diagram

Conduction by Electron and Holes :-

* The electrons and holes generated due to the thermal generation move randomly and hence cannot constitute any current.
* Now consider that battery is connected across the Intrinsic Semi-conductor.
* under the influence of applied voltage (battery) there is electron as well as hole motion in particular direction causing the "flow of current".

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* The free electrons are moved under the influence of applied voltage. These electrons are negatively charged get repelled from the -ve terminal of battery and attracted towards the +ve terminal. Thus there is an electric current due to the movement of electrons in Conduction band. This is called "Electron current".

* Ily, The holes are moved under the influence of applied voltage. These holes are +vely charged get repelled from the +ve terminal of battery and attracted towards the -ve terminal. Thus there is an electric current due to the movement of holes in Valence band. This is called "Hole current".

* Hole current is, the direction of motion of holes is in the opposite direction to that of electrons.

** **Note :-**
* Current due to movement of free electrons in the conduction band is "Electron-current".
* Current due to movement of holes in the Valence band is "Hole current".
* The Electron as well as hole current together Constitutes current in an intrinsic Semiconductor.

Holes
hole
free electron
+ -
o — Holes
• — electrons.
→ :- direction of flow of holes
← :- direction of flow of electrons

Fig: Conduction in Intrinsic Semiconductor.

Conductivity : The property called conductivity indicates the ease with which a material can carry the current. Thus more conductivity means that material can carry high current, very easily.

* The conductivity of a good conductor is high while that of an insulator is low.

Note :- In Intrinsic Semiconductor, Very few electron-hole pairs get generated at room temperature. Hence very small current can be constituted, due to the application of voltage to an Intrinsic Semiconductor. Thus the conductivity of an Intrinsic Semiconductor at room temperature is very low. Such a low conductivity has very little practical significance. i.e Intrinsic Semiconductor are not used in practice for manufacturing of electronic devices.

* Recombination of electrons and Holes :-
electrons movement in conduction band is always random
Holes movement in valence band is always random
This Thermal agitation continues to produce new Electron-Hole pairs. This merging of electrons and Holes is called "Recombination of electrons & holes".

* After recombination, electron-hole pair gets disappeared
* Due to recombination, charge carriers (electrons & holes) are decreases.
* The amount of time b/w the creation and disappearance of a free electrons or holes is called "Mean life time of the charge carrier".

Intrinsic concentration :-

At any temperature, at any instant, the free electrons and holes the two types of charge carriers are present in equal number. This concentration is called "Intrinsic Concentration"

Mathematically, indicated as,

$$n = p = n_i$$

Where n = Number of free electrons per unit volume

p = Number of holes " " "

n_i = Intrinsic concentration (units : number per m^3 (or) number per cm^3)

Derivation of Conductivity of an Intrinsic-Semiconductor :-

For the Semiconductor :-

n = Concentration of free-electrons / m^3

p = Concentration of holes / m^3

μ_n = Mobility of electrons in $m^2/V\text{-}s$

μ_p = Mobility of holes in $m^2/V\text{-}s$

The current density is given by,

$$J = (n\mu_n + p\mu_p)\, q\, E \ \ A/m^2$$

Where q = charge on one electron $= 1.6 \times 10^{-19}$ C

E = Electric field in V/m

According to ohm's law $\boxed{J = \sigma E}$

where σ = conductivity in $(\Omega\text{-}m)^{-1}$

Comparing (1) & (2) eqs

$$\sigma \cancel{E} = (n\mu_n + p\mu_p)\cancel{E} q \ (\Omega\text{-}m)^{-1}$$

Conductivity is $\boxed{\sigma = (n\mu_n + p\mu_p)\, q \ (\Omega\text{-}m)^{-1}}$

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for intrinsic semiconductor :

$$\sigma_i = n_i(\mu_n + \mu_p) q \ (\Omega\text{-}m)^{-1}$$

EXTRINSIC SEMICONDUCTORS :-

In order to change the properties of intrinsic semiconductor a small amount of some other material is added to it.

* The process of adding other material to the crystal of intrinsic semiconductors to improve its conductivity is called "Doping".
* Doped semiconductor material is called "Extrinsic Semiconductor"
* The Doping increases the conductivity of the basic intrinsic semiconductors hence the extrinsic semiconductors are used in practice for manufacturing of various electronic devices such as diodes, transistors etc.

Types of ~~Impurities~~ Extrinsic Semiconductors :-

Depending upon the type of Impurities, the two types of Extrinsic Semiconductors are

1. n-type
2. P-type

Types of Impurities :-

1. Donar Impurity
2. Acceptor Impurity

Donar Impurity :- The Impurity material having 5 valence electrons is called "pentavalent atom" when it is added to an intrinsic semiconductor it is called "Donar doping"

* Each impurity atom donates one free electron to an intrinsic material. Such an impurity is called "Donar impurity"

Ex:- Arsenic, Bismuth, phosphorous etc.

This creates an Extrinsic semiconductor with large number of free electrons, called n-type Semiconductor.

Acceptor Impurity :- another type of Impurity is trivalent atom which has only 3 Valence electrons. such an impurity is called "Acceptor impurity". when this is added to an intrinsic Semiconductor, it Creates more holes and ready to accept an electron hence the doping is "acceptor doing".

Ex:- Gallium, Indium, Boron etc.

The resulting extrinsic Semiconductor with large number of holes is called p-type Semiconductor.

N-Type Semi-conductor :-

Definition :- When a small amount of pentavalent impurity is added to a pure semiconductor, it is called as "n-type Semi-conductor".

P
A
A
B

pentavalent impurity : has 5 valence electrons.

Ex: Arsenic, Bismuth, Antimony, phosphorous

83 15 33 51

* these Impurities are called as "Donar impurity".

formation :- Consider the formation of n-type material by adding Arsenic (As) into Silicon (Si). The arsenic atom has five valence electrons. Silicon atom has 4 Valence electrons. These forms covalent bonds with four adjacent silicon atoms. but 5th electron has no charge to formation a covalent bond.

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This spare electron enters the conduction band as a "free electron". This means that each arsenic atom added into silicon atom gives one free electron. The number of free electrons are controlled by the amount of impurity added to the silicon.

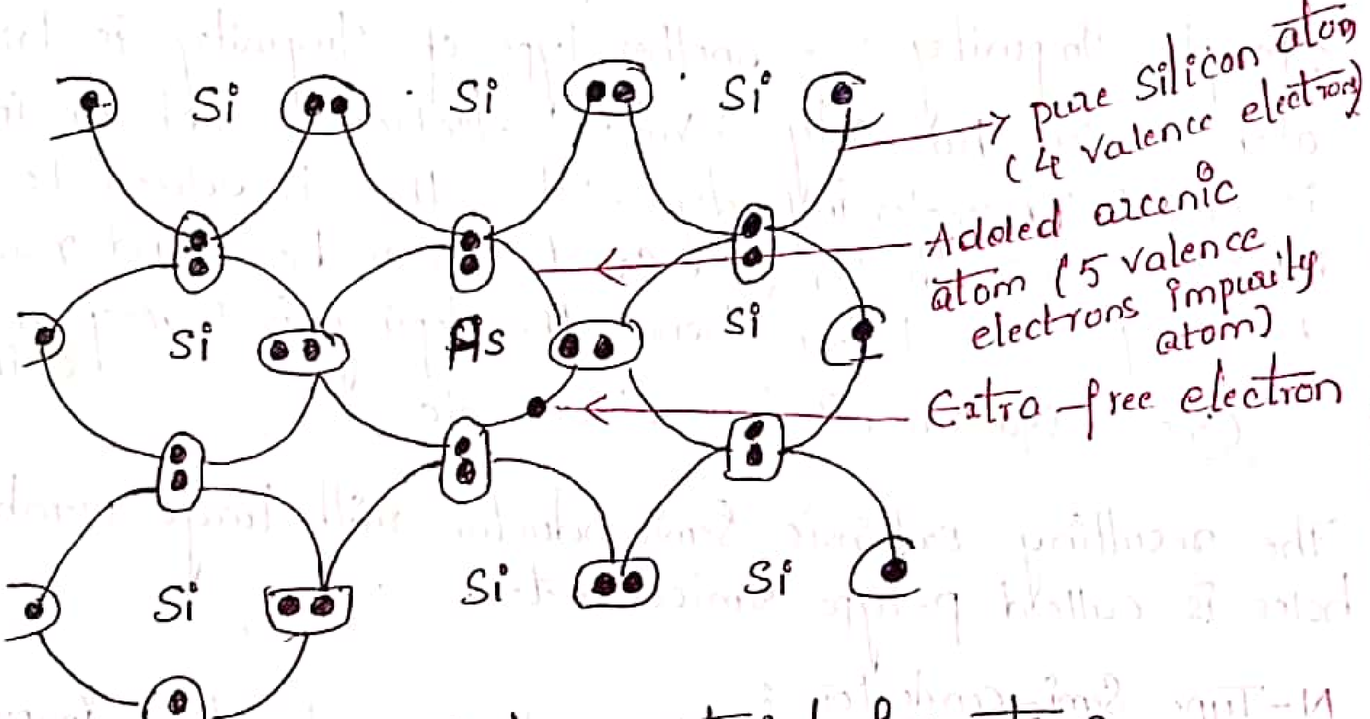

fig :- N-type material formation.

Conduction in N-type Semi-conductor :-

N-type material

free electrons (large in number) (majority).

Holes small in number (minority).

fig: Conduction in n-type material.

When the vtg (voltage) is applied to the n-type Semiconductor, the free electrons which are readily available due to added impurity, move in a direction of positive terminal of voltage applied. Holes are less in number hence electrons are dominated here.

Hence In N-type, free electrons are majority Carriers while the holes which are small in number are called "Minority Carriers".

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Conductivity of n-type material :

It is known that in n-type semiconductor material, the free electrons are majority carriers while the holes are minority carriers.

n_n = Concentration of free electrons in n-type
P_n = Concentration of holes in n-type
N_D = Concentration of donor atoms.

here p, n indicates concentration of type of charge carrier electron or hole while the suffix indicates the type of material i.e., n type or p-type.

from basic equation of conductivity,
the conductivity of n-type material can be expressed as,

$$\sigma_n = (n_n \mu_n + p_n \mu_p) e$$

but $P_n << n_n$ as holes are in minority hence,

$$\sigma_n = n_n \mu_n e$$

The number of free electrons is dominantly controlled by donor atoms added than the thermal generation at room temparature.

Hence, concentration of donor atoms N_D added can be approximately assumed to be equal to concentration of free electrons n_n in 'n' type materials.

Thus as $N_D >> n_i$ we can write

$$n_n \simeq N_D$$

$$\sigma_n \approx N_D \mu_n e$$

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2. **P-Type Semiconductor :-** (BINS)

When a small amount of trivalent impurity is added to a pure semiconductor, it is called "p-type Semiconductor."

* Tri-valent impurity has 3-valence electrons. These elements are Galium (Ga), Boron (B), Indium (In), Aluminium (13) etc. such an impurity is called "Acceptor Impurity". (BAGI)

P-Type material formation :-

Consider the formation of p-type material by adding Gallium (Ga) into Silicon (Si). Galium atom has 3 valence electrons & Si has 4 valence electron. So galium atom fits in the silicon crystal in such a way that its 3 valence electron form covalent bonds with the 3 adjacent atom of silicon. Being short of one electron, the fourth covalent bond in the valence shell is incomplete. The resulting vacancy is called a hole. Such a p-type material formation is represented as follows.

Si Si Si Si Ga Si Si Si Si

covalent bonds.

pure Si atom (4 valence electrons)

Hole Created due to incomplete bond

Added galium atom (3 Valence electron)

fig: P-Type material formation.

* Note: In this structure galium atom (trivalent impurity) is added to Si-atom (semi-conductor material) it give one hole. This process repeated for more no. of times gives more holes

Hence, p type material has majority number of Holes and minority number of electrons.

Conduction in p-type Semi-conductor :-

Now, p-type material is subjected to an electric-field by applying a voltage then the holes move in a valence band and are mainly responsible for the conduction. So the current conduction in p-type material is predominantly due to the holes. The free electrons are also present in conduction band but are very less in number. Hence holes are majority carriers while electrons are minority carriers in p type material.

The conduction of p-type material is as shown below

p-type material
Holes (majority)
Direction of holes.
o – Holes
• – Electrons
+ –
Direction of Conventional Current
Electrons (minority)

Fig: Conduction in p-type material.

When applying '+' positive terminal to one side of p type material and negative terminal is connected to another side of p-type. holes are positively charged so these are repell to positive terminal move away from positive terminal & move towards to negative terminal because of dislike polarities are attracted to each other. Hence current conduction take place through negative to positive terminal direction.

Conductivity of p-type material :-

For p-type holes are majority carriers, electrons are minority.

n_p = Concentration of free electrons in p-type
p_p = Concentration of Holes in p-type
N_A = Concentration of Acceptor atoms

Thus, the conductivity of p-type material can be Expressed as,

$$\sigma_p = (n_p \mu_n + p_p \mu_p) q \longrightarrow (1)$$

But $n_p << p_p$ as free electrons are in minority here

Hence from ① ⇒

$$\sigma_p = (p_p \mu_p q) \longrightarrow (2)$$

(n_p - neglected. so $n_p \mu_n = 0$).

The Number of Holes is dominantly controlled by added acceptor impurity than the Thermal generation. Each added impurity atom Creates a hole. hence $N_A >> n_i$. Thus all the holes generated p_p can be approximately assumed to be equal to the Concentration of acceptor N_A.

$$\therefore p_p \approx N_A$$

$$\therefore \sigma_p = N_A \mu_p q \longrightarrow \text{from } ②$$

(n_i = intrinsic concentration of the basic semiconductor used.)

Law of Mass-Action for Extrinsic-Semiconductor :-

Mathematically, the law is Expressed as,

St:- The product of electron & hole Concentration is equal to square of the intrinsic Carrier Concentration.

$$n \cdot p = n_i^2$$

Where n_i is Intrinsic concentration

Important observations :-

1. The Law can be applied to both intrinsic and extrinsic semiconductors.
2. In Case of Extrinsic Semiconductors, n_i is the intrinsic Concentration of the basic semiconductor material used.
3. For n-type material, $n = n_n$ while $p = p_n$
   Hence Law can be stated as...

$$n_n p_n = n_i^2$$

4. For p-type $n = n_p$ while $p = p_p$ hence law can be stated as $n_p p_p = n_i^2$
5. The Law is applicable irrespective of amount of doping.
6. As n_i depends on temparature, the law applicable at a fixed temperature.
7. The Law can be used to find both majority and minority Carrier Concentrations in an Extrinsic Semiconductor.

Proof:- Generation of charge Carrier = Recombination of charge Carriers.

$$R = G$$

Generation of charge Carrier's $G = n = p = n_i$

∴ Recombination of charge Carrier $R \propto n \cdot p$

$R \propto n \cdot p$

$G = R = r \cdot n \cdot p \rightarrow (1)$

$G = r \cdot n \cdot p = r \cdot n_i^2 \rightarrow (2)$

$(1) = (2)$

$r \cdot n_i^2 = r \cdot n \cdot p$

$$n_i^2 = n \cdot p$$

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Carrier Concentration in Extrinsic Semi-Conductors :-

Let us obtain the Concentration of minority and majority carriers in n type and p-type materials using Law of mass action.

N-type material :-

for n-type, $n_n = N_D$

At any fixed temperature, according to "Law of mass action"

$$n_n \times P_n = n_i^2$$

where n_n = majority (electrons) carrier Concentration.
P_n = minority (holes) carrier Concentration.

Using $n_n = N_D$, we can write minority carrier concentration as

$$N_D P_n = n_i^2$$

$$\boxed{P_n = \frac{n_i^2}{N_D}}$$ //

P-type material :-

for p-type $P_p = N_A$

According to law of mass action,

$$n_p \times P_p = n_i^2$$

where n_p = (electron) i.e minority Carrier Concentration
P_p = (hole) i.e majority Carrier Concentration

Using $P_p = N_A$ we can write

$$n_p N_A = n_i^2$$

$$\boxed{n_p = \frac{n_i^2}{N_A}}$$ //

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Concept of Depletion region and Barrier potential :

Extrinsic Semiconductors are classified as 2-types those are n-type and p-type. In n-type, the electrons are majority charge Carriers, while holes are minority charge carriers. In p-type, the holes are majority charge Carriers and electrons are minority charge carriers. These two types of materials namely p-type and n-type are chemically Combined with a Special fabrication technique to form a p-n junction. Such a Semiconductor p-n junction forms a popular electronic device called "Diode".

The Diode is a basic element of number of electronic Circuits. Thus, the study of behaviour and characteristics of Semiconductor p-n junction is very important in understanding the operation of number of Electronic circuits and applications.

* Before Enter into the operation of p-n junction diode, first we need to know some simple basic Concepts regarding to the p-n junction operation.

Those are

* formation of Depletion region
* Barrier potential

Formation of Depletion Region :— {Depletion region also called as "Transition region" and also space charge region}

* Normally, In ptype and n-type materials while we are Combine, junction is form. Concentration gradient Exist near to the junction. There are large number of holes on p-side while Very small number of holes on n-side, near the junction. Thus holes starts moving from p side to n-side i.e from high Concentration area towards low Concentration area.

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This is nothing but "Diffusion" of holes from p side to n side.

○ ⇨ Hole diffusion

⇦ ● Electron diffusion

(P) (n)

Depletion region

As holes enter the n-region, they find number of donor atoms. The holes recombine with the donor atoms. As donor atoms accept additional holes, they become positively charged immobile ions. This happens immediately when holes cross the junction hence number of positively charged immobile ions get formed near the junction on n-side.

Junction

Fig (2): Formation of immobile ions

Depletion region

Atoms on p-side are acceptor atoms. The electrons diffusing from n-side to p side recombine with the acceptor atoms on p-side. As acceptor atoms accept additional electrons, they become negatively charged immobile ions. Such large number of negatively charged immobile ions get formed near the junction on p-side. The formation of immobile ions near the junction is shown in above fig (2).

Thus in thermal Equilibrium, in the region near the junction there Exists a wall of negative immobile charges on p-side and a wall of positive immobile charges on n-side. In this region, there are no mobile charge Carriers. Such a region is depleted of the free mobile charge Carriers and hence called "Depletion region" or "Depletion layer".

Note :- The Depletion region gets formed in open Circuited p-n junction very quickly.

* The Depletion region is also called "Space-charge region.
* In Equilibrium Condition, the depletion region gets widened upto a point where no further electrons or holes can cross the junction. Thus depletion region acts as the "Barrier".

Barrier potential :- (also called as - Junction potential / Built-in-potential) :

Near the junction, on one side there are many positive charges and on other side there are many negative charges. According to Coulomb's law, there Exists a force between these opposite charges. And this force produces an Electric field between the charges. The Direction of an Electric field is from positive charge towards negative charge.

The opposite charges existing near the junction Creates a potential difference (Voltage) across the junction. The Electric field between the charges is responsible to produce potential difference across the junction. This potential difference has a fixed polarity and it acts as a barrier to flow of electrons and holes, across the junction. Hence this potential is called Barrier potential, junction potential or built-in potential barrier of a p-n junction.

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* Barrier potential is Expressed in volts. its Value is called "Height" of the barrier of a p-n denoted as V_j (or) V_{bi}
* Barrier potential also indicates the amout of voltage with proper polarity, to be applied across the p-n junction, to restart the flow of electrons and holes across the junction.

* The Barrier potential is expressed in volts, it is approximately 0.7V for Silicon and 0.3V for germanium, at 25 °C.

* Barrier potential of p-n junction mainly depends on the following factors:

1. The Type of Semiconductor used.
2. The Concentration of donor impurity on n-side
3. The Concentration of Acceptor impurity on p-side
4. The intrinsic Concentration of basic semiconductor
5. The Temparature.

The Expression for the Barrier potential / junction potential is

$$V_j = V_T \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Where V_T = voltage equivalent of temperature

N_D = Doping Concentration of n-side / amount of doping of n-side.

N_A = Doping Concentration of p-side / amount of doping of p-side.

Note: V_j (junction potential / Barrier potential) is depends on V_T.

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CONCEPT OF DRIFT CURRENT AND DIFFUSION CURRENT

DRIFT CURRENT :—

* When a voltage is applied to a Semiconductor, the free electrons try to move in a Straight line towards the positive terminal of the battery.
* The electrons moving towards positive terminal Colloide with the atoms of semiconductor and Connecting wires along its way.
* Each time electron strikes an atom, it rebounds in a random direction.
* But still the applied voltage make the electrons drift towards the positive terminal. This drift Causes Current produced due to drifting of free electrons is called "Drift Current", and the Velocity with which electrons drift is called "Drift Velocity".

Definition :— Drift current means, the flow of current due to Bouncing of electrons from one atom to another, travelling from negative terminal to positive terminal of the applied voltage.

fig:- Drift mechanism Causing Drift current.

DIFFUSION CURRENT :—

* Due to drifting of free electrons under the externally applied voltage, produces Drift-current.
* In addition to drift current, there may exist an additional current due to the transport of charges in a Semiconductor. Such an additional current is due to the phenomenon called "Diffusion".
* The current due to diffusion is called "Diffusion current". Basically it is due to "Non-uniform Concentration of charged particles" in a Semiconductor
* Let us know what is Diffusion and Non-uniform Concentration of charged particles":

Consider a p-type Semiconductor bar which is Non-uniformly doped as shown in fig. Due to non-uniform doping the holes are large in number on one side while less in number on other side. Due to this there is High Carrier Concentration area with one side and lower Carrier Concentration area on another side. This Creates "Concentration Gradient". In one side more no. of holes and another side lesser number holes due to applied voltage, the holes in higher side are move from higher Concentration area to lower Concentration area. Such a movement of charge Carriers, due to Concentration gradient in a Semiconductor is called process of "Diffusion"..

Both Drift & Diffusion currents are occur in the Semiconductor devices.

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Non-uniform doped semiconductor

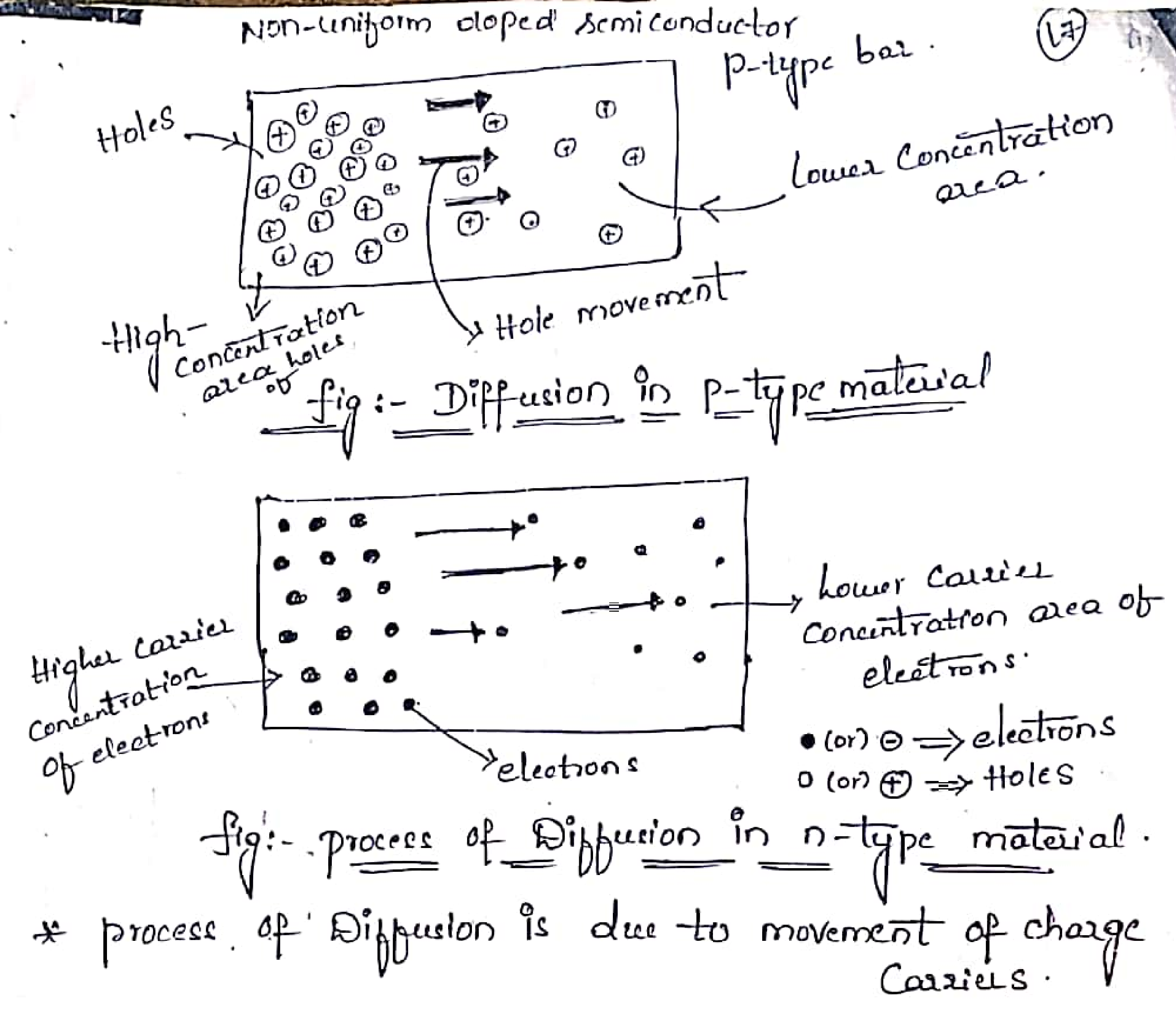

fig :- Diffusion in p-type material

fig :- process of Diffusion in n-type material.

* process of Diffusion is due to movement of charge carriers.

P-N Junction Diode :-

Introduction :-

"William Henry Eccles" was the first founder of Diod in 1919. It was derived from Greek roots as Di- means two "ode" - means Electrodes Combinedly called as Diode.

* Two types of Extrinsic semiconductors n-type & p-type are chemically combined with a special fabrication technique to form a p-n junction. Such a semi-conductor p-n junction forms popular electronic device called "p-n junction diod
* p-n junction has two terminals called Electrodes (anode, cathode) one each from p & n regions.

Symbol of P-n junction Diode :-

R. Diode (D)
\+ | -

(a) Anode o——▷|——o Cathode.

(b) Anode (Electrode 1) o——[P | n]——o Cathode. (Electrode-2).
ohmic contacts.

fig (a), (b) : Symbol and Schematic of p-n junction.

Construction :-

p-n junctions forms by Combining of p-type & n-type Semiconductors. It has two terminals called electrode i.e anode and cathode one each from p-region and n-region. To Connect n and p regions to the External terminals, a metal is applied to the heavily doped n and -type semiconductor regions. Such a Contact between

a metal and a heavily/lightly doped semiconductor is called "Ohmic contact".

* In p-type majority carriers are Holes, minority carriers are electrons.
  n-type majority carriers are Electrons, minority carrier are Holes.

* When we are combining p and n type semiconductors it forms a junction.

* The p-n junction diode is as shown below:

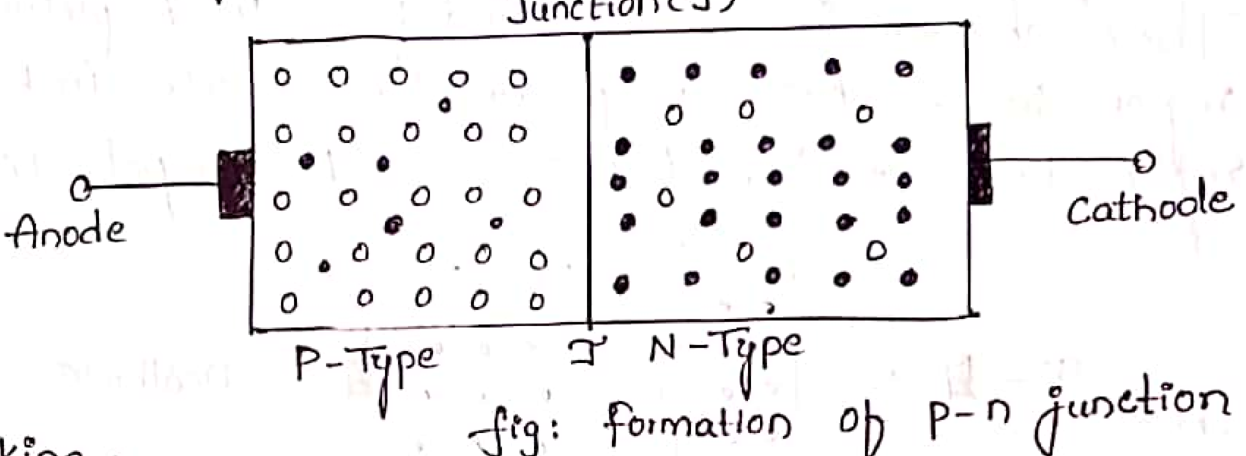

fig: formation of p-n junction

<u>Working</u>:

The electrons are majority charge carriers in n-type there are attracted towards holes of p-side near the junction. These electrons are cross over the junction and recombine with holes it sees to be free carriers. This process of recombination of electrons with holes and similarly from p-side holes are attracted to electrons in n-side. This process of recombination of electrons & holes is called "<u>Diffusion</u>". This recombination exist only at nearer to the junction only, free electrons & holes get depleted near the junction.

* Depletion region contains only negative ions on p-side positive ions on n-side of junction. These ions are "Immobile ions".

* Motion of electrons from n-side to p-side doesn't stop immediately, after the formation of Depletion region. But it cross the junction these electrons are repples to negative ions in Depletion region then it stops moment of electrons.

* These charged ions (electrons and holes) in Depletion region develope an Electric field in Depletion region known as "Junction potential / Barrier potential".

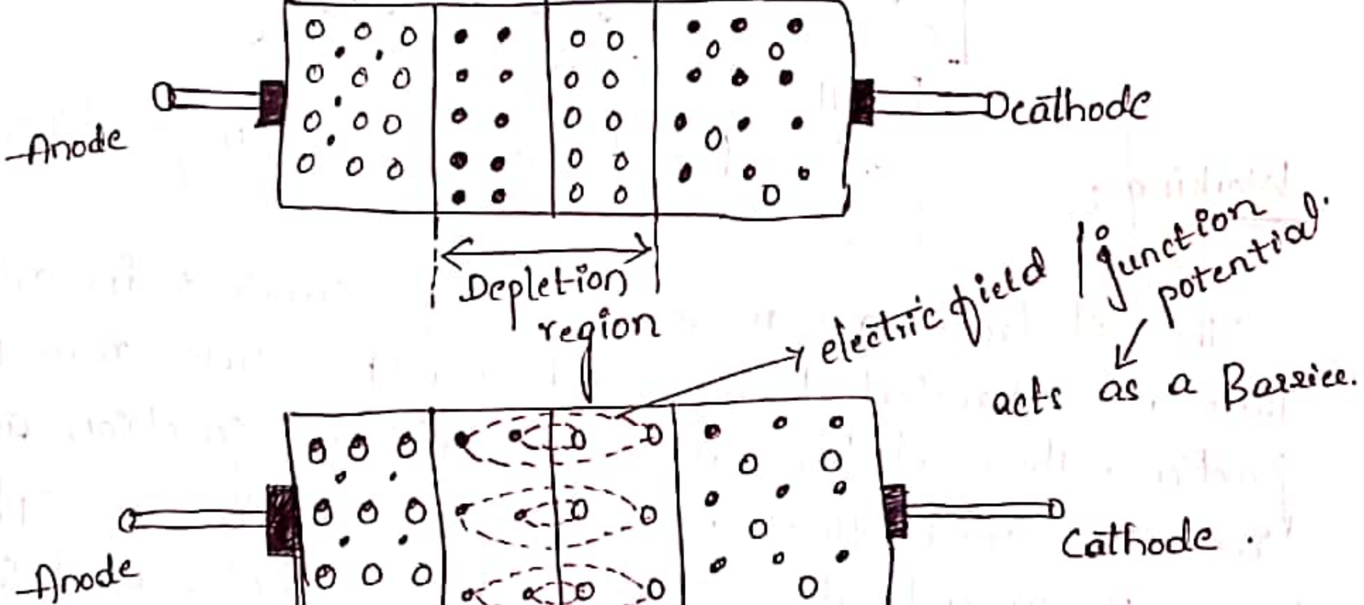

fig: Formation of Barrier potential in Depletion region.

* Junction potential acts as "Barrier also called as "Barrier potential" it restricts the flow of electrons and holes

Junction/Barrier potential for Si – 0.7V and,
for Ge – 0.3V

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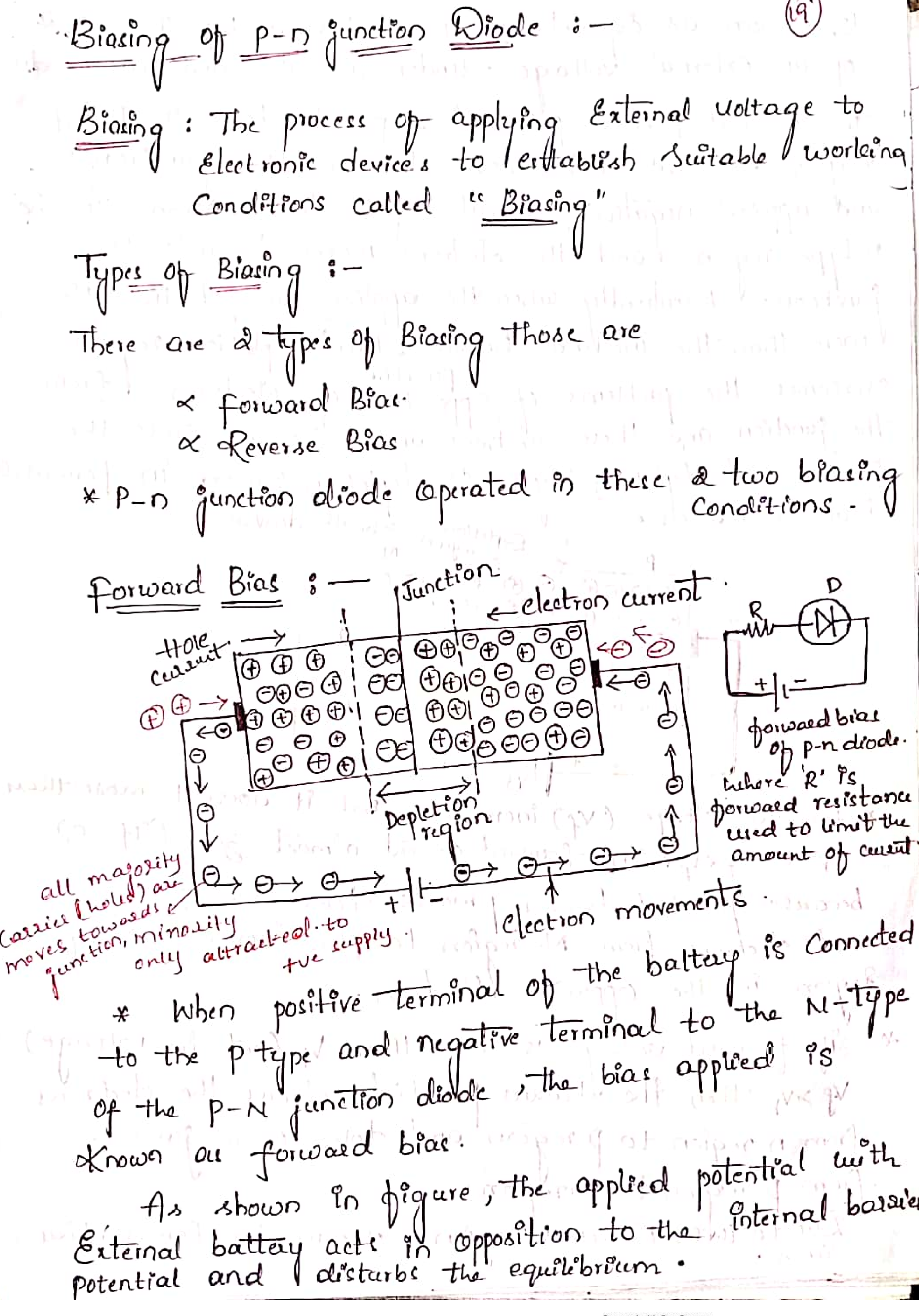

Biasing of P-n junction Diode :-

Biasing : The process of applying External voltage to Electronic devices to establish suitable working Conditions called "Biasing"

Types of Biasing :-

There are 2 types of Biasing those are

- ∝ forward Bias
- ∝ Reverse Bias

* P-n junction diode operated in these 2 two biasing Conditions.

Forward Bias :-

* When positive terminal of the battery is Connected to the p type and negative terminal to the N-type of the P-N junction diode, the bias applied is Known as forward bias.

As shown in figure, the applied potential with External battery acts in opposition to the internal barrier potential and disturbs the equilibrium.

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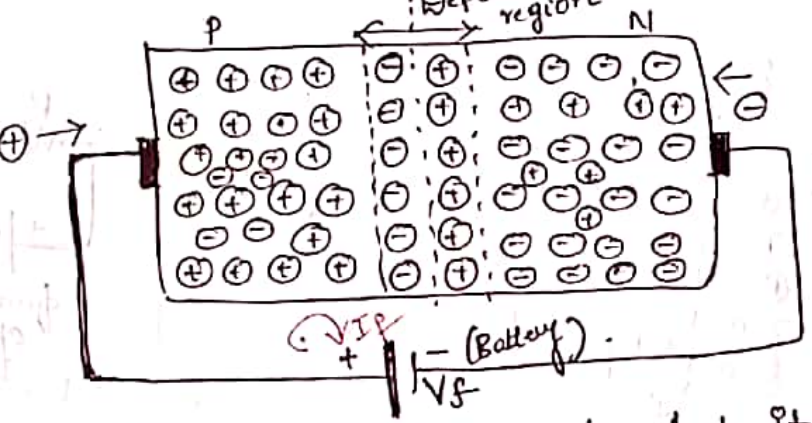
As soon as Equilibrium is disturbed by the application of an external voltage. Under the forward bias Condition. The applied positive potential repels the holes in p-type region. so that holes moves towards the junction and applied negative potential repels the electrons in the n type region and the electrons moves towards the junction. Eventually when the applied bias potential is more than the internal barrier, then in depletion region Overcomes the problems of potential Opposition of electrons from the junction and these electrons and holes are cross the junction and depletion layer. So depletion region in forward bias is reduces.



* forward voltage (V_f) increased, but it does not more than V_γ i.e $V_f < V_\gamma$ the forward current almost zero ($I_f = 0$). because potential barrier prevents holes from p-region and electrons from N-region to flow across the depletion region in the opposite direction.
* If forward voltage is more than V_γ (cut-in-voltage) $V_f > V_\gamma$ then the barrier potentials allows the electrons from n region to p region and holes cross junction from p region to n region.

Due to this, Depletion region decreases in forward bias Condition.

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Forward V-I characteristics of Diode :-

* The response of p-n junction can be easily indicated with the help of characteristics called V-I characteristics of p-n junction diode.
* It is the graph of vtg applied across the p-n junction diode (V_f) and current flowing through the p-n junction (I_f).

If (mA)
D
C
ΔIf
Q
F
E
ΔVf
P
Knee-point
O
zero
Cut-in voltage (V_γ)
A
B
Vf (V)

If (mA)
(V)
V
cut-in voltage (V_γ (or) V_{th})

Fig : Forward characteristics of a Diode.

Basically forward characteristics can be divided into 2 regions

1. Region O to P :- If V_f is less than V_γ (cut-in-voltage) the current flowing is very small. practically this current is assumed to be zero.

2. Region P to Q and onwards :-

If V_f increases towards V_γ the width of depletion region goes on reducing; when V_f exceeds V_γ i.e $V_f > V_\gamma$ the depletion region becomes very thin and current I_f increases suddenly. This increase in the current is exponential as shown above figure.

Diode Resistance under Forward bias :-

Forward Resistance of Diode :- Resistance offered by the p-n junction diode in forward bias condition is forward resistance.

1. Static forward resistance :-

Forward resistance is denoted as R_f and this can be calculated on a particular point on the forward characteristics.

Thus at a point E shown in the forward characteristics, the static resistance R_f is defined as the ratio of the d.c voltage applied across the p-n junction to the d.c current flowing through the p-n junction. It is also called as "d.c Resistance"

$$R_f = \frac{\text{forward d.c voltage (V)}}{\text{forward d.c current (I)}}$$

I_f (mA) ; $R_f = \frac{V_f}{I_f}$; V_f (V)

fig: forward biasing of a diode

from forward characteristics $R_f = \frac{OA}{OC}$ at point E.

2. A.C / Dynamic forward resistance :-

The resistance offered by the p-n junction under a.c conditions is called "Dynamic resistance" (or) "A.C resistance".

"Dynamic resistance" is reciprocal of the slope of the forward characteristic.

It is also defined as ratio of change in applied voltage from point A to B shown in fig which is ΔV_f and their corresponding change in forward current from C to D i.e ΔI_f.

Thus slope of characteristics is $\Delta I_f / \Delta V_f$

I_f (mA) ; ΔI ; I_1 ; V_f (V) ; ΔV

$\text{Slope} = \frac{1}{R_f} = \frac{1}{\Delta V_f / \Delta I_f}$

$$\therefore r_f = \frac{\Delta V_f}{\Delta I_f} \Rightarrow r_f = \frac{1}{(\Delta I_f / \Delta V_f)} = \frac{\eta V_T}{I}$$

where η = constant. $\text{slope} = \frac{\Delta I_f}{\Delta V_f}$.

$$r_f = \frac{1}{(\text{Slope of forward characteristics})}$$

I_f (mA) ; ΔI_f ; V_f (V) ; ΔV_f

fig: Dynamic ...

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2. Reverse biasing of p-n junction diode :—

Definition :

If an External d.c voltage is Connected in such a way that the p-region terminal of a p-n junction is Connected to the negative of the battery and the n-region terminal of a p-n junction diode is Connected to the positive terminal of the battery, this biasing Condition is called "Reverse biasing" of p-n junction.

The below figure shows the Connection of p-n junction in reverse bias Condition.

R J P n − +

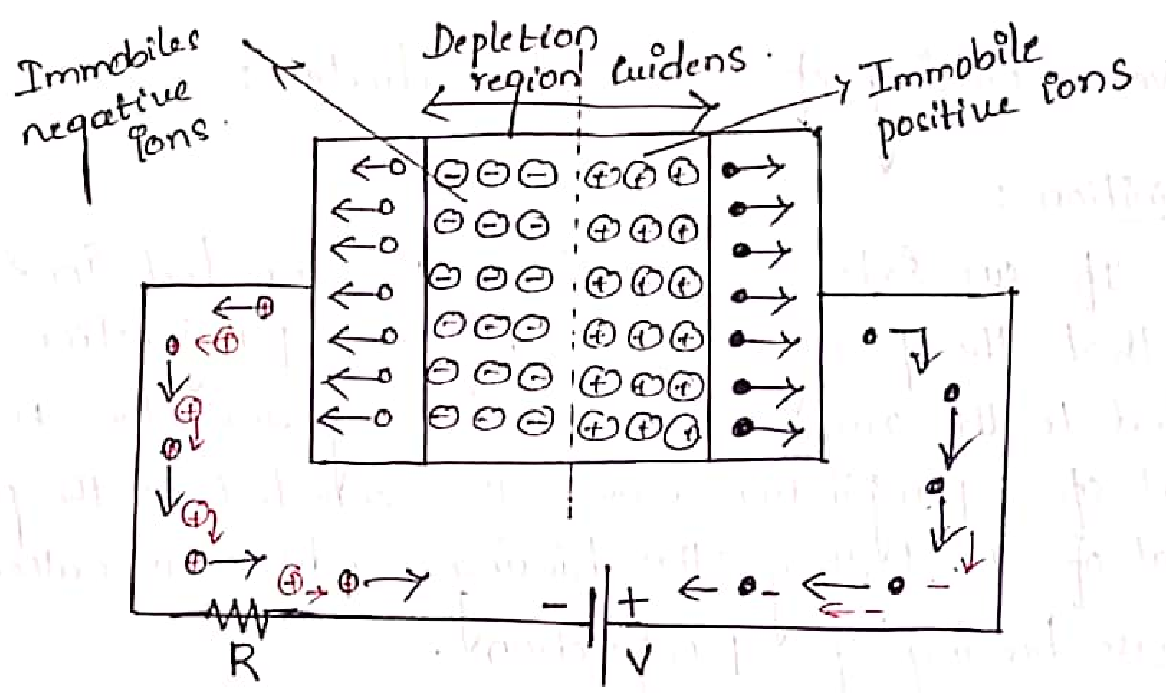
fig: Reverse biasing

R + − − +

fig: Symbol representation

Operation :—

* When the p-n junction is reverse biased the negative terminal attracts the holes in the p-region, away from the junction.
* The positive terminal attracts the free electrons in the n-region away from the junction.
* No charge Carrier is able to cross the junction.
* As electrons and holes both moves away from the junction, so depletion region widens. This creates more positive ions and hence more negative ions in n region. This is because of applied potential helps the Barrier potential as shown in below fig.



* Depletion region widens, barrier potential across the junction also increases, so the majority carrier holes from p to n electrons from n to p movement is stops.
* Due to increased Barrier potential, the positive side drags the electrons from p-region towards the positive of the battery, similarly negative side of barrier potential drags the holes from n-region towards the negative of battery.
* The electrons on p-side and holes on n-region towards +' are minority charge carriers, which constitutes the current in Reverse biased condition. This current is called "Reverse Saturation current" which is very small of the order of few microamphers for Ge, few nanoamphers for Si p-n junction diode.

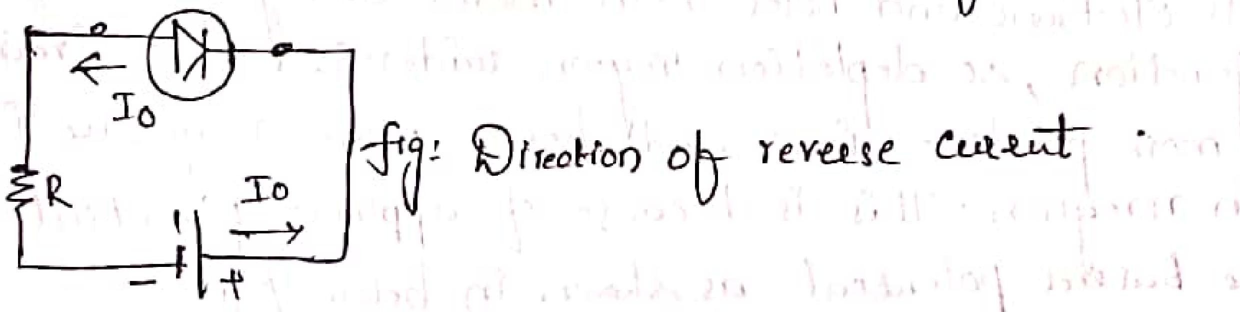


fig: Direction of reverse current.

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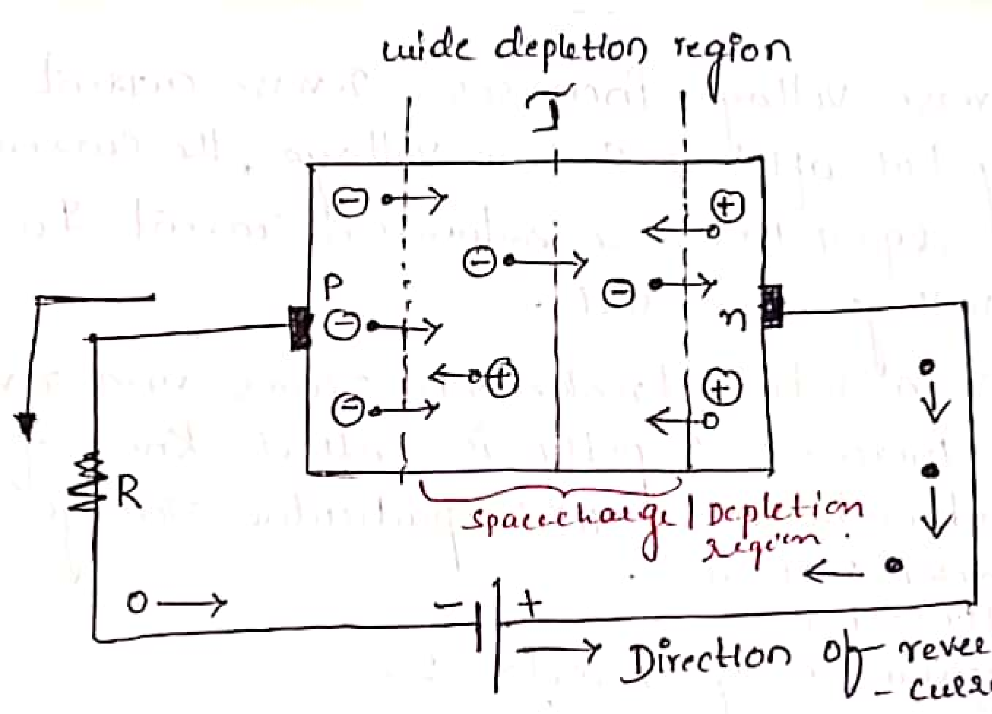

fig: flow of minority charge carriers in Reverse bias.

Reverse characteristics of p-n junction Diode :-

V_R
D
R
$V_R(V)$
Q
O
P
I_O (reverse saturation current).
reverse breakdown voltage
Breakdown
$I_R(\mu A)$

fig: Reverse biased diode.

The reverse voltage across the diode is V_R while the current flowing is reverse current. I_R flowing due to minority charge carriers. The graph of I_R Vs V_R is shown above.

* Reverse voltage is taken as negative because of applied polarity of reverse voltage is opposite to that of forward voltage.
* Reverse saturation current is also taken as "negative".

This can be plotted in third Quadrant

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* As reverse voltage increases, reverse current increases initially but after a certain voltage, the current remains constant equal to reverse saturation current I_o through reverse voltage increased.

* The point A where breakdown occurs and reverse current increases rapidly is called knee of the reverse characteristics. That particular voltage is called "Break-down voltage".

Diode Resistance (under R.B): —

Reverse Resistances of Diode :—

P-n junction offers large resistance in the reverse biased condition called "Reverse resistance".

These are 2 types.

1. Static reverse / Reverse static resistance
2. Reverse dynamic resistance.

(reverse-characteristics of diode (P-n diode): V_r (V), I_r (μA))

1. Reverse static / d.c resistance :—

It is ratio of applied reverse voltage to the reverse saturation current in p-n junction reverse bias condition. denoted by R_r

$$R_r = \frac{\text{Applied reverse voltage}}{\text{Reverse saturation current}} = \frac{OQ = V_o}{I_o}$$

2. Reverse Dynamic resistance :—

It is ratio of change in reverse voltage to change in reverse current.

$$r_r = \frac{\Delta V_R}{\Delta I_R} = \frac{\text{change in reverse voltage}}{\text{change in reverse current}}$$

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Complete V-I characteristics of a Diode :-

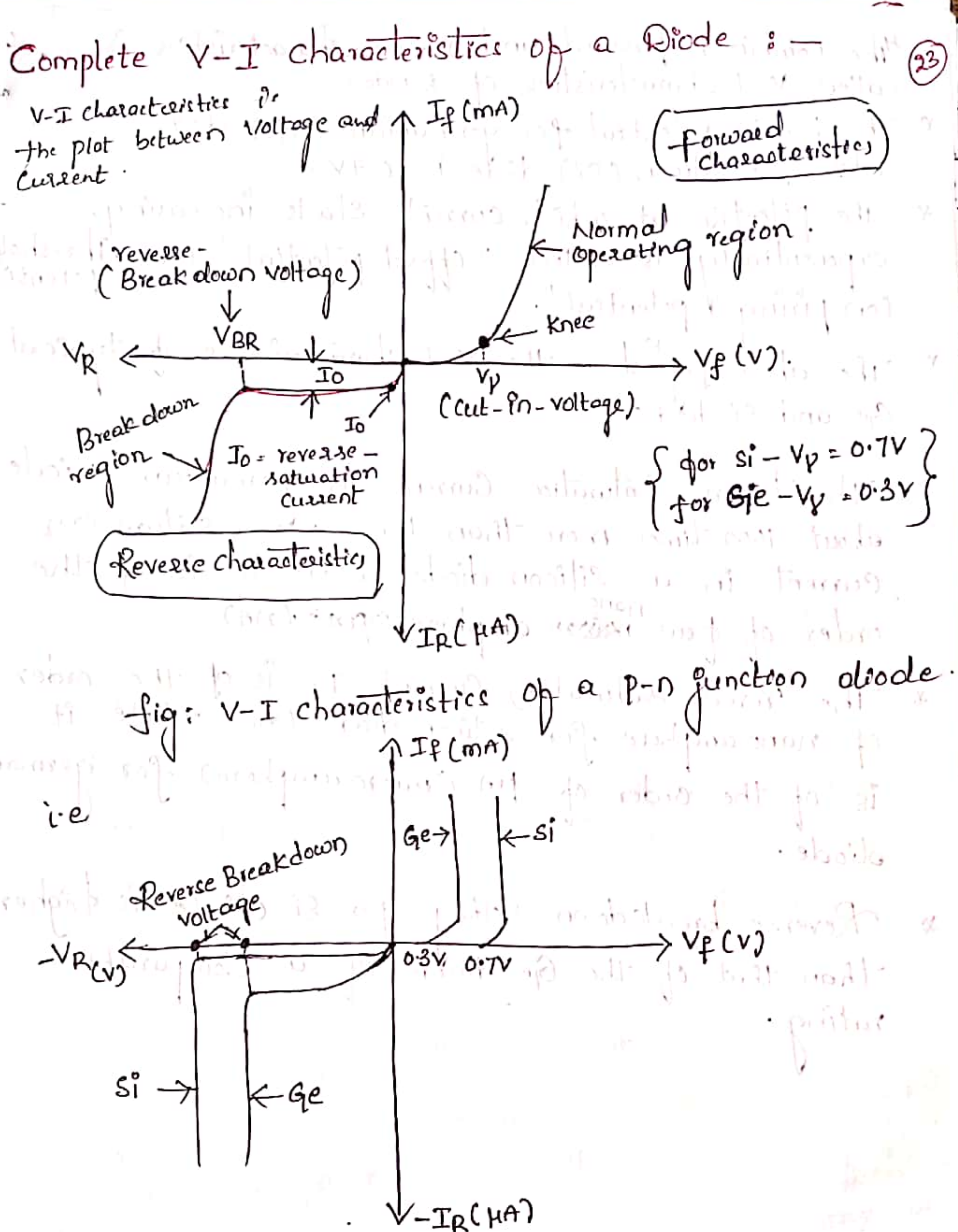

fig: V-I characteristics of a p-n junction diode.

i.e

Fig: V-I characteristics of typical Ge and Si diodes.

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* The Combined forward and reverse characteristics is called V-I characteristics of Diode.
* The Barrier potential for germanium (Ge) diode is 0.3V while for silicon (Si) diode is 0.7V.
* The potential at which current starts increasing exponentially is called "offset potential" (or) "Threshold potential" (or) firing potential".
* The above fig (b) shows the V-I characteristics of typical Ge and Si diodes.

* The Reverse Saturation Current in germanium diode is about 1000 times more than the reverse Saturation current in a Silicon diode while it is of the order of few nano amphere (nA)
* The reverse saturation Current I_0 is of the order of nano amphere for silicon diode (nA) while it is of the order of µA (micro amphere) for germanium diode.

* Reverse breakdown voltage for Si diode is higher than that of the Ge diode of a Comparable rating.

Diode Capacitance :-

* In PN Junction, the Depletion layer will be working as a parallel plate Capacitor.
* The width of the depletion layer changes during biasing. Therefore there are two types of Capacitance.
* These are,

1. Transition Capacitance (C_T) : during reverse bias
2. Diffusion Capacitance (C_D) : during forward bias

What is Capacitance :-

A Capacitor is a passive device Component that stores an "Electrical charge". The property of storing electric charge of capacitor is "Capacitance". Usually these having two conducting parallel plates there are seperated by "Di-electric".

C

≈

Q V

Insulating material di-electric.

Conducting plates (metals) Store charge

(Battery)

$$C = \frac{Q \text{ (coulombs)}}{V \text{ (volts)}} = \text{farads.}$$

Capacitance is ratio of charge stored on Capacitor to the voltage across the Capacitor.

Applied voltage

When the Capacitor is Connected to a Circuit with supply voltage source, two processes, which are called the charging & discharging Capacitor will happens in circuit specific Condition :

1. Transition Capacitance :-

* In Reverse bias Condition, the majority charge Carriers (electrons) in n-region and holes in p-region move away from the junction. This increases the "Width of the Depletion region".
* As the charged particles move away from the junction there Exists a change in charge with respect to the applied voltage.
* The change in charge 'dQ' with respect to the change in voltage 'dV' is nothing but "Capacitive Effect". Such Capacitance is called "Transition Capacitance". (or) "Space-charge Capacitance" (or) "Barrier Capacitance" (or) "Depletion layer Capacitance".
* It is Denoted by "C_T" it is given by

$$C_T = \frac{dQ}{dV}$$

P-Region | J | N-region

W = Width of depletion region.

Di-electric | plate 1 | plate-2.

C_T (Transition Capacitance)

V (Reverse bias voltage)

fig: Transition Capacitance in reverse bias Condition

This Capacitance is very important as it is not constant but depends on the magnitude of the reverse voltage. If 'W' is the width of the depletion region then the Transition Capacitance is given by,

$$C_T = \frac{\varepsilon A}{W}$$

permittivity means ability of a substance to store electrical energy in an "Electric field".

Where,

A = Area of Cross Section of the junction.
ε = permittivity of the Semiconductor.
W = width of Depletion region.

As the reverse bias applied to the diode increases, the width of the depletion region (W) increases. Thus the transition Capacitance C_T decreases. In short, the Capacitance can be Controlled by the applied voltage. The Variation of C_T with respect to the applied reverse bias voltage is shown in below.

fig: C_T against the Reverse voltage

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2. Diffusion Capacitance :—

⇒ During forward biased Condition, an another Capacitance comes into Existence Called "Diffusion-Capacitance" (or) "Storage Capacitance" denoted as "C_D".

* In forward biased condition, the width of the depletion region decreases and holes from p side get diffused in n-side while electrons from n-side move into p-side.
* As the Applied voltage increases, Concentration of injected charged particles increases.
* This rate of change of the injected charge with applied voltage is defined as a "Capacitance" called "Diffusion Capacitance".

$$C_D = \frac{dQ\,(C)}{dV\,(V)}$$

The Diffusion Capacitance can be determined by the Expression,

$$C_D = \frac{\tau I}{\eta V_T}$$

Where
τ = Mean life time for holes
η = proportionality constant.
V_T = Voltage equivalent at temperature.
I = forward Current.

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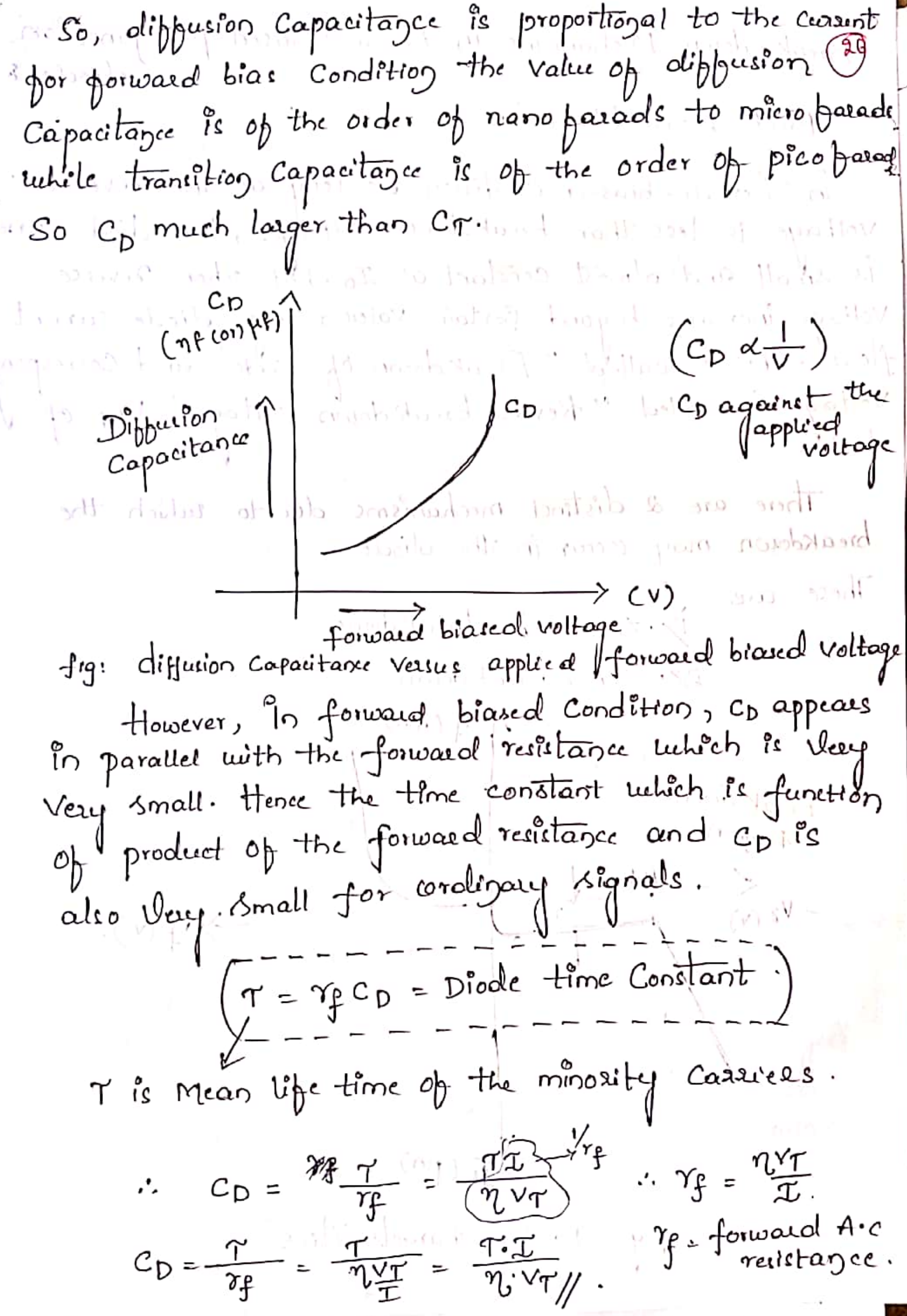

So, diffusion capacitance is proportional to the current. For forward bias condition the value of diffusion capacitance is of the order of nano farads to micro farads while transition capacitance is of the order of pico farads. So C_D much larger than C_T.

fig: diffusion capacitance versus applied forward biased voltage

However, in forward biased condition, C_D appears in parallel with the forward resistance which is very very small. Hence the time constant which is function of product of the forward resistance and C_D is also very small for ordinary signals.

$$\tau = r_f C_D = \text{Diode time Constant}$$

τ is Mean life time of the minority carriers.

$$\therefore \quad C_D = \frac{\tau}{r_f} = \frac{\tau I}{\eta V_T} \qquad \therefore r_f = \frac{\eta V_T}{I}$$

r_f = forward A.C resistance.

$$C_D = \frac{\tau}{r_f} = \frac{\tau}{\eta \frac{V_T}{I}} = \frac{\tau \cdot I}{\eta \cdot V_T}$$

∴ from the figure, the Current decreases towards the junction (I_{pp}) at the junction enters the n side and becomes I_{pn} which further decreases exponentially.

· Ily the current I_{nn} decreases towards the junction, at the junction enters the p-side and becomes I_{np} which also further decreases exponentially.

So, finally Conclusion is,

Sum of the currents Carried by electrons and holes at any point inside the diode always Constant equal to forward Current I.

Diode Current Equation :—

(V-I Characteristic equation of Diode).

The Diode Current equation is gives the relationship between voltage (V) and Current (I) is given by

$$I = I_0 \left(e^{\frac{V}{\eta V_T}} - 1\right)$$

Where,
- I : Diode Current
- I_0 : Diode reverse saturation Current at room temperature
- V = Voltage externally applied to the diode
- η = constant (1 for Ge, 2 for Si)
- V_T = Thermal voltage. = $\frac{KT}{q}$ volts

$V_T = \frac{KT}{q}$ $\boxed{V_T = KT}$ volts. 8.62×10⁻⁵ eV/°K

where K = Boltzmen Constant = 1.38066×10^{-23} J/K.

q = charge of e = 1.60019×10^{-19} C

At room temp - $T = 27° + 273° = 300°K$

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V-T characteristics ... [illegible]

$\therefore \quad V_T \simeq \frac{KT}{q} = \frac{T}{q/K} \simeq \frac{T}{11600}$ (where $\frac{q}{K} = \frac{1.6\times10^{-19}}{1.3\times10^{-23}} = 11600$)

at room temperature $V_T \simeq \frac{300}{11600}$

$\therefore$ At room temperature of 27°C i.e $T = 27+273 = 300^0K$ and the value of $V_T = 26\ mV$.

$V_T = K \cdot T$
$= 8.62\times10^{-5}\times300$
$= 0.02586 \simeq 0.026$
$V \simeq 26\ mV$ at room-temp.

V_T can be expressed as

$$V_T = \frac{T}{\left(\frac{1}{K}\right)} = \frac{T}{\left(\frac{1}{8.62\times10^{-5}}\right)} = \frac{T}{11600}$$

$$\left(V_T = \frac{T}{11600}\right)$$

for, forward biased V must be taken as positive and we get current I positive which is forward current.

for, reverse biased, V must be taken negative and we get negative current I which indicates that it is reverse current.

Current equation $I = I_0\left[e^{V/\eta V_T} - 1\right]$

divides by Area of cross-section of junction 'A' on both sides

$$\frac{I}{A} = \frac{I_0}{A}\left[e^{V/\eta V_T} - 1\right]$$

$$\therefore\ J = J_0\left(e^{V/\eta V_T} - 1\right)\ A/m^2.$$

where J = forward current density

J_0 = Reverse saturation current density.

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Nature of V-I characteristics from equation of diode :—

Consider a current equation of diode as

$$I = I_0 \left(e^{V/\eta V_T} - 1\right)$$

for forward bias :—

V is positive, so, $1 << e^{V/\eta V_T}$ (due to this exponential $V/\eta V_T$ → index has positive sign) hence neglect 1

we get,

$$I_f = I_0 e^{\frac{V}{\eta V_T}}$$

It indicates, once bias voltage exceeds cut in voltage, the forward current increases exponentially.

for Reverse bias :—

The bias voltage V is negative, due to this exponential index has negative sign.

so, $e^{-V/\eta V_T} << 1$ hence neglecting $e^{-V/\eta V_T}$

we get

$$I_R = I_0(-1) = -I_0$$

$$I_R = -I_0$$

It indicates under reverse bias, the current is negative indicating reverse saturation current which is negative indicating it flows in opposite direction to that of forward current.

i.e it flows in opposite direction to that of forward current.

I_f (mA), V_f (V), Knee, VBR, I_0, V_R (V), cut-in voltage, Breakdown, reverse saturation current, $-I_R$ (μA)

fig: V-I characteristics of p-n junction diode

Temperature Dependance on V-I Characteristic of Diode :-

V-I characteristics of diode is a plot between voltage and current variation. Temperature dependance on V-I characteristics of diode means how does the voltage and current of the diode can be change by changing the temperature. In this, we are seperately shows the what is the effect of temperature on current and what is the effect of temparature on voltage.

i.e., if we are increasing / decreasing temperature, the volt-amphere characteristics of diode changes significantly. This change in V-I characteristic is observe in both forward and reverse bias condition.

Let us consider V-I characteristics of Si-Diode.

I_f(mA)

125°C 25°C -75°C

Forward-Bias.

$-I_r$( ) V_f(V)

0.55V 0.7V 0.95V

100 amp.

Reverse bias

-75°C

10.24 μA

+25°C

+125°C

$-V_R$(V)

fig: Effects of Temperature on V-I characteristics

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Forward bias Condition :—

*** In Case of forward bias region, the characteristics of si-diode shift to the left at the rate of 2.5mv/°C (2.5mv per degree Centigrade) rise in temperature. and

if we decrease the temperature at the rate of 2.5mv/°C the characteristics of si- diode shifts to the right.

for ex :— $25^\circ C \longrightarrow V_f = 0.7V$,

$\Longrightarrow$ for $100^\circ C$ rise in temperature i.e., $100 + 25 = 125\,^\circ C$

$$\therefore V_f = 100 \times 2.5\,mV = 0.25\,V$$

i.e V_f reduced (↓) by 0.25 V.

new cut-in voltage across diode is reduced by 0.25v i.e

Temperature $\propto \frac{1}{V_\gamma}$

$$V_{f(new)_1} = (0.7 - 0.25)V$$

$$V_\gamma \rightarrow \boxed{V_{f(new)_1} = 0.45V}$$

$\Longrightarrow$ for $100^\circ C$ reduces in temperature i.e., $25 - 100^\circ C = -75^\circ C$

$$\therefore V_f = 100 \times 2.5\,mV = 0.25\,V$$

New voltage across diode is increased by 0.25v.

i.e., $(V_f)_{new_2} = (0.7 + 0.25)V$

$$V_\gamma \rightarrow \boxed{V_{f(new_2)} = 0.95V}$$

* i.e., If increase the temperature voltage across the diode is reduced, this is not reduced in voltage across the diode is not random. This voltage across the diode is not random voltage but it is equal to the barrier potential at this current rises exponentially.

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So, we can say Barrier potential is increases when decrease in temperature, Barrier potential is decreases when increase in temperature.

This new plot of forward V-I characteristics shows below:

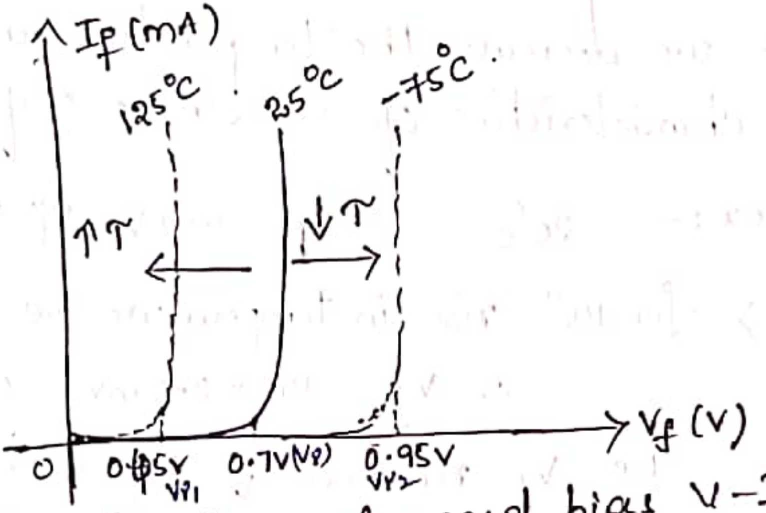

fig: Temperature Effect on forward bias V-I characteristics of diode.

Reverse bias Condition :—

In this condition, positive terminal is connected to n-type negative terminal of battery is connected to p-type

Let us take a connection of diode in reverse bias:

P N

I_0

Leakage current / reverse saturation current.

V_R

(−) (+)

V_R is negative.

For reverse bias condition :→

** "The Reverse saturation Current I_0 (or) I_s doubles for every 10°C rise in temperature."

Ex: Case (1) for 100°C rise in temperature to 25°C

i.e 100 + 25 = 125°C.

We know that for every 10°C rise in temperature reverse saturation current doubles.

i.e

25°C ⟶ 10 nA
35°C ⟶ 20 nA
45°C ⟶ 40 nA
55°C ⟶ 80 nA
⋮ 160, 320, 640, 1280
125°C ⟶ 10,240 nA (or) 10.24 μA.

∴ The new reverse saturation current (I_s) is 10.24 μA.

i.e I_s (reverse-saturation current) increases if we increase in temperature.

Similarly, by using same above process, if we calculate at −75°C i.e decreasing temperature at +25°C

i.e +100°C ~~+25~~. 25°C − 100°C = −75°C.

for every 10°C reduce in temperature the reverse saturation current also reduces, very small current.

i.e Temperature increases ⟶ Reverse saturation current increases.

Temperature decreases ⟶ Reverse saturation current decreases.

Breakdown voltage at 25°C

∴ The Reverse breakdown voltage of diode may increase (or) decreases depends on Zener potential. ~~It may incr.~~ We have to be careful in reverse bias condition, I_s increases if we increase in temperature it will damage the diode. The reverse saturation current should be closed to 10 pamp for high temperature applicatio.

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I_s closer to 10 pA → for High temperature applications.

In Case of 'Ge' the reverse saturation Current is high so we ~~can't~~ not prefer Ge in practical applications. for Si have reverse saturation Current is less than the 'Ge'.

The temperature dependance on voltage & Current Can be taken by the following equations
We know Diode equation of Current $I = I_0(e^{V/\eta V_T} - 1)$.

for Current :-

$$I_{02} = I_{01}\, 2^{(T_2 - T_1)/10}$$

where $T_2 = T_1 + 10$

I_{01}, I_{02} are the effects of reverse saturation Current I_0

I_{01} = Value of I_0 at temperature T_1
I_{02} = value of I_0 at temperature T_2.

$T_2 = T_1 + 10$

i.e for every 10°C rise in temperature current gets doubled.

for Voltage :-

$$\frac{dV}{dT} = -2.5\ \text{mV}/C^o$$

For every one degree Centigrade rise in temperature the cut-in voltage of diode decreased by 2.5 mV.

$-V_R$ (V)
small current 100A
10.24 µA
-75°C
25°C
125°C
$-I_R$ (µA)

Effect of Temperature on (V-I) characteristic of Reverse bias Condition.

PROBLEMS - on Diode Current Equation

*1. A Silicon diode has a reverse Saturation Current of 7.12 nA at room temperature of 27°C. Calculate its forward current if it is forward biased with the voltage of 0.7 V ?

Given that,

Reverse saturation Current $= I_0 = 7.12\ nA = 7.12 \times 10^{-9} A$

Applied voltage $V = 0.7V$

At room temperature of 27°c mean

$$T = 27°c + 273 = 300°K$$

for Silicon diode $V_D = 0.7V$ and $\eta = 2$.

The Diode - current equation is

$$I = I_0\left[e^{(V/\eta V_T)} - 1\right]$$

$$= 7.12 \times 10^{-9}\left[e^{\frac{0.7}{2 \times V_T}} - 1\right]$$

$$= 7.12 \times 10^{-9}\left[e^{\frac{0.7}{2 \times 0.026}} - 1\right]$$

$$= 7.12 \times 10^{-9}\left(e^{13.461} - 1\right)$$

$$= 7.12 \times 10^{-9}\left(700,815.545 - 1\right)$$

$$= 7.12 \times 10^{-9}\left(700,814.545\right)$$

$$= 4,989,799.56 \times 10^{-9}$$

$$= 4.989 \times 10^{6} \times 10^{-9}$$

$$I = 4.98 \times 10^{-3} \approx 4.98\ mA \approx 5\ mA$$

where

$V_T = K.T$

at room temp

$V_T = 8.62 \times 10^{-5} \times 300$

$= 0.0258V$

$V_T = 0.026\ V$.

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② The voltage across a Silicon diode at room temperature of 300°K is 0.71 V when 2.5 mA current flows through it. If the voltage increases to 0.8 V, Calculate the New diode current?

The Current equation of diode is

$$I = I_o\left(e^{V/\eta V_T} - 1\right)$$

At 300°K $\quad V_T = 26\,mV = 26 \times 10^{-3}\,V$

$V = 0.71\,V$ for $I = 2.5\,mA$, $\eta = 2$ for si

$$\therefore \quad 2.5 \times 10^{-3} = I_o\left[e^{\left(\frac{0.71}{2 \times 26 \times 10^{-3}}\right)} - 1\right]$$

$$2.5 \times 10^{-3} = I_o\left[e^{13.653} - 1\right]$$

$$2.5 \times 10^{-3} = I_o\left[850{,}007.116 - 1\right]$$

$$2.5 \times 10^{-3} = I_o\left[850{,}006.116\right]$$

$$I_o = \frac{2.5 \times 10^{-3}}{850{,}006.116}$$

$$= \frac{2.5 \times 10^{-3}}{8.5 \times 10^{5}} = \frac{2.5}{8.5} \times 10^{-3} \times 10^{-5}$$

$$= 0.294 \times 10^{-8} = 0.294 \times 10^{-8} \times \frac{10}{10}$$

$$I_o = 2.94 \times 10^{-9}$$

Now $V = 0.8\,V$.

$$I = 2.93 \times 10^{-9}\left[e^{\left(\frac{0.8}{2 \times 26 \times 10^{-3}}\right)} - 1\right]$$

$$= 2.93 \times 10^{-9}\left(e^{15.38} - 1\right)$$

$$= 2.93 \times 10^{-9}\left(4780233.73 - 1\right)$$

$$= 2.93 \times 10^{-9} \times 4780232.73$$

$$= 2.93 \times 10^{-9} \times 4.78 \times 10^{6}$$

$$I = 14.0054 \times 10^{-3} \simeq 14.1\,mA$$

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(3) A Ge diode has a reverse Saturation Current of 3 μA. Calculate the forward bias voltage at the room temperature of 27 °C and 1% of the rated Current is flowing through the forward biased diode. The Diode forward rated Current is 1A ?

Given values are

$I_0 = 3\ \mu A$

$T = 27^\circ C = 27 + 273 = 300^\circ K$

$\eta = 1$

$I_{rated} = 1A$ for diode

$\therefore I = 1\%$ of I_{rated}

$I = 1/100 \times (1) = 0.01A$

$V_T = KT = 8.62 \times 10^{-5} \times 300 = 0.026V$

According to Diode equation

$$I = I_0 \left(e^{V/\eta V_T} - 1\right)$$

$$0.01 = 3 \times 10^{-6} \left(e^{V/1 \times 0.026} - 1\right)$$

$$3333.333 = e^{\frac{V}{0.026}} - 1$$

$$e^{\frac{V}{0.026}} = 3333.333 + 1$$

$$e^{V/0.026} = 3334.333$$

.... Taking Natural log on both sides

$$\ln\left(e^{V/0.026}\right) = \ln(3334.333)$$

$$\frac{V}{0.026} = 8.112$$

$$V = 8.112 \times 0.026$$

$$\boxed{V = 0.2109V}$$

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4) A Diode operating at 300°K at a forward voltage of 0.4V carries a current of 10 mA. When voltage is changed to 0.42V, the current becomes twice, Calculate the value of reverse saturation current and η for the diode?

$V_1 = 0.4V$, $I_1 = 10\ mA$

$V_2 = 0.42V$, $I_2 = 2I_1 = 2\times 10 = 20\ mA$.

Now, $I = I_0\left(e^{\frac{V}{\eta V_T}} - 1\right)$

$$10\times 10^{-3} = I_0\left(e^{\frac{0.4}{\eta\times 26\times 10^{-3}}} - 1\right) \longrightarrow (1)$$

$$20\times 10^{-3} = I_0\left(e^{\frac{0.42}{\eta\times 26\times 10^{-3}}} - 1\right) \longrightarrow (2)$$

In forward bias condition $1 << e^{V/\eta V_T}$ .. neglecting 1.

$$\therefore\ 10\times 10^{-3} = I_0\, e^{\frac{15.38}{\eta}} \longrightarrow (3)$$

$$\therefore\ 20\times 10^{-3} = I_0\, e^{\frac{16.153}{\eta}} \longrightarrow (4)$$

Dividing (3) by (4)

$$\frac{1}{2} = \frac{e^{15.38/\eta}}{e^{16.153/\eta}}$$

$$2e^{15.38/\eta} = e^{16.153/\eta}.$$

Taking Natural Logarithm of both sides

$$\frac{16.153}{\eta} = \ln 2 + \frac{15.384}{\eta}$$

$$\frac{1}{\eta}(16.153 - 15.384) = 0.6931$$

$$\eta = 1.109$$

$$I_0 = 9.45\ nA$$

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5. A Silicon diode has a Saturation Current of 7.5 μA at room temperature 300K. Calculate the Saturation Current at 400K ?

Given $I_{01} = 7.5 \times 10^{-6}$ A at $T_1 = 300K \Rightarrow 27°C + 273K$.

$T_1 = 27°C$

lly $T_2 = 400K = 127°C + 273K$.

$T_2 = 127°C$

∴ The Saturation Current at 400K is

$$I_{02} = I_{01} \times 2^{(T_2 - T_1)/10}$$

$$= 7.5 \times 10^{-6} \times 2^{(127-27)/10}$$

$$I_{02} = 7.5 \times 10^{-6} \times 10^{10} = 7.68 \text{ mA}$$

6. The Reverse Saturation current of the ~~transistor~~ diode is 2 μA at room temperature of 25°C and increases by a factor of 2 for each temperature of 10°C. Find the reverse saturation Current of the ~~transistor~~ diode at a temperature of 75°C ?

Given $I_{01} = 2\,\mu A$ at $T_1 = 25°C$, $T_2 = 75°C$

∴ The Reverse Saturation Current of the transistor at $T_2 = 75°C$ is

$$I_{02} = I_{01} \times 2^{(T_2 - T_1)/10} = 2 \times 10^{-6} \times 2^{\left(\frac{75-25}{10}\right)}$$

$$= 2 \times 10^{-6} \times 2^5 = 64\,\mu A$$

$$I_{02} = 64\,\mu A$$

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Problems on Resistance (Static/DC and Dynamic/AC)

1. Find the value of DC resistance and ac resistance of a germanium junction diode at 25°C with I_0 is 25 μA and at an applied voltage of 0.2V across the diode?

Given $I_0 = 25\mu A$

$T = 25°C = 25 + 273 = 298\ K$

$V = 0.2V$

$$\therefore I = I_0 \left(e^{V/\eta V_T} - 1\right)$$

$$= 2.5 \times 10^{-6} \left(e^{\frac{0.2}{26 \times 10^{-3}}} - 1\right)$$

$I = 54.79 mA$.

DC resistance :-

$$R_f = \frac{V_f}{I_f}$$ → for forward bias.

$$R = \frac{V}{I} = \frac{0.2V}{54.79mA} = 3.65\Omega \qquad (R = 3.65\Omega)$$

AC resistance :-

For Ge ⇒ $\eta = 1$ $\quad V_T = \frac{KT}{q} = 25.71\ mV$

A.C resistance $$r_f = \frac{\eta V_T}{I}$$ → under reverse bias

$$r_f = \frac{\eta V_T}{I} = \frac{25.71 \times 10^{-3}}{54.79 \times 10^{-3}}$$

$$\therefore r_F = 0.47\Omega$$

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2. Calculate the Dynamic forward and reverse resistance of a PN junction diode when the applied voltage is 0.25V at T = 300K given $I_0 = 2\mu A$.

(150)

Given $V = 0.25\,V$

$T = 300K$

$I_0 = 2\mu A$

At $T = 300K$, $V_T = 26\,mV$

Assuming it to be silicon diode $\eta = 2$

$$\therefore \quad I = I_0\left(e^{V/\eta V_T} - 1\right)$$

$$= 2\times10^{-6}\left(e^{0.25/2\times26\times10^{-3}} - 1\right)$$

$$\boxed{I = 0.24\,mA}$$

For Ge diode, $\eta = 1$

$$I = I_0\left(e^{V/\eta V_T} - 1\right)$$

$$= 2\times10^{-6}\left(e^{\frac{0.25}{26\times10^{-3}}} - 1\right)$$

$$\boxed{I = 0.03\,A}$$

$$r_f = \frac{\eta V_T}{I} = \frac{26\times10^{-3}}{0.03} = 0.867\,\Omega$$

$$\boxed{r_f = 0.867\,\Omega}$$

Reverse Resistance $(r_f) = \frac{V}{I_0} = \frac{0.25}{2\times10^{-6}} = 125\,K\Omega$.

$$\boxed{r_f = \frac{V}{I_0}} \qquad \boxed{r_f = 125\,K\Omega}$$

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* The voltage across a Si - Diode at room temperature (300K) is 0.7 volts when 2 mA current flows through it. If the voltage increases to 0.7V. Calculate the diode current (assume $V_T = 26mV$).

Given data

at room temperature $T = 300k$

Voltage across a silicon diode $V_{D1} = 0.7V$

Current through the diode $I_{D1} = 2\ mA$

When voltage increases to 0.75V V_{D2} then,

$$\frac{I_{D2}}{I_{D1}} = \frac{I_0(e^{V_{D2}/\eta V_T} - 1)}{I_0(e^{V_{D1}/\eta V_T} - 1)}$$

$$= \frac{(e^{(0.75/2 \times 25.7 \times 10^{-3})} - 1)}{(e^{0.7/2 \times 25.7 \times 10^{-3}} - 1)} = \frac{2172608.828}{821326.3605}$$

$$= 2.64$$

$$\therefore \frac{I_{D2}}{I_{D1}} = 2.64 \quad (\text{where } I_{D1} = 2\ mA)$$

$$I_{D2} = I_{D1} \times 2.64 = 2.64 \times 2 \times 10^{-3}$$

$$I_{D2} = 5.3\ mA$$

(5). A Silicon diode has a Saturation Current of 7.5 μA at room temperature 300K. Calculate the Saturation Current at 400K ?

Given $I_{01} = 7.5 \times 10^{-6}$ A at $T_1 = 300K \Rightarrow 27^{\circ C} + 273K$.

$T_1 = 27^{\circ}C$

lly $T_2 = 400K = 127^{\circ C} + 273^{K}$.

$T_2 = 127^{\circ}C$

∴ The Saturation Current at 400K is

$$I_{02} = I_{01} \times 2^{(T_2 - T_1)/10}$$

$$= 7.5 \times 10^{-6} \times 2^{(127-27)/10}$$

$$I_{02} = 7.5 \times 10^{-6} \times 10^{10} = 7.68 \text{ mA}$$

(6). The Reverse Saturation current of the ~~transistor~~ diode is 2 μA at room temperature of 25°C and increases by a factor of 2 for each temperature of 10°C. Find the reverse saturation Current of the ~~transistor~~ diode at a temperature of 75°C ?

Given $I_{01} = 2 \mu A$ at $T_1 = 25^{\circ}C$, $T_2 = 75^{\circ}C$

∴ The Reverse Saturation Current of the transistor at $T_2 = 75^{\circ}C$ is

$$I_{02} = I_{01} \times 2^{(T_2 - T_1)/10} = 2 \times 10^{-6} \times 2^{\left(\frac{75-25}{10}\right)}$$

$$= 2 \times 10^{-6} \times 2^{5} = 64 \mu A$$

$$I_{02} = 64 \mu A$$

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2(A) RECTIFIERS

Concept of Rectifiers :-

- What is Rectifier
- What is the need of Rectifier
- Block diagram of Rectifier & characteristics
- Types of Rectifiers (Different types - Circuits, operation, wave-form)
- Derivations of characteristics of Rectifiers
- Comparison of Rectifiers
- Applications, Advantages, Disadvantages of all types of Rectifiers.

1 Rectifiers :-

Definition :- A Rectifier is a device which converts a.c voltage to pulsating d.c voltage, using one or more p-n junction diodes.

(or)

Rectifier is a device which converts an Bi-directional a.c signal into uni-directional d.c signal.

2. Need of Rectifiers :-

Rectifiers are the power electronic circuits which converts AC power (which is available from the power sockets in home) in to DC power (which is available from batteries). The advantage of DC power over AC power is it (DC) can be stored in batteries where as AC power can't be stored. So every portable electronic device requires a battery to run it. So batteries in turn requires DC power to charge them. So in order to charge the batteries in your portable electronic devices like mobile phones, laptops, etc (The ones with battery in it). Rectifiers are used to convert bidirectional a.c to uni-directional d.c.

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Characteristics of Rectifiers :-

The important points to be studied while analyzing the Various rectifier Circuits are,

a). Waveform of the load Current

b). Regulation of the output voltage (study the effect of change in load current on the load voltage)

c). Rectifier Efficiency (How efficiently the rectifier circuit converts a.c into d.c

d). peak value of current in the rectifier Circuit (maximum value of current - decides rating of rectifiers)

e). peak value of voltage across the rectifier element in the reverse direction (PIV)

f). Ripple factor (amount of A.C component in output of rectifier)

Block diagram of Rectifier :-

230V, 50Hz A.C signal → Transformer → Bi-directional a.c signal → Rectifier → uni-directional d.c signal as output

Transformer: (step up / stepdown) transformer

Rectifier: (resistors & diodes)

fig: Rectifier Block - diagram

Rectifiers are used for rectification of a.c signal (voltage) and Converts into d.c. The above (correction of errors) and Converts into d.c. The above figure shows block diagram of Rectifier. In this first block is "Transformer". Transformer is used to bring the level of a.c voltage, if we want to increase the level of a.c voltage we use "step-up-transformer". If we decrease the level of a.c voltage we use "step-down transformer". AC signal (voltage 230V, 50Hz for India) is applied to the Transformer

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The output of transformer is given to the input of or the Rectifier block. Rectifier is used for "Rectification (i.e process of correcting error of a.c for converting into d.c). In rectifiers we are using resistors and diodes. It converts an a.c signal into "pulsating d.c / uni-directional d.c".

Types of Rectifiers :-

Using one or more diodes, rectifiers are classified into 3-types. Those are

Rectifiers
- Half-Wave Rectifier
- Full-wave rectifier
- Bridge-wave rectifier

1. Half-wave rectifier :-

Fig: Half-wave rectifier circuit.

* In Half wave rectifier, rectifying element conducts only positive half cycle of input a.c supply.
* The negative half cycles of a.c supply are eliminated from the output.

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* This rectifier circuit consists of resistive load, rectifying element i.e p-n junction diode., and the source of a.c voltage, all are connected in series.
* Usually the rectifier circuits are operated from ac main supply
* To obtain the desired d.c, the a.c voltage is applied to rectifier circuit using suitable step-up or step-down transformer, mostly a step-down one, with necessary turns ratio.
* The input voltage (230V) of half-wave rectifier is a sinusoidal a.c voltage, having a frequency (50Hz).

i.e $e_s = E_{sm} \sin \omega t \longrightarrow (1)$ ($\omega = 2\pi f$, f = supply frequency)

Transformer decides peak value of secondary voltage E_{sm}

i.e peak value of primary voltage is E_{pm}

$$\therefore \frac{N_2}{N_1} = \frac{E_{sm}}{E_{pm}} = \frac{V_{sm}}{V_{pm}} \Rightarrow \frac{\text{Secondary Maximum Voltage}}{\text{Primary Maximum Voltage}}$$

Where E_{sm} = The peak value of the secondary a.c voltage

N_1 = primary number of turns

N_2 = secondary number of turns

Operation :— The Half-wave rectifier operation is done by considering 2 cases

(i) By applying positive half cycle as input

(ii) By applying negative half cycle as input

i.e during positive half cycle – Diode acts as forward bias

and during negative half cycle – Diode acts as Reverse-bias

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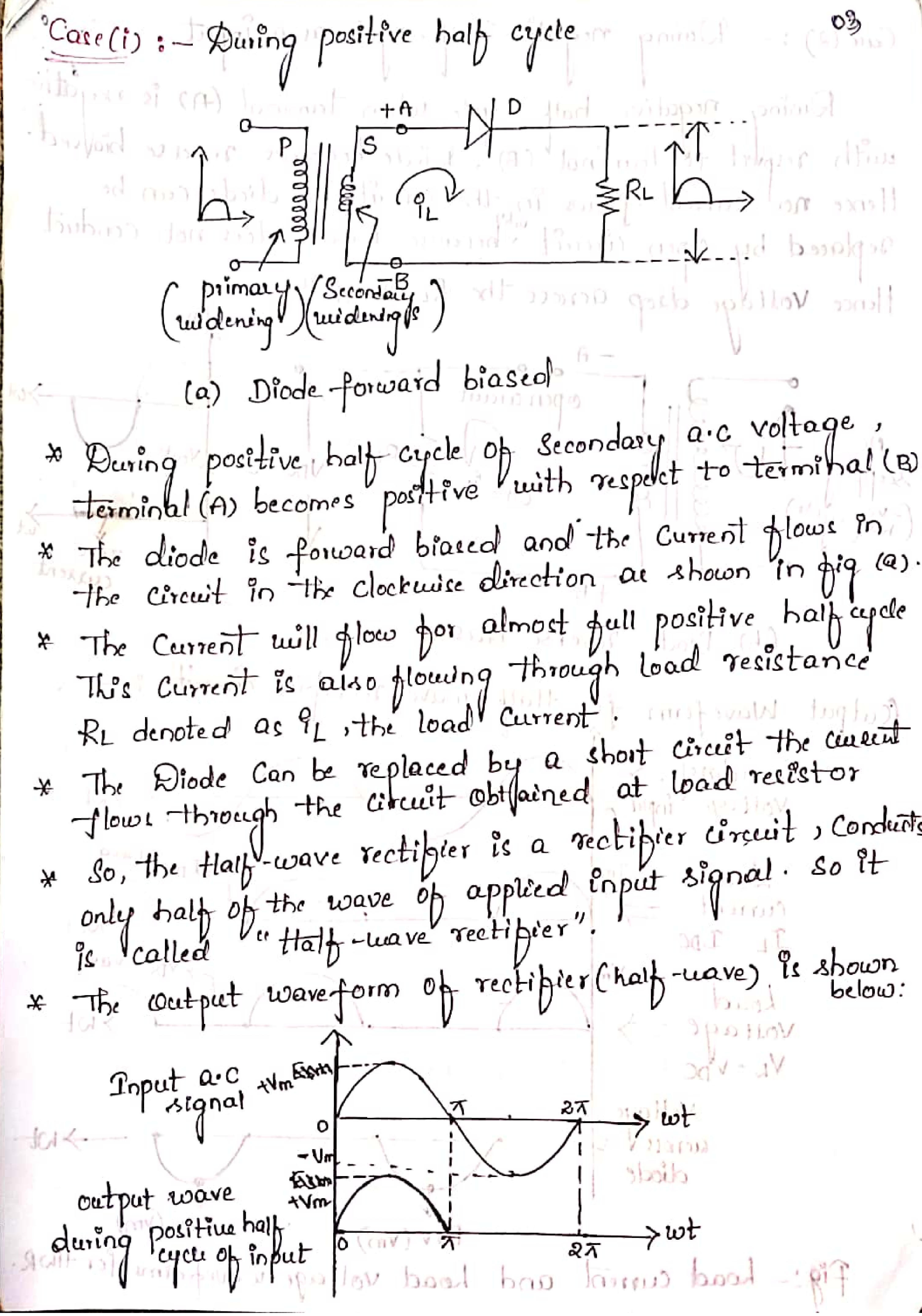

Case (i) :- During positive half cycle

(a) Diode forward biased

* During positive half cycle of secondary a.c voltage, terminal (A) becomes positive with respect to terminal (B).
* The diode is forward biased and the current flows in the circuit in the clockwise direction as shown in fig (a).
* The current will flow for almost full positive half cycle. This current is also flowing through load resistance R_L denoted as i_L, the load current.
* The Diode can be replaced by a short circuit the current flows through the circuit obtained at load resistor.
* So, the Half-wave rectifier is a rectifier circuit, conducts only half of the wave of applied input signal. So it is called "Half-wave rectifier".
* The output waveform of rectifier (half-wave) is shown below:

Case (2) :- During negative half-cycle as a input

During negative half-cycle when terminal (A) is negative with respect to terminal (B). Diode becomes reverse biased. Hence no current flows in the circuit i.e diode can be replaced by open circuit, why? because Diode does not conduct. Hence voltage drop across the R_L is zero

−A

open circuit

AC supply (−ve half cycle)

R_L

$0A = i_L$

$V_{DC} = 0$

+B

V_{in}

ωt

V_{out}

ωt

zero current

(b) Diode reverse biased

Output Waveform for Half-wave rectifier circuit :-

Secondary voltage = input ⇒

V_m

0

ωt

Load current $I_L = I_{DC}$ ⇒

I_m

$I_{DC} = I_{avg}$

ωt

Load voltage $V_L = V_{DC}$ ⇒

V_m

$V_{DC} = V_{avg}$

ωt

Voltage across diode →

ωt

PIV (V_m)

PIV (V_m)

Fig :- Load current and Load voltage waveforms for HWR.

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The D.C wave form is expected to be a straight line but on the half-wave rectifier gives output in the form of positive sinusoidal parts.

Hence, the output is called "pulsating D.C". it is discontinuous in nature. Hence it is necessary to calculate the average value of load current and average value of output voltage.

Derivations of characteristics of Half-wave rectifier :-

1. Average D.C Load current (I_{DC})
2. Average D.C Load Voltage (V_{DC})
3. R.M.S Value of Load current (I_{RMS})
4. R.M.S Value of Load Voltage (V_{RMS})
5. D.C power output (P_{DC})
6. A.C power input (P_{AC})
7. Rectifier Efficiency (η)
8. Ripple factor (γ)
9. Load current (i_L)
10. peak Inverse voltage (PIV)
11. Transformer utilization factor
12. Voltage Regulation (%R)

These are the various important characteristics of Half-wave rectifier circuit. The derivations of these all are as follows.

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1. Average D.C Load Current :-

The Average (or) D.C Value of alternating current is obtained by "integration".

For finding the average value of an alternating wave-form we have to determine the area under the curve one complete cycle i.e from 0 to 2π and then dividing it by the base i.e 2π.

Mathematically, current wave-form can be described as,

$$i_L = I_m \sin\omega t \quad \text{for } 0 \leq \omega t \leq \pi$$
$$= 0 \quad \text{for } \pi \leq \omega t \leq 2\pi$$

where

I_m = peak value of load current

$$I_{DC} = \frac{1}{2\pi}\int_0^{2\pi} i_L \, d(\omega t)$$

$$= \frac{1}{2\pi}\int_0^{2\pi} (I_m \sin\omega t)\, d\omega t$$

As no current flows during negative half cycle of a.c input voltage i.e between $\omega t = \pi$ to $\omega t = 2\pi$, we change the limits of integration.

$$\therefore I_{DC} = \frac{1}{2\pi}\int_0^{\pi} I_m \sin\omega t \, d\omega t + \frac{1}{2\pi}\int_{\pi}^{2\pi} I_m \sin\omega t \, d\omega t \rightarrow 0$$

$$= \frac{1}{2\pi}\int_0^{\pi} I_m \sin\omega t \cdot d\omega t$$

$$= \frac{1}{2\pi} I_m \left(\int_0^{\pi} \sin\omega t \cdot d\omega t\right)$$

$$= \frac{I_m}{2\pi}(-\cos\omega t)_0^{\pi} = \frac{-I_m}{2\pi}(\cos\pi - \cos 0)$$

$$= \frac{-I_m}{2\pi}(-1-1) = \frac{-I_m}{2\pi}(-2) = \frac{I_m}{\pi}$$

$$\therefore I_{DC} = I_m/\pi$$

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$$\left(I_{DC} = \frac{I_m}{\pi} = \text{Average Value}\right)$$

Where $I_m = \dfrac{V_m}{R_f + R_s + R_L}$

where R_s = Resistance of Secondary winding of transformer

R_f = forward resistance of diode

R_L = load Resistance

I_m = Maximum (or) peak value of current.

V_m = Maximum (or) peak Value of voltage.

Note :– if R_s, R_f are given then we consider these values if these are not given then neglected while calculating

i.e $\left(I_m = \dfrac{V_m}{R_L}\right)$ $\left(\because R_s, R_f << R_L - \text{neglect } R_s, R_f\right)$.

2). Average D.C Load voltage :–

It is the product of average (or) D.C load current and the load resistance R_L.

$$V_{DC} = I_{DC} \cdot R_L$$

$$= \frac{I_m}{\pi} \cdot R_L \quad \left(\because \text{where } I_{DC} = \frac{I_m}{\pi}\right)$$

$$V_{DC} = \frac{V_m}{\pi(R_f + R_s + R_L)} \cdot R_L \quad \left(\because I_m = \frac{V_m}{R_L + R_s + R_f}\right)$$

R_s, R_f are practically very small so neglect these.

$$V_{DC} = \frac{V_m}{R_L \cdot \pi} R_L = \frac{V_m}{\pi} \quad \therefore \left(V_{DC} = \frac{V_m}{\pi}\right)$$

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3. R.M.S Value of Load current (I_{RMS}) :-

The R.M.S means squaring, finding mean and then finding square root. Hence R.M.S value of load current can be obtained as,

$$I_{R.M.S} = \sqrt{\frac{1}{2\pi}\left(\int_0^{\pi}(I_m \sin\omega t)^2 d\omega t\right)}$$

$$= \sqrt{\frac{1}{2\pi}\int_0^{\pi} I_m^2 \sin^2\omega t \cdot d(\omega t)} \qquad \left(\sin^2\omega t = \frac{1-\cos 2\omega t}{2}\right)$$

$$= I_m\sqrt{\frac{1}{2\pi}\int_0^{\pi}\left(\frac{1-\cos 2\omega t}{2} d\omega t\right)}$$

$$= I_m\sqrt{\left(\frac{\omega t}{2} - \frac{\sin 2\omega t}{2\times 2}\right)_0^{\pi}} \qquad (\text{as } \sin 2\pi = \sin(0) = 0)$$

$$= I_m\sqrt{\frac{1}{2\pi}\left(\frac{\pi}{2} - 0\right)}$$

$$= I_m\sqrt{\frac{1}{4}}$$

$$I_{RMS} = \frac{I_m}{2}$$

4. R.M.S. Value of load voltage :-

$$V_{R.M.S} = (I_{R.M.S}) R_L$$

$$= \frac{I_m}{2} \cdot R_L \qquad \left(R_s, R_f << R_L \text{ neglect } R_s, R_f\right)$$

$$= \frac{V_m}{2(R_L + R_s + R_f)} \cdot R_L$$

$$= \frac{V_m}{2 R_L} \cdot R_L = \frac{V_m}{2} \qquad V_{Rms} = \frac{V_m}{2}$$

5. D.C power Output (P_{DC}) :-

The D.C power output can be obtained as,

$$P_{DC} = V_{DC} \cdot I_{DC}$$

According to ohm's law ($\because V_{DC} = I_{DC} \cdot R_L$)

$$= (I_{DC} \cdot R_L) \cdot I_{DC}$$

$$P_{DC} = (I_{DC})^2 \cdot R_L$$

Dc power output $= I_{DC}^2 \cdot R_L = \left(\frac{I_m}{\pi}\right)^2 R_L = \frac{I_m^2}{\pi^2} R_L$

$$P_{DC} = \frac{I_m^2}{\pi^2} R_L \quad \text{where } I_m = \frac{V_m}{R_L + R_s + R_f}$$

$$P_{DC} = \frac{V_m^2 \cdot R_L}{\pi^2 (R_f + R_s + R_L)^2}$$

$$P_{DC} = \frac{V_m^2 \cdot R_L}{\pi^2 \times R_L^2} = \frac{V_m^2}{\pi^2 \cdot R_L}$$

$$\boxed{P_{DC} = \left(\frac{V_m}{\pi}\right)^2 \left(\frac{1}{R_L}\right)}$$

6. A.C power input :-

The power input taken from the Secondary of transformer is the power supplied to three resistances namely load-resistance R_L, the diode resistance R_f, winding resistance R_s. The a.c power is given by,

$$P_{AC} = I_{Rms}^2 [R_L + R_f + R_s]$$

($\because P_{AC} = I_{AC} \cdot V_{AC} = I_{AC}(I_{AC} R_L)$)

$$P_{AC} = I_{AC}^2 \cdot R_L$$

$$\left(P_{AC} = I_{rms}^2 \cdot R_L\right)$$

$$(I_{AC} = I_{rms})$$

but $I_{rms} = \frac{I_m}{2}$

$$\therefore \boxed{P_{AC} = \frac{I_m^2}{4} (R_L + R_f + R_s)}$$

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6. Rectifier Efficiency (η) :—

The rectifier efficiency is defined as the ratio of output d.c power to input a.c power

$$\eta = \frac{\text{D.C output power}}{\text{A.C input power}} = \frac{P_{DC}}{P_{AC}}$$

$$\eta = \frac{\left(I_m^2/\pi^2\right) \cdot R_L}{\frac{I_m^2}{4}\left[R_L+R_S+R_f\right]} = \frac{\left(4/\pi^2\right) R_L}{R_f+R_S+R_L}$$

$$\eta = \frac{0.406}{1+\left(\frac{R_f+R_S}{R_L}\right)}$$

→ Efficiency is 0.406, this formula is used when R_f, R_s are given during calculation

If R_S, R_f are very small practically so neglect it then

$$\eta = \frac{\left(4/\pi^2\right) \cdot R_L}{R_L+R_S+R_f} = \frac{4}{\pi^2} = 0.406$$

($R_S \to 0$, $R_f \to 0$)

$$\eta = 0.406$$

Percentage of efficiency ($\% \eta$) $= 0.406 \times 100$

$= 40.6\%$

$$\% \eta = 40.6\%$$

Thus, In HWR, maximum 40.6% a.c power gets converted to d.c power at the load. The remaining 60% of power is present interms of ripples in the output which is fluctuating component (pulsating D.C).

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7. Ripple factor :-

It is seen that the output of half wave rectifier is not pure d.c but a pulsating d.c. The output contains pulsating components called "Ripples". The measure of such ripples present in the output is with the help of factor called "Ripple factor". it is denoted by γ (or) Γ (gama) :
it tells how smooth is the output.

* Smaller the ripple factor ≃ closer to pure d.c

$$\text{Ripple factor } \gamma = \frac{\text{R.M.S value of a.c component of output}}{\text{Average (or) D.C Component of output}}$$

Now, the output current is composed of a.c component as well as d.c component.

Let I_{ac} = r.m.s value of a.c component present in output.

I_{DC} = D.C component present in output

I_{RMS} = R.M.S value of total output current

$$I_{RMS} = \sqrt{I_{ac}^2 + I_{DC}^2}$$

$$I_{ac} = \sqrt{I_{Rms}^2 - I_{DC}^2}$$

$$\therefore \text{ Ripple factor} = \frac{I_{ac}}{I_{DC}}$$

$$\gamma = \frac{\sqrt{I_{rms}^2 - I_{DC}^2}}{I_{DC}}$$

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$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{DC}}\right)^2 - 1}$$

This is general Expression for ripple factor and can be used for any rectifier circuit.

Similarly, ripple factor interms of voltage is same i.e

$$\gamma = \sqrt{\left(\frac{V_{rms}}{V_{DC}}\right)^2 - 1}$$

Now for a half-wave rectifier circuit,

$$I_{rms} = \frac{I_m}{2}, \quad I_{DC} = \frac{I_m}{\pi}$$

$$\gamma = \sqrt{\frac{\left(\frac{I_m}{2}\right)^2}{\left(\frac{I_m}{\pi}\right)^2} - 1} = \sqrt{\left(\frac{\pi^2}{4}\right) - 1} = \sqrt{1.4674} = 1.21$$

$$\gamma = 1.211$$

This indicates that the ripple contents in output are 1.21 times the d.c component i.e 121.01% of d.c component.

Note :- The Ripple factor is minimised using filter circuit along with the rectifier.

9. Peak inverse Voltage (PIV).

The PIV is the peak voltage across the diode in the reverse direction i.e when the diode is reverse biased. In half-wave rectifier, the load current is ideally zero. when the diode is reverse biased and hence the maximum value of the voltage that can exist across the diode is

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nothing but V_m. This is shown below

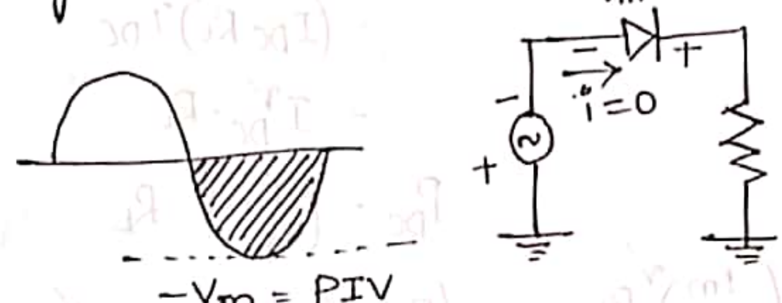

Fig : PIV rating of diode

PIV = Maxium value of secondary voltage = V_m

$$V_m = \pi V_{DC} \text{ (or) } \pi I_{DC}$$

Diode must be selected based on PIV rating and the circuit specifications.

10. Transformer utilization factor (T.U.F)

The factor which indicates how much is the utilization of the transformer in the circuit is called (T.U.F) Transformer utilization factor.

$$T.U.F = \frac{\text{D.c power delivered to the load}}{(\text{a.c power rating of the transformer})_{rated}}$$

Note :- while we are calculating a.c power rating it is necessary to consider r.m.s value of a.c voltage and current.

The A.c power rating of Transformer $= (V_{rms} \cdot I_{RMS})_{rated}$

Wher $(V_{rms})_{rated} = \frac{V_m}{\sqrt{2}}$ $\quad$ $A.C_{power} = \frac{V_m}{\sqrt{2}} \cdot \frac{I_m}{2}$

$(I_{rms})_{rated} = \frac{I_m}{2}$ $\quad$ $P_{AC} = \frac{V_m \cdot I_m}{2\sqrt{2}}$

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D.C power delivered to load $P_{DC} = V_{DC} \cdot I_{DC}$

$$= (I_{DC} R_L) I_{DC}$$

$$= I_{DC}^2 \cdot R_L$$

$$P_{DC} = \left(\frac{I_m}{\pi}\right)^2 \cdot R_L$$

$$\therefore \text{TUF} = \frac{\left(\frac{I_m}{\pi}\right)^2 R_L}{\left(\frac{V_m I_m}{2\sqrt{2}}\right)} = \frac{\left(\frac{I_m}{\pi}\right)^2 R_L}{\left(\frac{I_m^2 R_L}{2\sqrt{2}}\right)} = \frac{I_m^2}{\pi^2} R_L \times \frac{2\sqrt{2}}{I_m^2 R_L}$$

$$= \frac{2\sqrt{2}}{\pi^2} = 0.287$$

$$\text{T.U.F} = 0.287$$

The value of TUF is low which shows that in half-wave circuit the transformer is not fully utilized.

11. Voltage Regulation :—

The Secondary voltage should not change with respect to the load current. The voltage regulation is the factor which tells us about the change in the d.c output voltage as load changes from no load to full load Condition

if $(V_{dc})_{NL}$ = D.C voltage on no load

$(V_{DC})_{FL}$ = D.C voltage on full load

$$\text{Voltage Regulation} = \frac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}}$$

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$$(V_{dc})_{NL} = \frac{V_m}{\pi}$$

$$(V_{dc})_{FL} = I_{DC} \cdot R_L = \frac{I_m}{\pi} \cdot R_L = \frac{V_m}{\pi(R_L + R_s + R_f)} \cdot R_L$$

$$\% R = \frac{\frac{V_m}{\pi} - \frac{V_m}{\pi} \cdot \frac{R_L}{R_L + R_s + R_f}}{\frac{V_m}{\pi} * \frac{R_L}{R_f + R_s + R_L}}$$

$$\% R = \frac{\frac{V_m}{\pi}\left(1 - \frac{R_L}{R_L + R_s + R_f}\right)}{\frac{V_m}{\pi} \times \frac{R_L}{R_L + R_s + R_f}} = \frac{1 - \frac{R_L}{R_L + R_s + R_f}}{\frac{R_L}{R_L + R_s + R_f}}$$

$$\% R = \frac{R_f + R_s}{R_L} \times 100$$

Neglecting winding resistance

$$\% R = \frac{R_f}{R_L} \times 100$$

Less the value of Voltage regulation, better is the performance of rectifier circuit.

Disadvantages of Half-wave rectifier Circuit :—

* The ripple factor of HWR is 1·21 which is quite high.
* Rectification Efficiency is 40% – it indicates the HWR is quite inefficient.
* The circuit has low transformer utilization factor shows that transformer not fully utilized
* DC current is flowing through the secondary winding of the transformer which may cause dc saturation of the core of transformer.

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To minimize this transformer size have to be increased accordingly. This increases the cost.

Because of all these disadvantages, the halfwave rectifier circuit is normally not used as a power rectifier circuit.

FULL WAVE RECTIFIER :—

The Full wave rectifier conducts during both positive and negative half-cycles of input a.c supply. In order to rectify both the half-cycles of a.c input, two diodes are used in this circuit. The diodes feed a common load R_L with the help of a centre tap transformer. The a.c voltage is applied through a suitable power transformer with proper turns ratio.

The full wave rectifier circuit is as shown below. For the proper operation of the circuit, a centre-tap-transformer is essential.

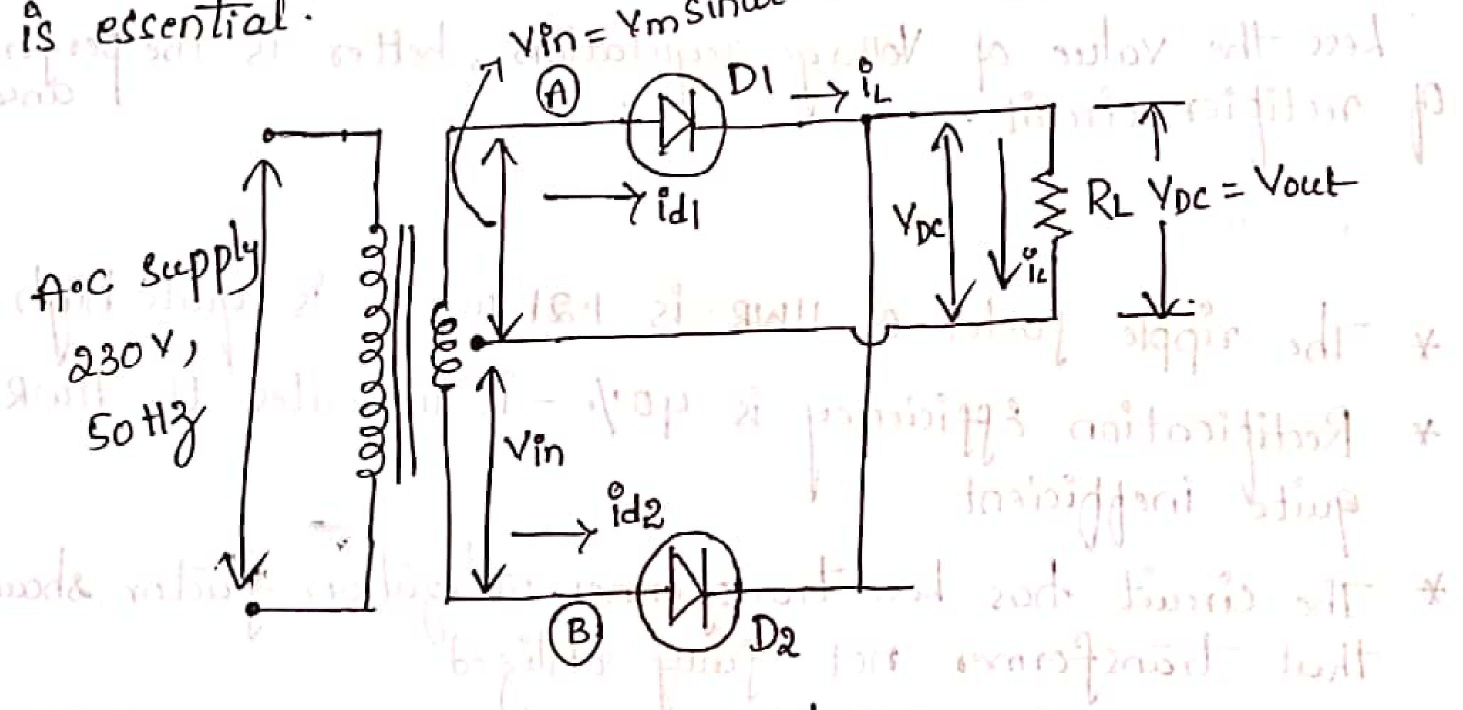
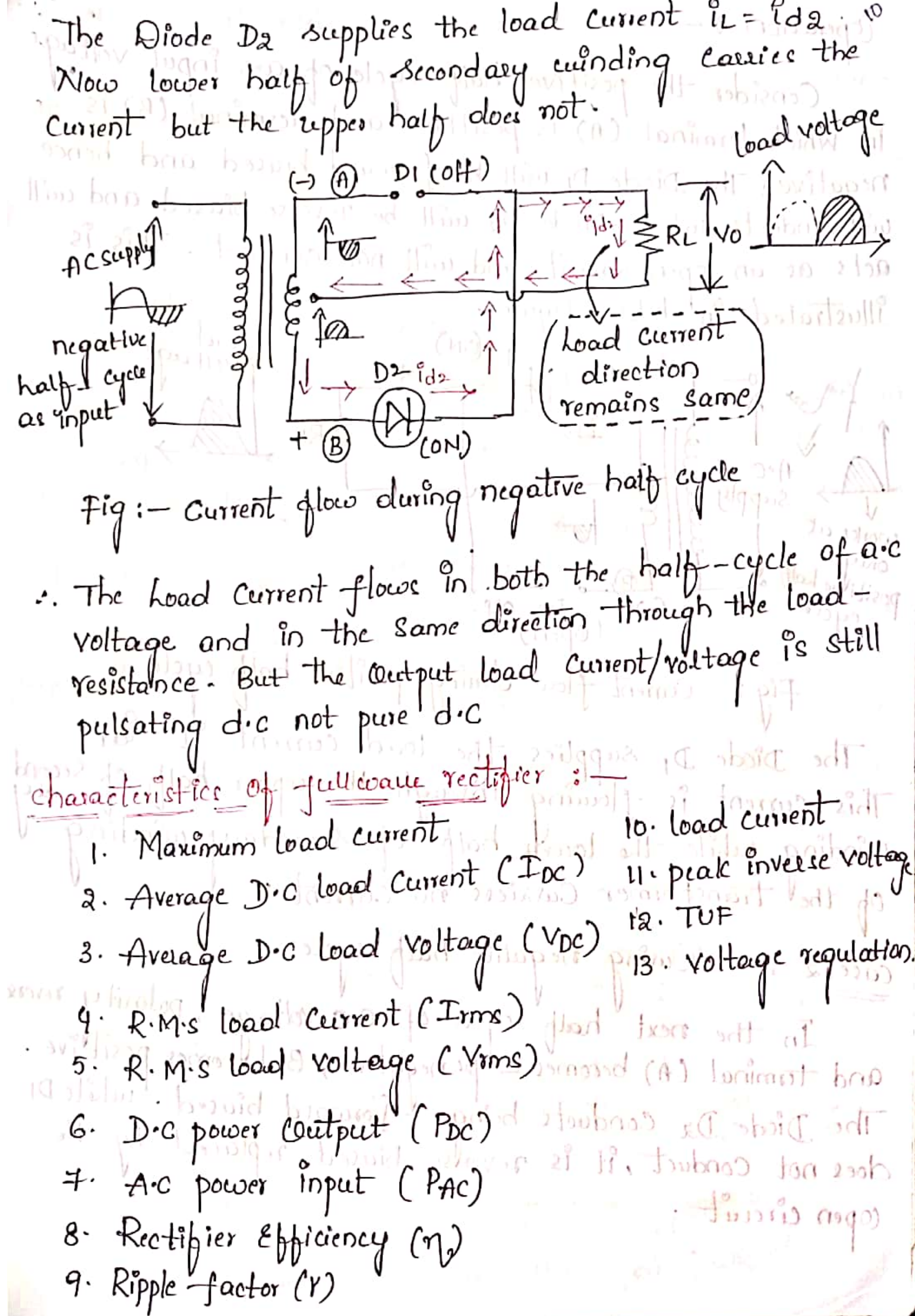


Fig :- Full-wave rectifier



The Diode D_2 supplies the load current $i_L = i_{d2}$. Now lower half of secondary winding carries the current but the upper half does not.

Fig :– Current flow during negative half cycle

∴ The load current flows in both the half-cycle of a.c voltage and in the same direction through the load-resistance. But the output load current/voltage is still pulsating d.c not pure d.c

characteristics of full wave rectifier :–

1. Maximum load current
2. Average D.C load current (I_{DC})
3. Average D.C load voltage (V_{DC})
4. R.M.S load current (I_{rms})
5. R.M.S load voltage (V_{rms})
6. D.C power output (P_{DC})
7. A.C power input (P_{AC})
8. Rectifier Efficiency (η)
9. Ripple factor (r)
10. load current
11. peak inverse voltage
12. TUF
13. Voltage regulation.

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Operation :-

Case 1 :- Consider the positive half-cycle of a.c input voltage in which terminal (A) is positive and terminal (B) is negative. The Diode D_1 will be forward biased and hence will conduct, while Diode D_2 will be reverse biased and will acts as an open circuit and will not conduct. This is illustrated in below figure.

Fig :- Current flow during positive half cycle.

The Diode D_1 supplies the load current $i_L = i_{d1}$. This current is flowing through the upper half of secondary winding while the lower half of secondary winding of the transformer carries no current.

Case 2 :- During negative half cycle

In the next half cycle of a.c voltage, polarity reverse and terminal (A) becomes negative, B becomes positive. The Diode D_2 conducts being forward biased. While D_1 does not conduct, it is reverse biased replaced by the open circuit.

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1. Maximum load Current :-

R_f = forward resistance of diodes

R_s = Winding resistance of each half of secondary

R_L = load resistance

V_{in} = Instantaneous a·c voltage across each half of secondary.

$V_{in} = V_m \sin\omega t$ → interms of voltage (maximum load V_m voltage)

$I_{in} = I_m \sin\omega t$ → (Maximum load current – I_m)

I_m = Maximum value of a·c input voltage across each half of secondary winding $= \frac{V_m}{R_s + R_f + R_L}$

The Output Wave-form of Full wave rectifier circuit.

V_{in} — D2 off, D1 ON | D1-off, D2-ON | D1-ON, D2-off | D1=off, D2-ON | D1-ON

Secondary voltage (one half): V_m, 0, π, 2π, 3π, 4π, ωt

I_m, 0, π, 2π, 3π, 4π, ωt

Secondary voltage (-ve one half): I_m, 0, π, 2π, 3π, 4π, ωt

Load current: I_m, 0, π, 2π, 3π, 4π, ωt, $I_{av} = I_{DC} = \frac{2I_m}{\pi}$

Load voltage: V_m, 0, π, 2π, 3π, 4π, ωt, $V_{avg} = V_{DC} = \frac{2V_m}{\pi}$

Fig:- load Current and load Voltage for FWR.

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2. Average (or) DC Current :-

Consider one cycle of the load current i_L from 0 to π, to obtain the average value which is d.c value of load current

$$i_L = I_m \sin\omega t \quad - 0 \leq \omega t \leq \pi$$

$$I_{avg} \text{ or } I_{DC} = \frac{1}{\pi}\int_0^{\pi} i_L \, d(\omega t) = \frac{1}{\pi}\int_0^{\pi} I_m \sin\omega t \cdot d\omega t$$

$$= \frac{I_m}{\pi}\left[(-\cos\omega t)_0^{\pi}\right]$$

$$= \frac{I_m}{\pi}\left(-\cos\pi - (-\cos 0)\right)$$

$$= \frac{I_m}{\pi}(+1-(-1))$$

$$I_{DC} = \frac{2I_m}{\pi}$$

3. Average (or) D.C load voltage (V_{DC}) :-

$$V_{DC} = I_{DC} \cdot R_L = \frac{2 I_m \cdot R_L}{\pi}$$

$$V_{DC} = \frac{2V_m \cdot R_L}{\pi[R_L + R_s + R_L]} = \frac{2V_m}{\pi\left(1 + \frac{R_f + R_s}{R_L}\right)}$$

$$\frac{R_f + R_s}{R_L} << 1$$ (R_s, R_f are neglected)

$$V_{DC} = \frac{2V_m}{\pi}$$

4. R.M.S load Current (I_{rms}) :-

The r.m.s value of current

$$I_{Rms} = \sqrt{\frac{1}{2\pi}\int_0^{2\pi} i_L^2 \, d(\omega t)}$$

$$I_{R.M.S} = \sqrt{\frac{1}{2\pi}\int_0^{\pi} (I_m \sin \omega t)^2 d(\omega t)}$$

$$= I_m \sqrt{\frac{1}{\pi}\int_0^{\pi}\left(\frac{1-\cos 2\omega t}{2}\right) d\omega t}$$

$$= I_m \sqrt{\frac{1}{2\pi}\left[(\omega t)_0^{\pi} - \left(\frac{\sin 2\omega t}{2}\right)_0^{\pi}\right]}$$ (as $\sin 2\pi = \sin(0) = 0$)

$$= I_m \sqrt{\frac{1}{2\pi}(\pi - 0)}$$

$$= I_m \sqrt{\frac{1}{2\pi}\pi} = \frac{I_m}{\sqrt{2}}$$

$$\boxed{I_{R.M.S} = \frac{I_m}{\sqrt{2}}}$$

5. R.M.S Value of load voltage :-

$$V_{R.M.S} = I_{R.M.S} \times R_L$$

$$= \frac{I_m}{\sqrt{2}} \times R_L$$

$$V_{R.M.S} = \frac{V_m}{\sqrt{2} \cdot R_L} \times R_L = \frac{I_m}{\sqrt{2}}$$

$$\boxed{V_{R.M.S} = \frac{V_m}{\sqrt{2}}}$$

6. D.C power output :- (P_{DC})

D.C power output $= V_{DC} \cdot I_{DC} = I_{DC}^2 \cdot R_L$

$$P_{DC} = I_{DC}^2 \cdot R_L = \left(\frac{2I_m}{\pi}\right)^2 R_L$$

$$P_{DC} = \frac{4}{\pi^2} I_m^2 R_L$$

Sub Value of I_m we get.

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$$P_{DC} = \frac{4}{\pi^2} \frac{V_m^2}{(R_s + R_f + R_L)^2} \times R_L$$

7). A.C power input ($P_{A.C}$) :-

$$P_{A.C} = I_{rms}^2 (R_s + R_f + R_L) = \left(\frac{I_m}{\sqrt{2}}\right)^2 (R_f + R_s + R_L)$$

$$P_{A.C} = \frac{I_m^2 (R_f + R_s + R_L)}{2}$$

Sub value of I_m we get,

$$P_{AC} = \frac{V_m^2}{(R_f + R_s + R_L)^2} \times \frac{1}{2} \times (R_f + R_s + R_L)$$

$$P_{AC} = \frac{V_m^2}{2(R_f + R_s + R_L)}$$

8. Rectifier Efficiency :-

$$\eta = \frac{P_{DC} \text{ output}}{P_{AC} \text{ input}} = \frac{4/\pi^2 \cdot I_m^2 R_L}{\frac{I_m^2 (R_f + R_s + R_L)}{2}} = \frac{8 R_L}{\pi^2 (R_f + R_s + R_L)}$$

$$\eta = \frac{8 R_L}{\pi^2 (R_L)} = \frac{8}{\pi^2} = 0.812$$

$$\% \eta = 0.812 \times 100 = 81.2\%$$

$$\% \eta = 81.2\%$$

Maximum theoretical Efficiency of FWR = 0.812
= 81.2%

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9). Ripple factor :-

$$\gamma = \sqrt{\left(\frac{I_{rms}}{I_{dc}}\right)^2 - 1} \quad \left(\because I_{rms} = \frac{I_m}{\sqrt{2}},\ I_{DC} = \frac{2I_m}{\pi}\right)$$

$$= \sqrt{\left(\frac{I_m/\sqrt{2}}{2I_m/\pi}\right)^2 - 1} = \sqrt{\frac{\pi^2}{8} - 1} = 0.48$$

$$\gamma = 48\%$$

10). Load Current (i_L) :-

The Fourier Series for the load current is obtained by taking the sum of the series for the individual rectifier current. The two diodes conduct in alternate half cycles i.e. there is phase difference of π radians between two diodes current. Hence,

$$i_{d1} = I_m\left[\frac{1}{\pi} + \frac{1}{2}\sin\omega t - \frac{2}{3\pi}\cos 2\omega t - \frac{2}{15\pi}\cos 4\omega t \cdots\right]$$

i_{d2} = i_{d1} with ωt replaced by $(\omega t + \pi)$

$$i_{d2} = I_m\left[\frac{1}{\pi} + \frac{1}{2}\sin(\omega t + \pi) - \frac{2}{3\pi}\cos 2(\omega t + \pi) - \frac{2}{15\pi}\cos 4(\omega t + \pi) \cdots\right]$$

$$= I_m\left(\frac{1}{\pi} - \frac{1}{2}\sin\omega t - \frac{2}{3\pi}\cos(2\omega t + 2\pi) - \frac{2}{15\pi}\cos(4\omega t + 4\pi) + \cdots\right)$$

$$= I_m\left(\frac{1}{\pi} - \frac{1}{2}\sin\omega t - \frac{2}{3\pi}\cos 2\omega t - \frac{2}{15\pi}\cos 4\omega t \cdots\right]$$

Then the fourier series for the load current is,

$$i_L = i_{d1} + i_{d2}$$

$$i_L = I_m\left[\frac{2}{\pi} - \frac{4}{3\pi}\cos 2\omega t - \frac{4}{15\pi}\cos 4\omega t \cdots\right]$$

$\frac{2}{\pi}$ → d.c component; remaining terms → a.c (or) ripples.

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$$i_{secondary} = i_{d1} - i_{d2}$$

$$\therefore \; i_{secondary} = I_m \sin\omega t$$

11. Peak inverse voltage :-

the Maximum reverse voltage the diode can be withstand without damaging the junction of diode.

$$\text{PIV of diode} = 2V_m = \pi V_{DC} \text{ (or) } \pi I_{DC}$$

D1 forward biased

A.C supply

V_m

R_L V_o

A B

D2 (reverse biased)

voltage across D1

voltage across D2

ωt

$2V_m$

$$\boxed{PIV = 2V_m}$$

if diode drop is considered to be 0.7V then

$$\boxed{PIV = 2V_m - 0.7}$$

12. Transformer utilization factor :- (T.U.F)

$$T.U.F = \frac{\text{D.C power to the load}}{\text{A.C power rating of secondary}}$$

$$= \frac{I_{DC}^2 \cdot R_L}{V_{rms} \cdot I_{rms}} = \frac{\left(\frac{2I_m}{\pi}\right)^2 R_L}{\frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}}$$

neglecting forward & secondary resistance R_f & R_s.

$$V_m = I_m R_L$$

$$(TUF)_{sec} = \frac{4/\pi^2 \times I_m^2 R_L}{\frac{I_m^2 R_L}{2}} = \frac{8}{\pi^2} = 0.812$$

∴ The primary of the transformer is feeding two half wave rectifiers separately. These two half-wave rectifiers work independently of each other but feed a common load. i.e

T.U.F for primary winding = 2 X T.U.F for secondary

$$= \frac{0.574 + 0.812}{2}$$

$$= 0.693$$

Average T.U.F for full-wave rectifier = 0.693

$$T.U.F = 0.693$$

13. Voltage Regulation :-

$$(V_{dc})_{NL} = \frac{2V_m}{\pi}, \quad (V_{dc})_{FL} = I_{DC} \cdot R_L$$

$$\%R = \frac{(V_{dc})_{NL} - (V_{dc})_{FL}}{(V_{dc})_{FL}} \times 100$$

$$= \frac{\frac{2V_m}{\pi} - I_{DC} R_L}{I_{DC} R_L} \times 100$$

$$\%R = \frac{2V_m/\pi - I_{DC} R_L}{I_{DC} R_L} \times 100$$

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$$I_m = \frac{V_m}{R_f + R_s + R_L}$$

$$V_m = I_m(R_f + R_s + R_L)$$

$$I_{DC} = \frac{2I_m}{\pi}$$

$$\% R = \frac{\frac{2I_m}{\pi}(R_f + R_s + R_L) - \frac{2I_m}{\pi} R_L}{\frac{2I_m}{\pi} \times R_L} \times 100$$

$$= \frac{R_f + R_s + R_L - R_L}{R_L} \times 100$$

$$\% R = \frac{R_f + R_s}{R_L} \times 100$$

Neglecting winding resistance R_s, the regulation can be expressed as,

$$\% R = \frac{R_f}{R_L} \times 100$$

Where R_f = Forward resistance of the diode.

Advantages of Full wave rectifier :—

* The D.C load voltage and current are more than half-wave.
* No D.C current through transformer windings hence no possibility of saturation.
* TUF is better as transformer losses are less.
* Efficiency is higher
* large d.c power output
* The ripple factor is less.

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Disadvantages of full wave rectifier :-

* The PIV rating of diode is higher
* Higher PIV diodes are larger in size and costlier.
* The cost of centre tap transformer is higher.

BRIDGE RECTIFIER :-

The Bridge rectifier Circuit are mainly used as,

a). The power rectifier circuit for Converting a.c power to d.c power.

b). A rectifying system in rectifier type a.c meters, such as a.c voltmeter, in which the a.c voltage under measurement in first converted into d.c and measured with conventional meter. In this system, the rectifying elements are either Copper oxide type or Selenium type.

The Basic Bridge rectifier circuit is shown below

Fig:- Bridge rectifier Circuit.

The bridge rectifier circuit is essentially a full-wave rectifier circuit, using 4 diodes forming the 4 arms of an electrical bridge. To one diagonal of the bridge the a.c voltage is applied through a transformer if necessary, and the rectified d.c voltage is taken from the other diagonal of the bridge.

The main advantage of the circuit is that it does not require a centre tap transformer on the secondary winding. Hence wherever possible a.c voltage can be directly applied to the bridge.

Operation :—

Consider the positive half cycle of ac input voltage. The point A of secondary becomes positive. The diodes D_1 and D_2 will be forward biased, while D_3 and D_4 reverse biased. The two diodes D_1, D_2 conduct in series with the load and the current flows as shown in fig below.

Fig: Current flow during positive half-cycle.

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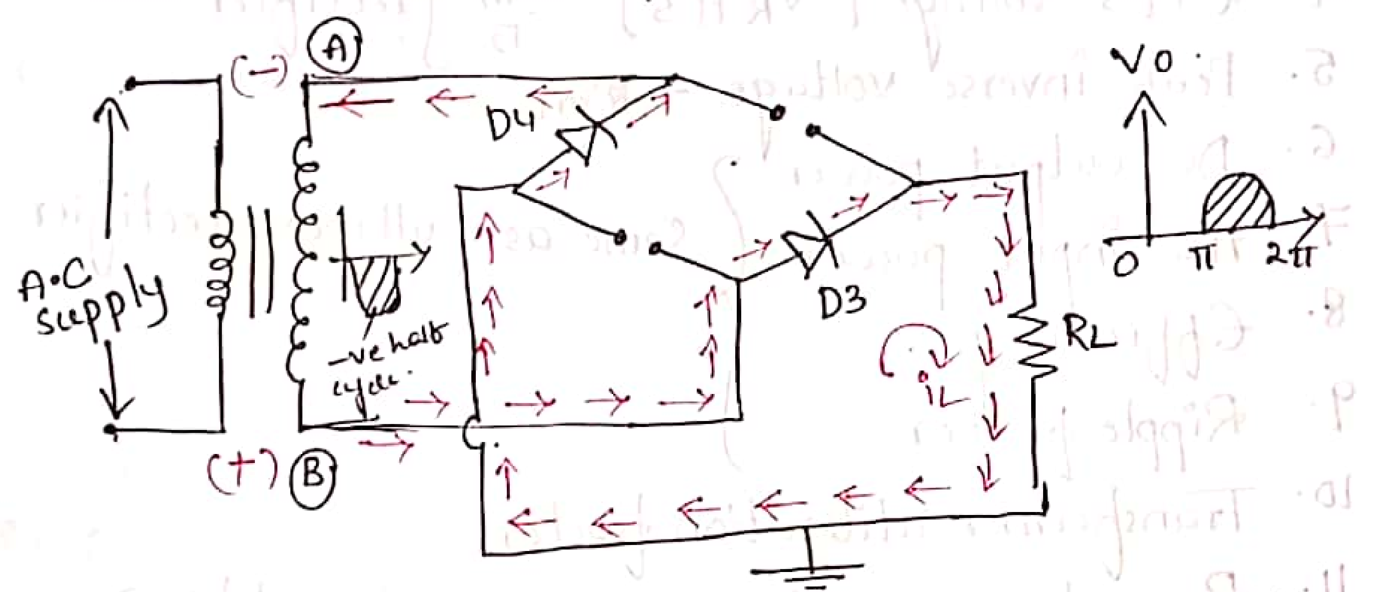
In the next half-cycle, when the polarity of a.c Voltage reverses hence point B becomes positive diodes D3 and D4 are forward biased, while D1 and D2 reverse biased. Now the diodes D3 and D4 conduct is series with the load and the current flows as shown in below



It is seen that in both cycles of a.c the load current is flowing in the same direction hence, we get a full-wave rectified output.

The output waveforms of Bridge rectifier :—

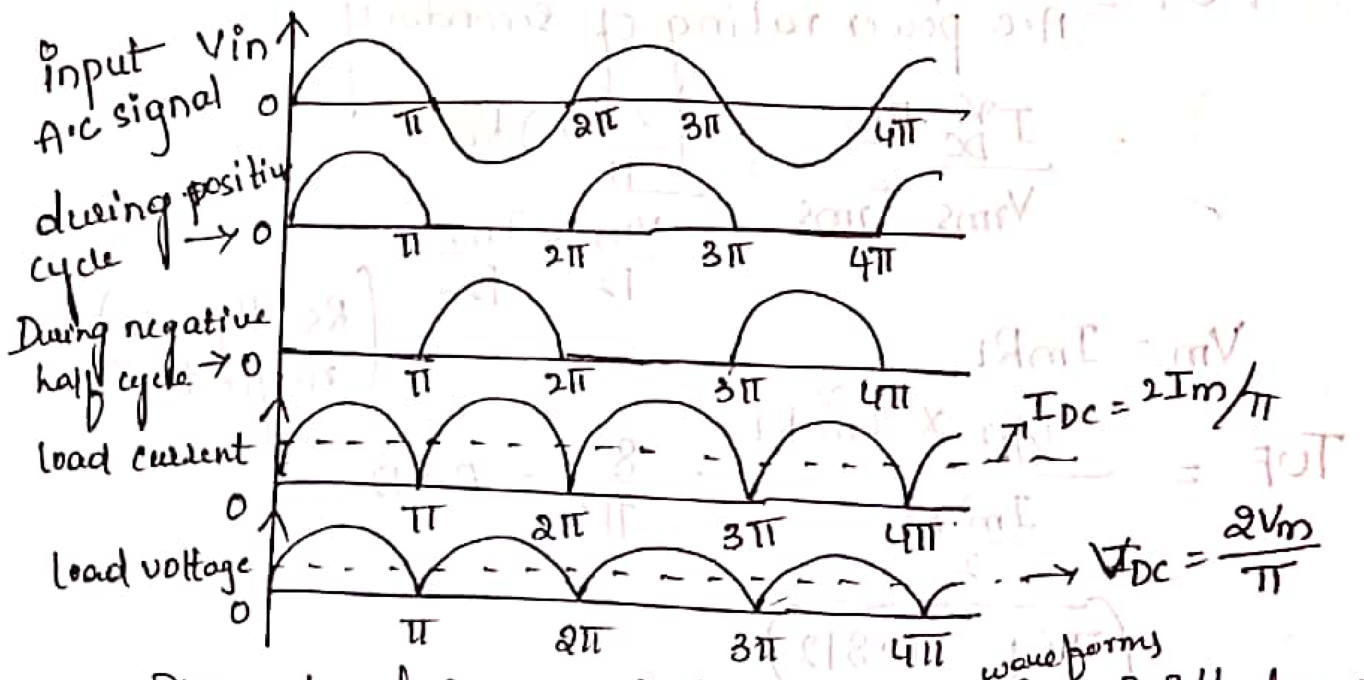


Fig:- Load Current & load voltage waveforms for Bridge rectifier.

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Characteristics of Bridge rectifier :-

1. Average (or) DC current – $\frac{2I_m}{\pi}$ } Same as Full-wave rectifier
2. Average (or) DC voltage – $\frac{2V_m}{\pi}$ }
3. R.M.S current ($I_{R.M.S}$) – $\frac{V_m}{\sqrt{2}}$ } Same as full wave rectifier
4. R.M.S Voltage ($V_{R.M.S}$) – $\frac{V_m}{\sqrt{2}}$ }
5. Peak inverse voltage – $2V_m$
6. DC output power } Same as Full wave rectifier.
7. AC input power }
8. Efficiency }
9. Ripple factor }
10. Transformer utilization factor
11. Regulation ⟶ (Same as full wave rectifier).
12. Forward resistance.

(10). Transformer utilization factor :-

$$T.U.F = \frac{D.C \text{ power to the load}}{A.C \text{ power rating of secondary}}$$

$$= \frac{I_{DC}^2 \cdot R_L}{V_{rms} \cdot I_{rms}} = \frac{\left(\frac{2I_m}{\pi}\right)^2 R_L}{\frac{V_m}{\sqrt{2}} \times \frac{I_m}{\sqrt{2}}}$$

$$V_m = I_m R_L$$

($R_s = R_f = 0$ neglect).

$$TUF = \frac{4/\pi^2 \times I_m^2 R_L}{\frac{I_m^2 R_L}{2}} = \frac{8}{\pi^2} = 0.812$$

$$TUF = 0.812$$

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* DC current $I_{DC} = \frac{2I_m}{\pi}$
* DC voltage $V_{DC} = \frac{2V_m}{\pi}$
* R.M.S current $I_{R.M.S} = \frac{I_m}{\sqrt{2}}$
* R.M.S voltage $V_{R.M.S} = \frac{V_m}{\sqrt{2}}$
* Forward resistance is $R_f + R_f = 2R_f$
  (because at a time two diodes are conduct. so two forward resistance occur).
* $I_m = \frac{V_m}{R_s + 2R_f + R_L}$
* $P_{DC} = I_{DC}^2 R_L = \frac{4}{\pi^2} I_m^2 \cdot R_L$
* $P_{AC} = I_{RMS}^2 (R_s + 2R_f + R_L)$
  $= \frac{I_m^2 (2R_f + R_s + R_L)}{2}$
* Efficiency $\eta = \frac{8R_L}{\pi^2 (R_s + 2R_f + R_L)}$

  $\% \eta = 81.2\%$
* Ripple factor $\gamma = 0.48$.
* peak inverse voltage is V_m.

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Advantages of Bridge rectifier :-

* No centre tap transformer is required. Hence, whenever possible a.c voltage can directly be applied to the bridge.
* As two diodes conduct in series in each half-cycle, inverse voltage appearing across diodes get shared. Hence the circuit can be used for high voltage applications. Such a peak reverse voltage appearing across diode is called peak inverse voltage rating (PIV) of diode.

Disadvantages :-

The only disadvantage of Bridge rectifier is the use of four diodes as compared to two diodes in normal full wave rectifier. This causes additional voltage drop as indicated by term $2R_f$ present in expression of I_m instead of R_f. This reduces the output voltage.

Applications :-

* Used as rectifier in power circuits to convert a.c to d.c
* In rectifier type meters, to convert a.c voltage to be measured to d.c
* In power supply circuits.

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Comparison of FWR with Bridge rectifier :—

Full-wave rectifier (FWR using two Diodes)	Bridge rectifier (FWR using 4 (four) diodes
1. It uses centre tapped transformer.	1. It does not use centre tapped transformer.
2. One Diode conducts in each half cycle of input	2. Two diodes conduct in each half cycle of input
3. The voltage drop across the diode is due to R_f only	3. The voltage drop across the ~~load~~ diodes is due to $2R_f$
4. The output voltage is more	4. The output voltage is less
5. The transformer is less effectively used	5. The Transformer is used more Effectively.
6. T.U.F is 0.693	6. T.U.F is 0.812
7. PIV rating of the Diode is $2V_m$	7. The PIV rating of the diode is V_m.

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Comparison of Rectifier Circuits

S.No	parameter	Half-wave rectifier	Full-wave rectifier	Bridge rectifier
1.	Number of Diodes	1	2	4
2.	Average D.C current (I_{DC})	$\frac{I_m}{\pi}$	$\frac{2I_m}{\pi}$	$\frac{2I_m}{\pi}$
3.	Average D.C voltage (V_{DC})	$\frac{V_m}{\pi}$	$\frac{2V_m}{\pi}$	$\frac{2V_m}{\pi}$
4.	R.M.S current	$\frac{I_m}{2}$	$\frac{I_m}{2}$	$\frac{I_m}{2}$
5.	R.M.S voltage	$\frac{V_m}{2}$	$\frac{V_m}{2}$	$\frac{V_m}{2}$
6.	Dc output power (P_{DC})	$\frac{I_m^2 R_L}{\pi^2}$	$\frac{4}{\pi^2} I_m^2 R_L$	$\frac{4}{\pi^2} I_m^2 R_L$
7.	A.C input power (P_{AC})	$\frac{I_m^2 (R_L+R_f+R_s)}{4}$	$\frac{I_m^2 (R_f+R_s+R_L)}{2}$	$\frac{I_m^2 (2R_f+R_s+R_L)}{2}$
8.	Maximum rectifier efficiency (η)	40.6%	81.2%	81.2%
9.	Ripple factor (γ)	1.21	0.482	0.482
10.	Maximum load current (I_m)	$\frac{V_m}{R_s+R_f+R_L}$	$\frac{V_m}{R_s+R_f+R_L}$	$\frac{V_m}{R_s+2R_f+R_L}$
11.	PIV	V_m	$2V_m$	V_m
12.	Ripple frequency	50Hz	100Hz	100Hz.
13.	T.U.F	0.287	0.693	0.812

2(B) · FILTERS

Filter :— Filters are used to minimise the undesirable ac i.e ripples (unwanted particles). It is an electronic-circuit composed of capacitor-inductor or combination of both and connected between the rectifier and load to convert pulsating d.c to pure d.c

Vin → Filter → Vout (ripple)

Need of Filters :—

It is seen that the output of a half-wave or full wave rectifier circuits is not pure d.c but it contains ripples or undesired components. To minimize the ripple content in the output, filter circuits are used. These circuits are connected between the rectifier and load.

Block diagram of filter :—

Block diagram for filter is as shown below :—

A.C input → Rectifier circuit → D.C (ripple) → Filter → Pure D.C → R_L

pulsating D.C

filtered D.C

Fig :- power supply using Rectifier and filter.

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An a.c input is applied to the rectifier. At the output of the rectifier, there will be d.c and ripple voltage present, which is the input to the filter. Ideally the output of the filter should be pure d.c. practically, the filter circuit will try to minimize the ripple at the output as far as possible.

Basically the ripple is a.c (i.e., Varying with time) while D.C (i.e not varying with time) is Constant. Hence in order to separate d.c from ripple, the filter circuit should use components which have widely different impedance for a.c and D.C. Two such components are

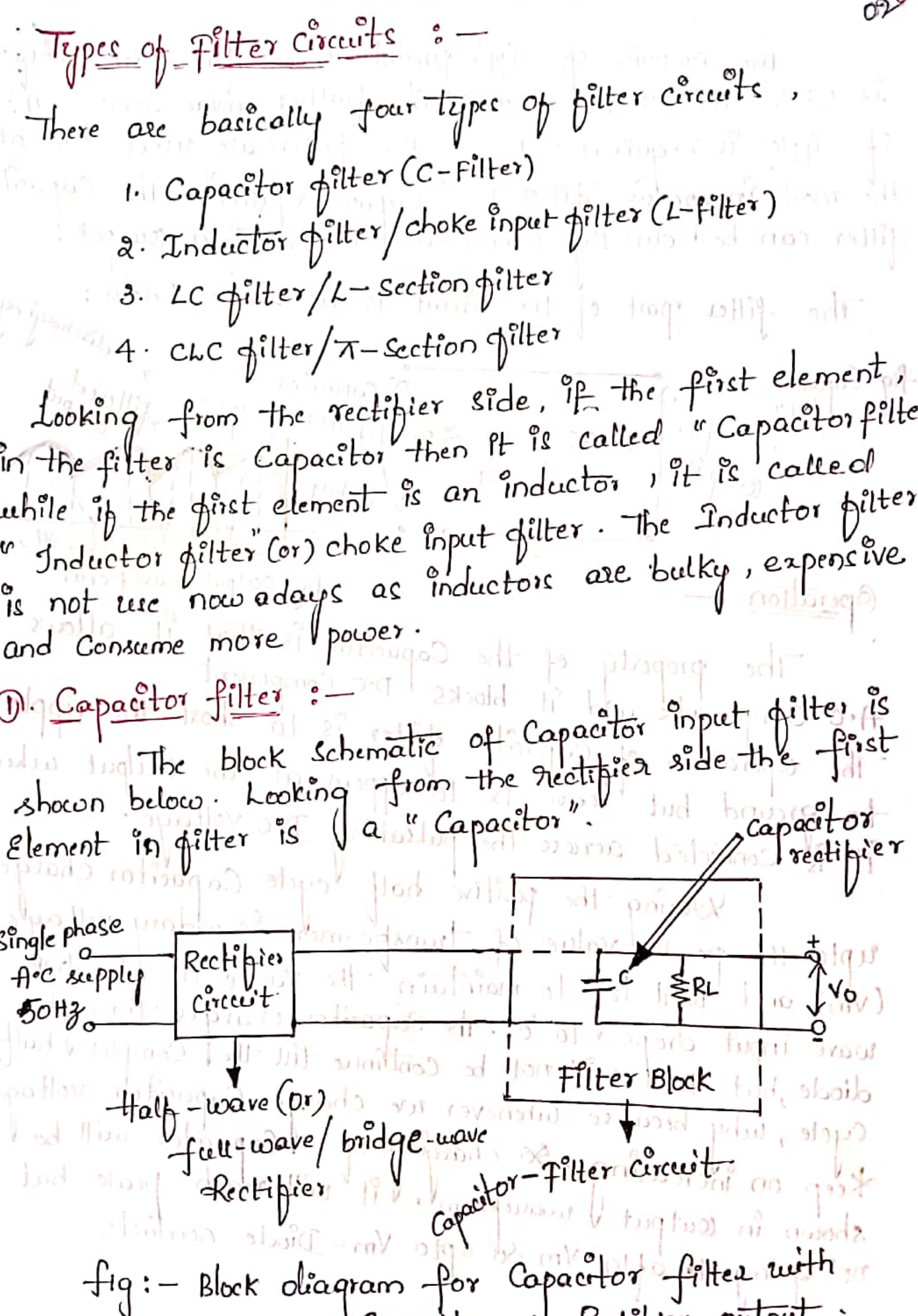
* Capacitors
* Inductors

* Ideally, Inductors acts as short circuit for d.c but it has large impedance for a.c
* Capacitors acts as short circuit for a.c but it has large impedance for d.c.

* Inductors acts as short circuit for d.c so it cannot be placed in shunt arm across the load, otherwise d.c will be shorted. (i.e Inductors are always connected in series with the load).
  (shunt arm → parallel)

* Inductance used in filter circuits is also called "choke".

* Similarly, the capacitance is open for d.c i.e it blocks d.c; hence it cannot be connected in series with the load.



Types of Filter Circuits :-

There are basically four types of filter circuits,

1. Capacitor filter (C-Filter)
2. Inductor filter/choke input filter (L-filter)
3. LC filter/L-Section filter
4. CLC filter/π-Section filter

Looking from the rectifier side, if the first element in the filter is Capacitor then it is called "Capacitor filter" while if the first element is an inductor, it is called "Inductor filter" (or) choke input filter. The Inductor filter is not use now adays as inductors are bulky, expensive and Consume more power.

①. Capacitor filter :-

The block schematic of Capacitor input filter is shown below. Looking from the rectifier side the first Element in filter is a "Capacitor".

fig :- Block diagram for Capacitor filter with Connection of Rectifier output.

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The amount of ripple present in a full wave rectifier is 48%. This is not sufficient, further more reduction of ripple is required. To do this filters are used. One of the most "inexpensive" filter is "Capacitor filter". The capacitor filter can be directly connected to rectifier output.

The filter part of the circuit is as shown below:

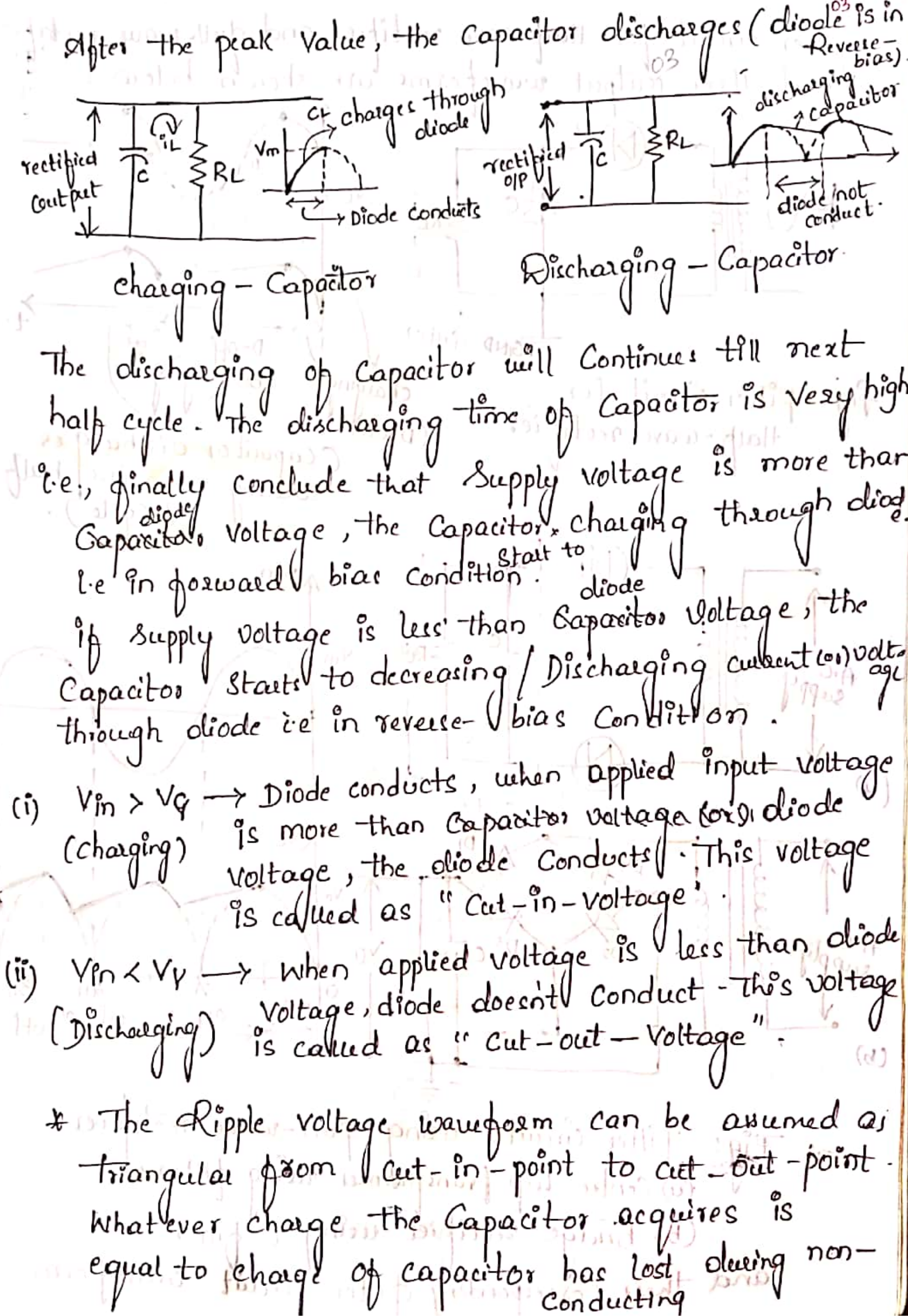
fig: Capacitor filter

fig: output waveform.

Operation :-

The property of the capacitor is that it allows A.C component and it blocks D.C component. The operation of capacitor filter is to short the ripple to ground but leave DC to appear at the output when it is connected across the pulsating D.C voltage.

During the positive half cycle capacitor charges upto the peak value of transformer secondary voltage (vm) and will try to maintain the value as the full wave input drops to '0'. The capacitor charges through diode, but that will not be continue till the complete half cycle, why because whenever we charge capacitor voltage keep on increasing, so charging of capacitor will be shown in output waveform. It will reach peak but not going to after Vm so upto Vm - Diode conducts.



After the peak value, the Capacitor discharges (diode is in Reverse-bias).

rectified output | C | i_L | R_L | V_m | C_L charges through diode | Diode conducts

charging - Capacitor

rectified O/P | C | R_L | discharging capacitor | diode not conduct.

Discharging - Capacitor

The discharging of capacitor will Continues till next half cycle. The discharging time of Capacitor is very high i.e., finally conclude that Supply voltage is more than Capacitor diode voltage, the Capacitor start to charging through diode. i.e in forward bias condition.

if supply voltage is less than Capacitor diode Voltage, the Capacitor Starts to decreasing / Discharging current (or) voltage through diode i.e in reverse- bias Condition.

(i) $V_{in} > V_C$ → Diode conducts, when applied input voltage (Charging) is more than Capacitor voltage (or) diode voltage, the diode Conducts. This voltage is called as "Cut-in-voltage".

(ii) $V_{in} < V_\gamma$ → when applied voltage is less than diode (Discharging) Voltage, diode doesn't Conduct. This voltage is called as "Cut-out-Voltage".

* The Ripple voltage waveform can be assumed as triangular from cut-in-point to cut-out-point. Whatever charge the Capacitor acquires is equal to charge of capacitor has lost during non-Conducting

Filter circuit for Half wave rectifier and full-wave rectifier and their output waveforms are shown below :

D, C, RL, GND, Filter

V_m, 0, π, 2π, V_C, t

charging (D-ON), D-off (Discharging), ON

fig: Filter circuit for Half-wave rectifier

(Capacitor discharges during negative half cycle).

A.C supply, C, RL, Filter

V_{in}, V_m

(a)

A.C supply, D4, D1, D2, D3, C, RL, Vo

V_C, V_m, 0, π, 2π, 3π, ON, off, ON, off, ON, off

(b)

Fig: Filter circuits using full-wave rectifier
(a) Centre-tap transformer using filter-C
(b) Bridge rectifier using C-filter
and their corresponding filter circuit waveform.

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Ripple factor :-

In Capacitor filter circuit, whatever the charge acquires by capacitor is equal to the charge of the Capacitor has lost during the period of non-conducting.

i.e The charge aquires $= V_{rp-p} \times C$

The charge Loss $= I_{dc} \times T_2$

$\therefore$ Acquired charge = charge lost

$$V_{rp-p} \times C = I_{dc} \times T_2$$

The value of capacitor is large and load resistance is also large. Then we have to assume that

T_2 = Half of the periodic time of waveform $(T_2 = \frac{T_1}{2})$

$$T_2 = \frac{T_1}{2} = \frac{1}{2f}$$

then the value of ripple voltage peak-to-peak is

$$V_{r,p-p} = \frac{I_{dc}}{2fC}$$

With the assumption made above, the ripple form will be triangular in nature and the value of r.m.s of the ripple is given by $V_{r,rms}$,

$$V_{r,rms} = \frac{V_{r,p-p}}{2\sqrt{3}}$$

$$V_{r,rms} = \frac{I_{dC}}{2\sqrt{3} \times 2f_C} = \frac{I_{dc}}{4\sqrt{3}\, fc} = \frac{V_{dc}}{4\sqrt{3}\, fc R_L}$$

for Full-wave rectifier with filter :—

$$V_r = \frac{V_{dC}}{2fCR_L}$$

$$V_{r(rms)} = \frac{V_r}{2\sqrt{3}}$$

$\therefore$ Ripple factor $\Gamma = \dfrac{V_{r,rms}}{V_{dC}}$

$$= \frac{V_{dC}}{V_{dC}\, 4\sqrt{3} fCR_L}$$

The ripple may be decreased by increasing C or R_L (or) both with a resulting increase in dc o/p voltage.

if f = 50 Hz, C = in μF, R_L = in Ω, $\Gamma = \frac{2890}{CR_L}$ //.

for fullwave → $\boxed{\Gamma = \dfrac{1}{4\sqrt{3} fCR_L}}$

Where f_c = supply frequency (Hz)
R_L = load-resistance (Ω)
C = Capacitor (F). filter in F.

for Half-wave rectifier with filter :—

$$V_r = \frac{V_{dc}}{fCR_L}, \quad V_{r(rms)} = \frac{V_r}{2\sqrt{3}}$$

$$\text{Ripple factor} = \frac{V_{r(rms)}}{V_{dC}} = \frac{V_{dc}}{2\sqrt{3} fCR_L \cdot V_{dc}} = \frac{1}{2\sqrt{3} fCR_L}.$$

($V_{r(rms)}$)

i.e $V_{r(rms)} = \dfrac{V_r}{2\sqrt{3}} = \dfrac{V_{dC}}{2\sqrt{3} fCR_L}$

$$\therefore \frac{V_{r(rms)}}{V_{dc}} = \frac{V_{dc}}{2\sqrt{3}\times fc \times R_L \times V_{dc}} = \frac{1}{2\sqrt{3} fcR_L}.$$

$\boxed{\Gamma = \dfrac{1}{2\sqrt{3} fCR_L}}$ → for Half wave.

Where f = Supply frequency (Hz)
C = Capacitor filter in F
R_L = load resistance in Ω

** imp

formulae :—

* DC output voltage $V_{DC} = V_m - I_{DC}\left[\frac{1}{4fC}\right]$ → for fullwave rectifier with C-filter.
* DC output voltage $V_{DC} = V_m - I_{DC}\left(\frac{1}{2fC}\right)$ → for Half-wave with C-filter
* $V_{r(rms)}$ (rms voltage) $= \dfrac{I_{DC}}{4\sqrt{3} fC}$ Volts. → full wave C-filter
* $V_{r(rms)}$ (rms voltage) $= \dfrac{I_{DC}}{2\sqrt{3} fC}$ volts → Half wave C filter

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Advantages :- The advantages of C-filter are

1. Less number of components
2. Low ripple factor hence low ripple voltage
3. Suitable for high voltage at small load current

Disadvantages :- The Disadvantages of C-filter are

1. Ripple factor depends on load resistance.
2. Not suitable for variable loads as ripple content increases as R_L decreases.
3. Regulation is poor.
4. Diodes are subjected to high surge currents hence must be selected accordingly.

Problems:

1). Calculate the value of capacitance to use in capacitor filter connected to a full wave rectifier operating at a standard aircraft power frequency of 400 Hz. If the ripple factor is 10% of a load of 500Ω

$$\Gamma = \frac{1}{4\sqrt{3} f C R_L}$$

$$\Gamma = 10\% = 10 \times \frac{1}{100} = 0.1$$

$f = 400$, $R_L = 500\,\Omega$

$$\Gamma = \frac{1}{4\sqrt{3} f C R_L} \Rightarrow C = \frac{1}{4\sqrt{3} f \Gamma R_L}$$

$$= \frac{1}{4\sqrt{3} \times 400 \times 0.1 \times 500}$$

$$= \frac{1}{138560} = 7.21\,\mu f$$

$$\boxed{\Gamma = 7.21\,\mu f}$$

2. Calculate the value of Capacitance to use in a Capacitor filter connected to a full-wave rectifier operating at a standard aircraft power frequency of 400 Hz, if the ripple factor is 10% for a load of 500 Ω.

(3)

2. A FWR voltage of 18V peak is applied across a 500 μF filter capacitor. Calculate the ripple and dc voltages if the load takes a current of 100 mA.

Given $V_m = 18V$

$C = 500 \mu F$

$I_{dc} = 100 mA$

$$V_{dc} = V_m - \frac{I_{dc}}{4fC} = 18 - \frac{100 \times 10^{-3}}{4 \times 50 \times 500 \times 10^{-6}} = 17V$$

$$V_{r,rms} = \frac{I_{dc}}{4\sqrt{3} fC} = \frac{100 \times 10^{-3}}{4\sqrt{3} \times 50 \times 500 \times 10^{-6}} = 0.577 V$$

∴ ripple factor $\Gamma = \frac{V_{rms}}{V_{dc}} = \frac{0.577}{17} \times 100 = 3.39\%$

3. A Bridge rectifier with capacitor filter is fed from 220V-to 40V step down transformer. If average d.c current in load is 1A and capacitor filter of 800 μF. Calculate the load regulation and ripple factor. Assume power line frequency of 50 Hz. Neglect diode forward resistance and d.c resistance of secondary of transformer?

$V_{rms} = 40V$ $C = 800 \mu F$, $f = 50 Hz$

$I_{dc} = 1A$

∴ $V_m = \sqrt{2} V_{rms} = \sqrt{2} \times 40 = 56.56 V$

$$V_{dc(FL)} = V_m - \frac{I_{dc}}{4fC} = 56.5685 - \frac{1}{4 \times 50 \times 800 \times 10^{-6}} = 50.31V$$

On no load $I_{dc} = 0$

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CLIPPERS:-

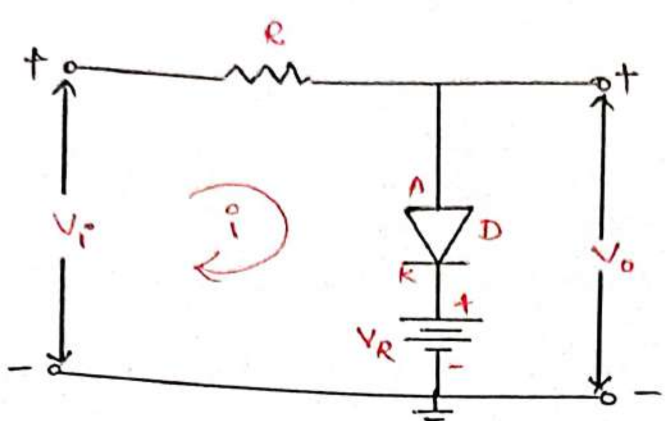
* A clipping circuit is a circuit which removes the undesired part of the waveform and transmits only the desired part of the signal which is above or below some particular reference level.
* That is, it is used to select for transmission that part of an arbitary waveform which lies above or below some particular reference.
* Clipping circuits are also called voltage (or current) limiters, amplitude selectors or slicers.
* The different types of clippers are 1. Shunt clippers
  2. series clippers

1. SHUNT CLIPPERS:-

* In shunt clippers diode is connected in shunt across the output.

1. Clipping above Reference Voltage:

* The Diode D is connected in series with battery V_R and this series combination forms a parallel path across the output V_o. V_R represents the reference voltage. R is a current limiting resistance.
* Let V_o denotes the output voltage when an input voltage V_i is transmitted through the circuit.



* For $V_i < V_R + V_r$, the diode D is OFF since it is reverse-biased and hence doesnot conduct. Since no current flows there is no voltage drop across R.

$$\therefore V_o = V_i \quad \text{for } V_i < V_R + V_r$$

* It is evident that when $V_o = V_i$ i.e., when D is OFF, there is no clipping action and the input signal is transmitted without any alteration of wave shape.

For $V_i > V_R + V_r$:

* For $V_i > V_R + V_r$, the diode D is ON, since it is forward biased and the potential barrier is overcomed.

we have $i = \dfrac{V_i - (V_R + V_r)}{R + R_f}$

output voltage $V_o = V_i - iR$

$$= V_i - \left[\frac{V_i - (V_R + V_r)}{R + R_f}\right] R$$

$$= \frac{V_i(R + R_f) - V_i R + (V_R + V_r)R}{R + R_f}$$

$$= \frac{V_i R + V_i R_f - V_i R + V_R R + V_r R}{R + R_f}$$

$$V_o = \frac{V_i R_f + V_R R + V_r R}{R + R_f}$$

* Hence $R >> R_f$ we can neglect R_f

$$V_o = \frac{V_R R + V_r R}{R}$$

$$\boxed{V_o = V_R + V_r}$$

* However when diode is ON, it is seen that V_o is constant whatever the instantaneous magnitude of V_i. Hence there is clipping action. The portion of the input signal greater than $(V_R + V_r)$ is not transmitted.

* In practice, $V_R >> V_r$ we have $V_R + V_r \approx V_R$. Hence V_R itself can be taken as the level below which transmission occurs without clipping action, but beyond which clipping readily occurs.

* The transfer characteristics is as shown,

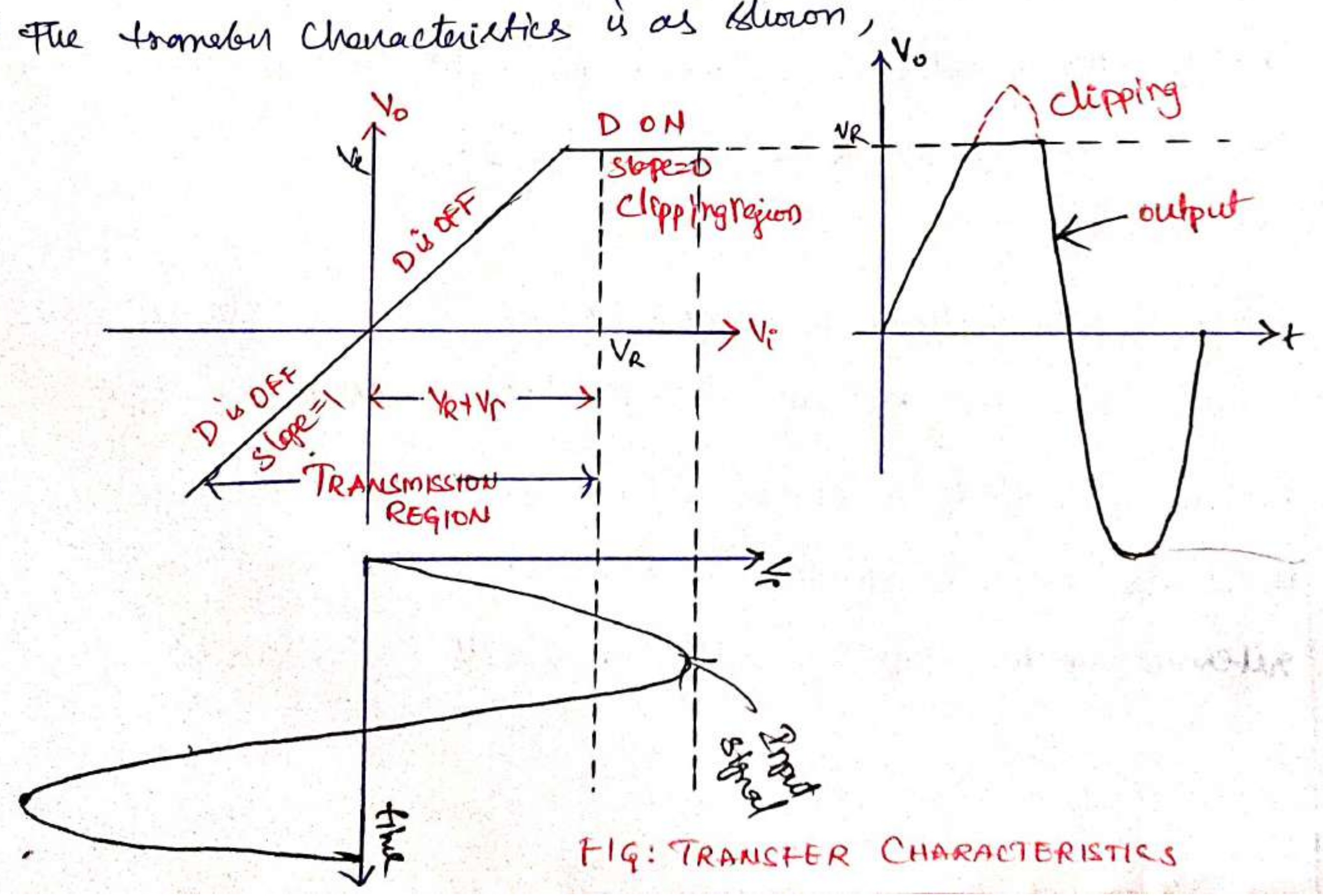
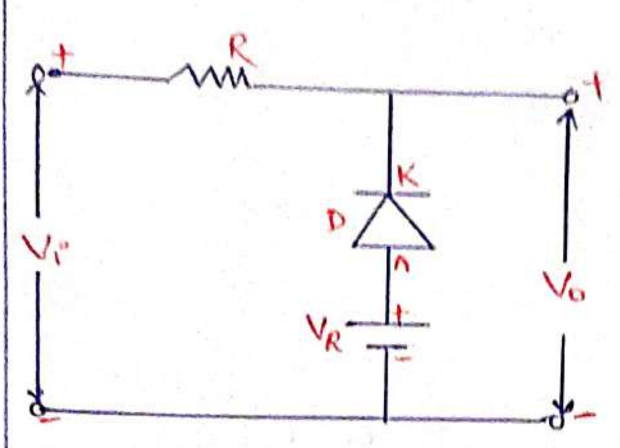


FIG: TRANSFER CHARACTERISTICS

CLIPPING BELOW THE REFERENCE VOLTAGE V_R:



* Let D be assumed as ideal diode, so that $R_f = 0$ and $V_r = 0$. V_R is the reference voltage, it is of fixed magnitude V_i is Input Voltage and V_o is the output voltage.

For $V_i < V_R$:

* For $V_i < V_R$ the diode is ON, the diode gets forward biased. The ideal diode acts as a short circuit and conduction readily occurs. there is no voltage drop across it ($R_f = 0$). Hence $V_o = V_R$
* When the diode is ON, clipping action readily takes place, since the output $V_o = V_R$ of constant magnitude.
* Thus for all values of $V_i < V_R$ the output voltage has the magnitude V_R. In other words, the portion of the input voltage waveform below the reference voltage V_R is readily clipped.

For $V_i > V_R$ -

* For $V_i > V_R$, diode D is OFF, since it gets reverse biased. There is no conduction, and no voltage drop across R. $V_o = V_i$.
* When the diode is OFF, we have $V_o = V_i$ and there is no clipping. Hence the portion of the input signal wave form lying above the reference voltage V_R is readily transmitted without attenuation.

Vo

Voltage

D OFF ← Transmission Region

D ON   D ON

Output Voltage

45°

0   V_R V_i

t

← clipping region →

Input Signal

0

→ V_i

↓time

FIG: TRANSFER CHARACTERISTIC

2. SERIES CLIPPERS :-

* In a series clipper using a resistor and a diode, the diode forms a series path connecting the input and output and the Resistor R comes in series with the reference voltage.

* Series clippers are also of two types.

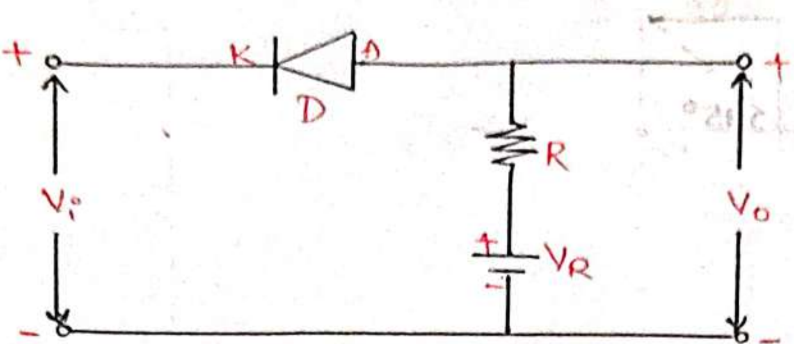
1. Clipping above the reference voltage V_R.
2. Clipping below the reference voltage V_R.

1. Clipping above the reference voltage V_R:

* In a series clipper circuit, employing a junction Diode D and it is seen that clipping action occurs above the reference voltage V_R.

* D is an ideal diode connected in the circuit that it forms a series path connecting the input and output.

* Since $R_f = 0$ for an ideal diode, the diode acts as short circuit when conducting and as open circuit when reverse biased.



FOR $V_i < V_R$:

* When $V_i < V_R$, the diode is forward biased and hence it conducts. Since it is ON, the diode acts as short circuit. It is obvious that $V_o = V_i$.

* For $V_i < V_R$, the Diode D is forward biased because its anode is at higher potential than its cathode.

* The difference voltage $(V_R - V_i)$ is dropped across R. Therefore $V_o = V_i$ and the slope of the transfer characteristic is 1.

* Since the input voltage is transmitted to the output without any change, this region is called transmission region.

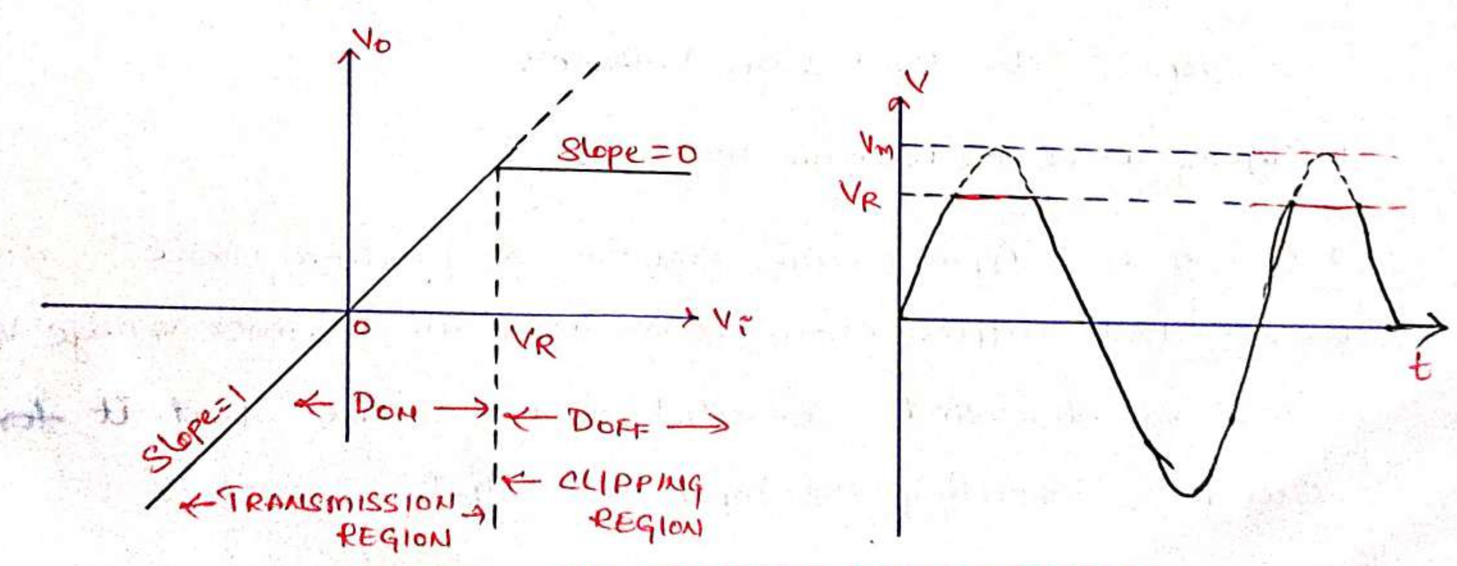


FIG: TRANSFER CHARACTERISTICS

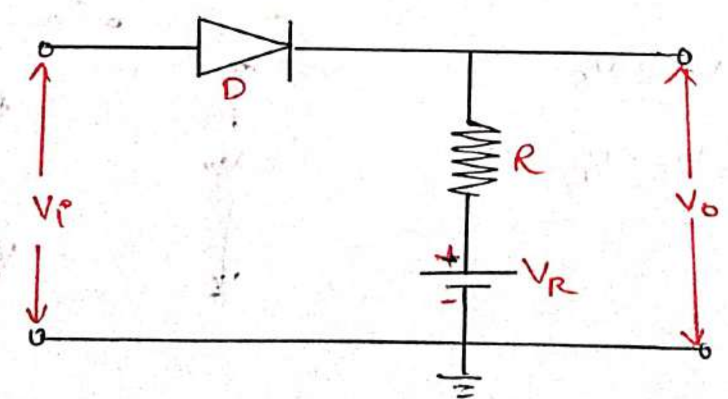
FOR $V_i > V_R$

* For $V_i > V_R$, the diode is reverse biased because its cathode is at a higher potential than its anode,
* It doesn't conduct and acts as open circuit. No current flows through R and so no voltage drop across it.
* The output voltage $V_0 = V_R$ and the slope of transfer characteristic is zero.
* Since the input signal above V_R is clipped off for $V_i > V_R$ this region is called the clipping region.

$$V_0 = V_i \text{ for } V_i < V_R$$
$$V_0 = V_R \text{ for } V_i > V_R$$

Clipping below the reference voltage V_R:

* A series clipper circuit uses P-N junction diode and a reference voltage source V_R. The diode is assumed to be ideal ($R_f = 0, R_r = \infty, V_f = 0$) so that it acts as a short circuit when it is ON and as a open circuit when it is OFF.
* Since the diode is in the series path connecting the input and the output it is called a series clipper.



For $V_i < V_R$:

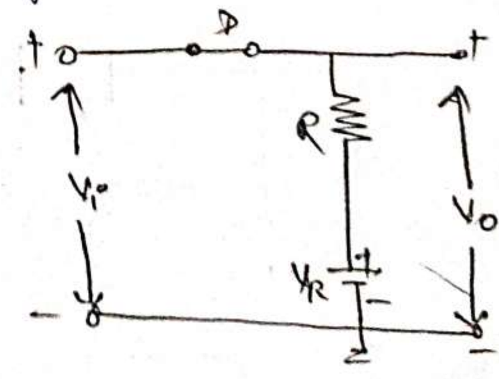
* For $V_i < V_R$, Diode D is reverse biased because its anode is at a lower potential than its cathode.
* The diode doesn't conduct and act as an open circuit. No current flows through R and hence no voltage drop across R, so $V_o = V_R$.
* So, the slope of the transfer characteristic is zero for $V_i < V_R$. Since the input is clipped off for $V_i < V_R$, this region is called the clipping region.

For $V_i > V_R$

* For $V_i > V_R$ the diode is forward biased because its anode is at a higher potential than its cathode.
* The diode conducts and acts as a short circuit. Current flows through R and the difference voltage between the input and the output voltages $V_i - V_R$, drops across R and the o/p $V_o = V_i$
* The slope of the transfer characteristic for $V_i > V_R$ is one. Since the i/p is transmitted to the o/p for $V_i > V_R$, this region is called the transmission region.

$V_o = V_R$ for $V_i < V_R$

$V_o = V_i$ for $V_i > V_R$



V_o Slope=1
Slope=0
V_R
← D_{OFF} → ← D_{ON} →
← Clipping region → ← Transmission region
V_R V_i

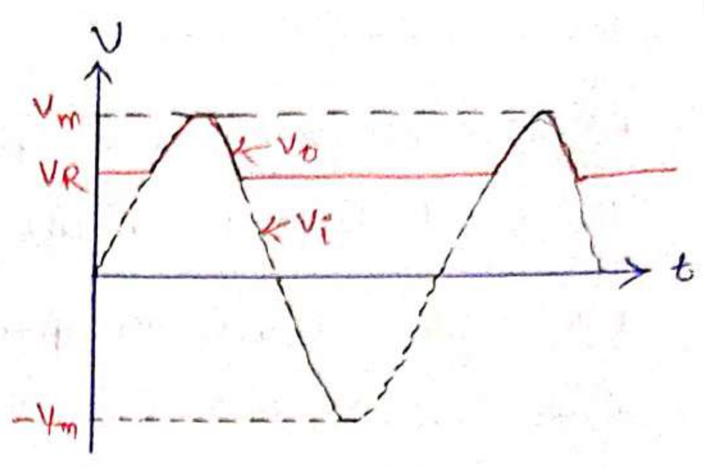


FIG: TRANSFER CHARACTERISTICS

CLAMPERS:-

* The circuits which are used to clamp or fix the extremity of a periodic waveform to some constant reference level V_R, such circuits are called as clamping circuits.
* When a signal is transmitted through a capacitive coupling network, it looses its dc component, and a clamping circuit may be used to introduce a dc component by fixing the positive or negative extremity of that waveform to some reference level.
* For this reason, the clamping circuit is often referred to as dc restorer or dc reinserter.
* The clamping circuit only changes the dc level of the input signal. It doesnot affect its shape.
* Basically clamping circuits are of two types
  1. Positive-voltage clamping circuit
  2. Negative-voltage clamping circuit

NEGATIVE CLAMPER:

* Negative clamper is also termed as a positive peak clamper since the circuit clamps the positive peak of a signal to zero level.

* In Negative clamper, the positive extremity of the waveform is fixed at the reference level and the entire waveform appears below the reference.

* That is the output waveform is negatively clamped with respect to the reference level.

* Assume that the signal source has negligible output impedance and that the diode is ideal $R_f = 0\Omega$ and $V_r = 0V$ so that input is a sinusoidal signal which begins at $t=0$. Let the capacitor C be uncharged at $t=0$.

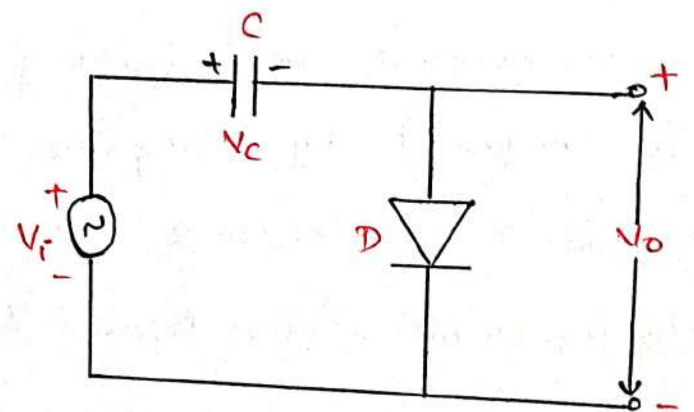


FIG: NEGATIVE CLAMPING CIRCUIT

WORKING:

* During the first quarter cycle, the input signal rises from zero to maximum value.

* The diode becomes forward biased and conducts ~~strongly~~ during this time, since we have assumed an ideal diode, the voltage across it is zero.

* The Capacitor C is charged abruptly through the series
of the signal source and the diode so that the voltage across
Capacitor rises sinusoidally.

* At the end of the first quarter cycle $V_c = V_m$.

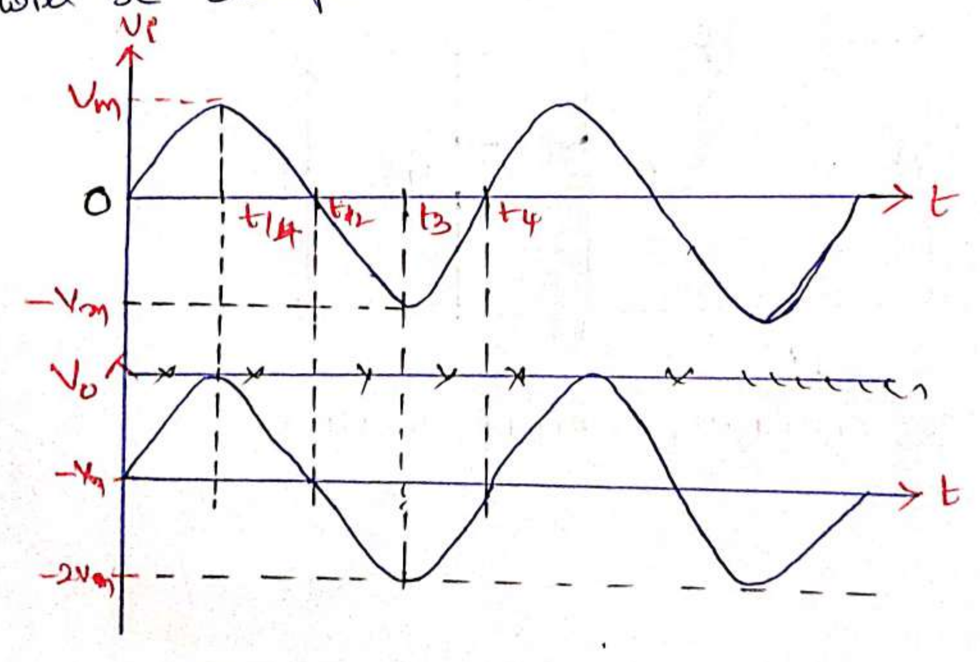
* When after the first quarter cycle the peak has been passed
and the input signal begins to fall. The voltage V_c across the
Capacitor is no longer able to follow the input, because there
is no path for the Capacitor to discharge.

* Hence the voltage across the Capacitor remains constant
at $V_C = V_m$, and the charged capacitor acts as a Voltage source
of V Volts.

* After the first quarter half cycle the output is given by

$$V_0 = V_i - V_m$$

* During the succeeding cycles, the positive extremity of the
Signal will be clamped & restored to zero



at $t = t_0$, $V_0 = V_i - V_m$

$V_i = 0$ $\boxed{V_0 = -V_m}$

at $t = t_1$ $V_0 = V_i - V_m$

$V_i = V_m$ $\boxed{V_0 = 0}$

at $t = t_2$ $V_0 = V_i - V_m$

$V_i = 0$ $\boxed{V_0 = -V_m}$

at $t = t_3$ $V_0 = V_i - V_m$

$V_i = -V_m$ $V_0 = -V_m - V_m$

$\boxed{V_0 = -2V_m}$

* Suppose the amplitude of the input signal is decreased after the steady state condition has been reached. There is no path for the capacitor to discharge.
* To permit the voltage across the capacitor to decrease, it is necessary to shunt a resistor across capacitor or equivalently shunt a resistor across the diode.

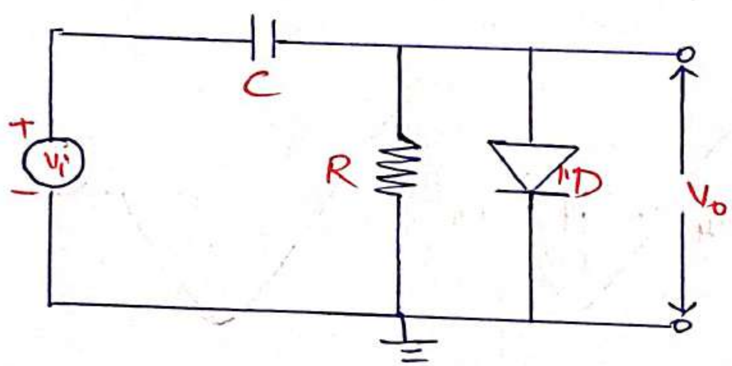


FIG: CLAMPING CIRCUIT WITH A RESISTOR

POSITIVE CLAMPER:

* Positive clamper is also termed as Negative peak clamper since this circuit clamps the negative peaks of a signal to zero level.
* In positive clamper, the negative extremity of the waveform is fixed at the reference level and the entire waveform appears above the reference level i.e., the output waveform is positively clamped with reference to the reference level.

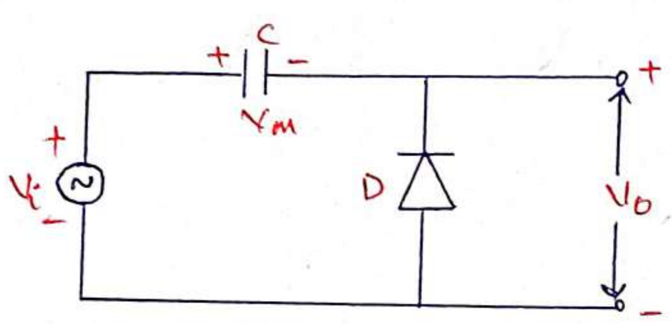


FIG: POSITIVE CLAMPING CIRCUIT

WORKING:

* During the negative half cycle of the input signal the diode becomes forward biased and conducts during this time. Diode is reverse biased during positive half cycle doesn't conduct.
* When V_i goes negative, diode gets forward biased and conducts and in a few cycles capacitor gets charged to the peak value V_m.
* The capacitor C is charged through the series combination of the signal source and the diode so that the voltage across capacitor rises sinusoidally.

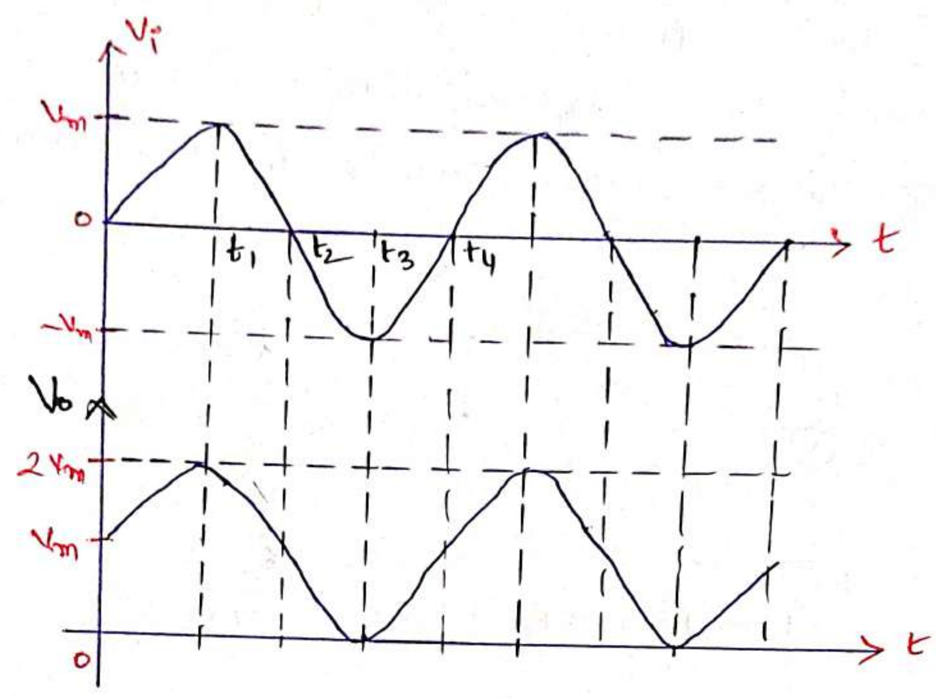
* Under steady - state conditions, the Capacitor acts as a constant voltage source and the output is

$$V_o = V_i - V_c$$

$$V_o = V_i - (-V_m)$$

$$\boxed{V_o = V_i + V_m}$$

(∵ Capacitor is charged during negative cycle and its peak value is $-V_m$)



at $t = 0$, $V_i = 0$

$$V_o = V_i + V_m$$

$$\boxed{V_o = V_m}$$

at $t = t_1$, $V_i = V_m$

$$V_o = V_i + V_m$$

$$V_o = V_m + V_m$$

$$\boxed{V_o = 2V_m}$$

at $t = t_2$, $V_i = 0$

$$V_o = V_i + V_m$$

$$\boxed{V_o = V_m}$$

at $t = t_3$, $V_i = -V_m$

$$V_o = V_i + V_m$$

$$= -V_m + V_m$$

$$\boxed{V_o = 0}$$

at $t = t_4$, $V_i = 0$, $V_o = V_i + V_m$

$$\boxed{V_o = V_m}$$

* To accomodate for variations in amplitude of input, the diode D is shunted with a resistor.

* When the amplitude of the input waveform is reduced, the output will adjust to its new value.

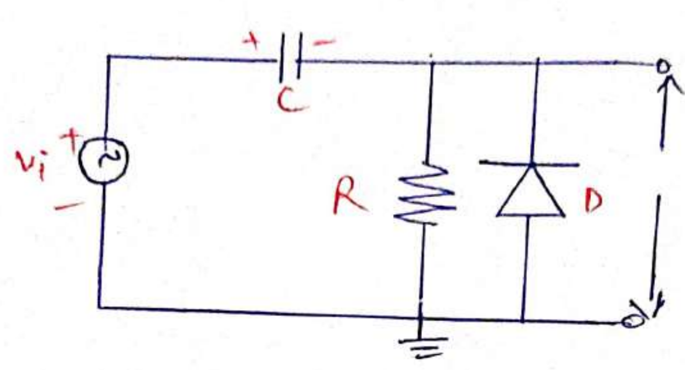


FIG: CLAMPING CIRCUIT WITH A RESISTOR.

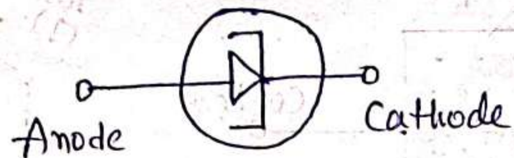
BIASED CLAMPING:

* If a voltage source of V_R is connected in series with the diode of a clamping circuit, the input waveform will be clamped with reference to V_R.

* Depending on the position of the diode, the input waveform may be positively clamped with reference to V_R or negatively clamped with reference to V_R.

TUNNEL DIODE:

SYMBOL: The Symbol of tunnel diode is



BASICS:

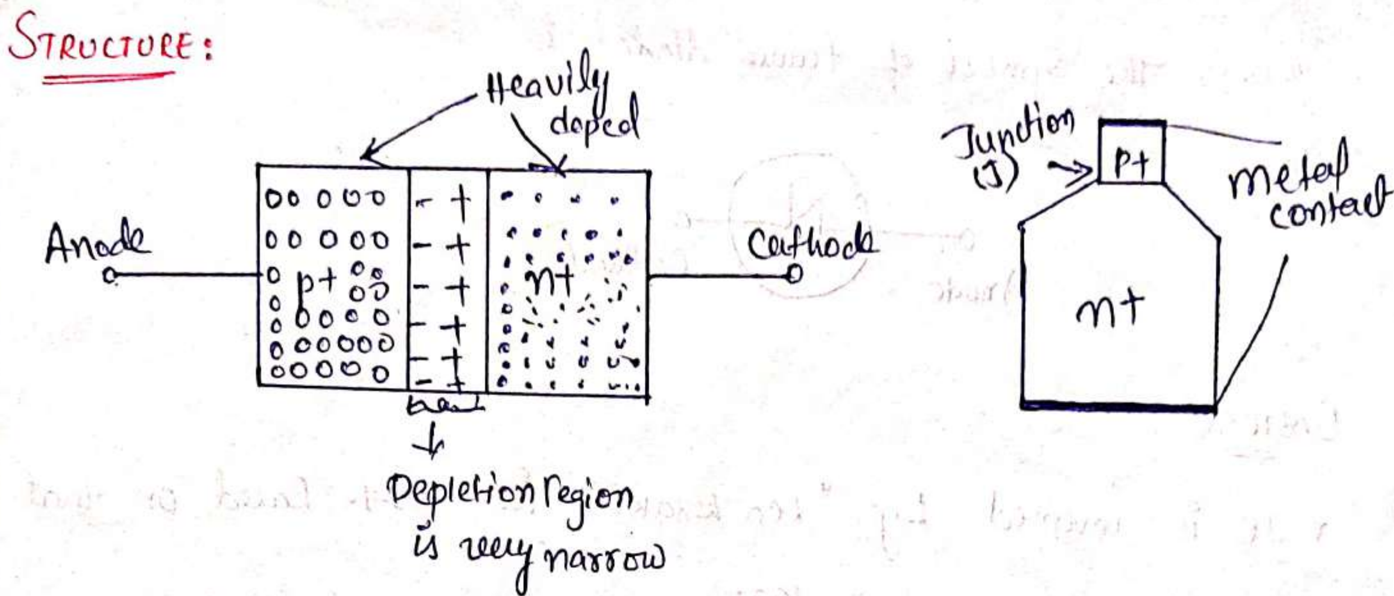
* It is invented by "Leo Esaki" in 1957. Based on that he have received Nobel in 1973.
* Sony have manufactured tunnel diode 1st in 1957 From 1960 onwards other Companies like "general Electrical" have started manufacturing of tunnel diode.
* The Basic operation of Tunnel diode is, it is used for "Fast - Switching" characteristic.
* It is utilized in microwave applications
* The working of Tunnel diode is based on "Quantum mechanical Tunneling".

i. Highest from room temperature, Solid State oscillators are based on (RTD) "Resonant Tunnelling diode".

ii. metal Insulator metal (MIM): Mostly it is used in "Research based applications".

* It is also called as "ESAKI DIODE".

STRUCTURE:



* The structure of Tunnel diode include p+ and n+ materials. These are Heavily-doped.

* Heavily-dopped means, the doping concentration of p and n type semiconductor is very high due to this, the "Depletion region" is very narrow (small), than the normal p-n junction diode.

* In the fabrication of tunnel diode, the p+ materials is very small than the n+ material i.e, size of p-type is very small, than the n-type material.

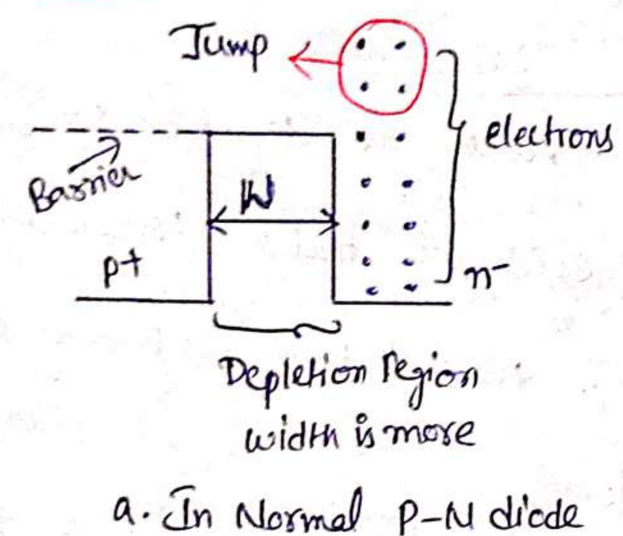
* At the top of p-type and at bottom of n-type materials a metal contacts are present as shown in figure

* In tunnel diode p and n materials are fabricated with the materials 1. Gallium Arsenide (GaAs) 2. Gallium Antimonide (GaSb) 3. Si (Silicon)

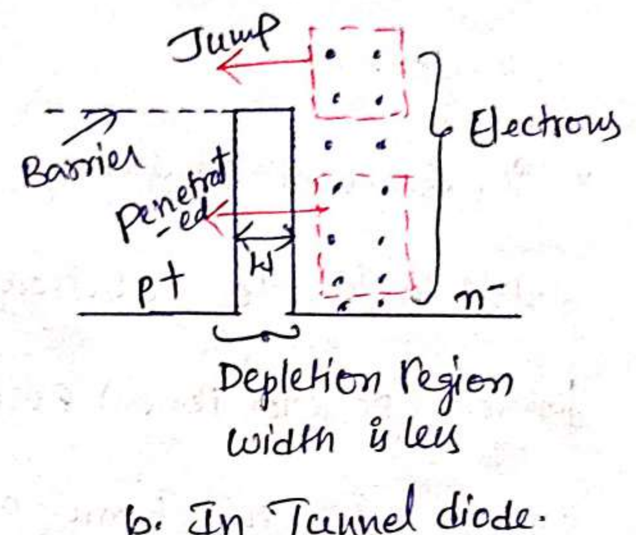
* A Junction is present in between p and n-type of Tunnel diode.

* The main difference between the Tunnel diode and P-N diode is, In tunnel diode the p and n regions are heavily doped but in P-N junction diode, p and n materials are lightly doped.

WORKING:



a. In Normal P-N diode



b. In Tunnel diode.

* In Normal p-n diode, the depletion region width is more due to lightly dopped. When the diode is forward bias, those electrons have greater potential energy than Barrier potential, those electrons only jump from n-type to p-type material these are participated to flow of current.

* In Tunnel diode, the depletion region width is less due to heavily dopped. When the tunnel diode is forward bias, those electrons have greater potential energy than the Barrier potential energy, those electrons jumps from n-type to p-type material along with these electrons, those electrons have lower potential energy than the energy of Barrier potential, those electrons penetrate through the junction

from n-type to p-type materials. these all electrons participated to flow of current. This process is "Tunnelling of electrons".
Tunnelling means "penetration of electrons through the barrier eventhough the electrons have less energy than the barrier potential.

* So, Quantum mechanics explains, when the depletion region width is less, then electrons can easily penetrated through the junction (Depletion Region) even though the electrons are having less energy than the barrier potential.

Characteristics:

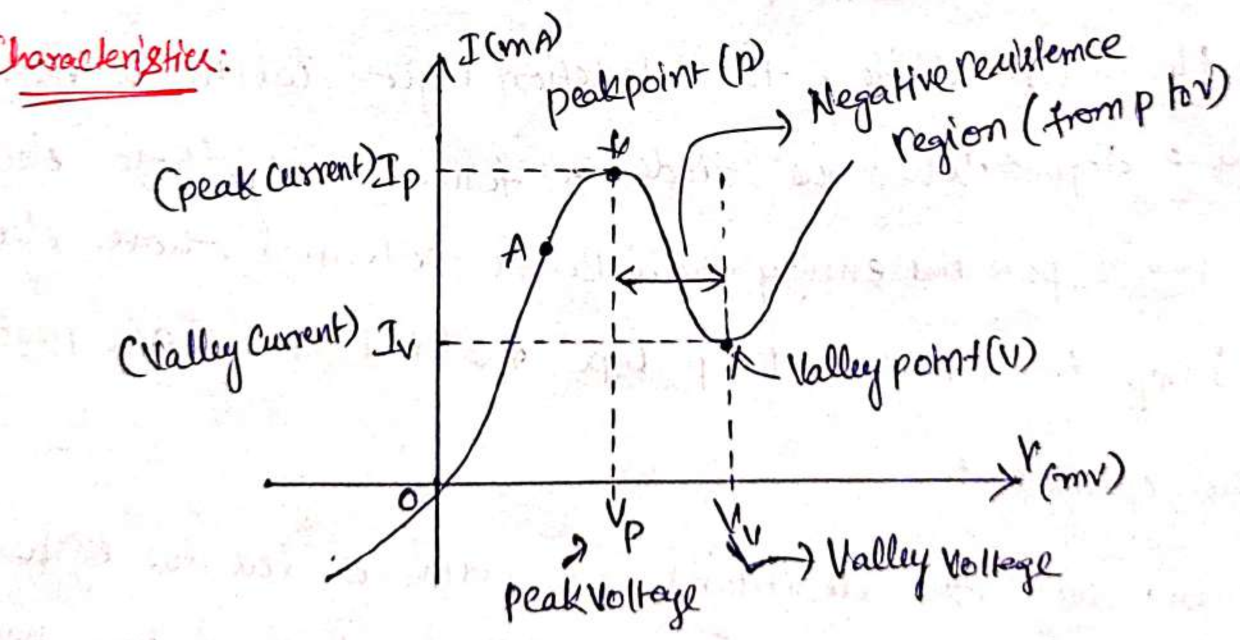


FIG: Characteristics (V-I) of Tunnel diode.

* When Tunnel diode is in forward bias the p-type material is connected to positive terminal and n-type material is connected to negative terminal of battery.
* Then the tunnel diode starts to conduct, the applied voltage

increases, the Voltage across diode and Current also increases exponentially and reached point A as shown in figure.

* When applied Voltage increases, then the current also increases upto the point 'P' which is peak point indicated as 'P' as shown in above. The corresponding current and Voltage is called as "peak Current" and "peak Voltage" (V_P).

* If we further increase voltage greater than the peak value the current will decrease up to the point 'V' which is called as "Valley point". The corresponding current and Voltage is called as "Valley Current" (I_V) and Valley Voltage (V_V).

* Valley point is Negative Resistance Region.

* Further increment of voltage (applied voltage) the diode again starts to conduct then this diode acts like a normal diode then the current increases from the Valley point again when we increase the applied voltage.

TUNNEL DIODE BAND DIAGRAM:

* By using Band diagram, try to understand what happens inside the tunnel diode with the Energy band diagram.

* The Characteristics of tunnel diode is explained by using Energy band diagram in different Cases.

Case(1): No BIAS (point 0)

* When No bias is applied to tunnel diode then the gap between the Conduction band and Valence band of p-type and n-type material is very high

* In this, total number of electrons and holes are equal then there is zero current i.e., no current flow through the diode and voltage is also zero.

p-type { E_c, E_v

E_g Gap is more So, tunnel diode acts as a "Insulator" (Zero Current)

E_c, E_v } N-type

Case 2: When the bias is applied (forward bias)

* When the diode is in forward bias, the voltage increases, the gap between Conduction and Valence band is reduced, then there is a flow of current.

* Due to increase in applied Voltage (F.B) the holes and electrons recombine and forms Covalent bonds and this bonds will break up. So that free electrons and holes are available because of this current flows in the tunnel diode up to point A.

E_c
E_v
0000000
p-type

Gap is reduced
diode acts as Semiconductor
current increases

E_c
E_v
n-type

FIG: FORWARD BIAS OF TUNNEL DIODE [at point A]

Case 3: Further Increment of Forwar bias (Voltage)

* In this case, we are going to increase the forward bias i.e., further increase in the applied Voltage then the gap between Conduction band and valence band is always equal (parallel) i.e, there is no gap between the conduction band and valence bands of p-type and n-type materials.
* Because of this high amount of current flows through the diode. This current is called as "Peak current" (I_p)

E_c
E_v
0000000

No gap both electrons & holes level is equal (parallel)
high amount of Current flow (peak current)

E_c
E_v

FIG: FORWARD BIAS (point 'p')

Case 4 : Further increase in the Voltage in F.B beyond Peak Voltage.

* In this, forward voltage is increased beyond the peak voltage then the levels of p and n-type materials are shifted and exchange their positions, due to high increase in applied voltage

* The level of electrons crosses the level of holes in valence band of p-type material and level of holes is decreased then the level of electrons in conduction band of n-type material.

* The flow of current decreased up to point V which is called as "valley point". The corresponding current is "valley current" and voltage is "valley voltage".

FIG: FORWARD BIAS (Point V)

Case 5:

* After decreasing the current (Valley Current) again this valley current increases at point B when further increment of applied voltage then the diode will work as in normal forward bias. In this case voltage increases then the current increases and reached at point B shown in characteristic curve

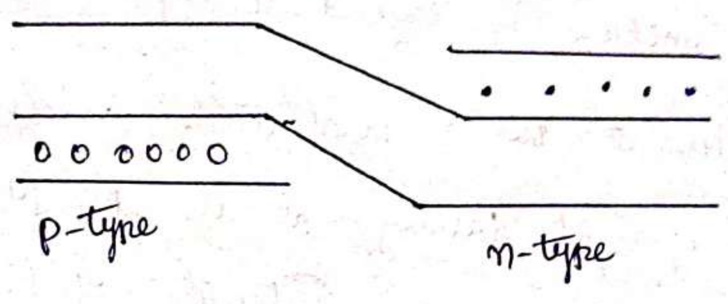


FIG: FORWARD BIAS (point-B)

ADVANTAGES:

1. Low Noise
2. Ease of operation
3. High speed
4. Low power

DISADVANTAGES:

1. Voltage range over which it can be operated is 1V.
2. Being ~~two~~ two terminal device there is no isolation between two regions.

APPLICATIONS:

* Tunnel diode is used as a Ultra high speed switch.
* As logic memory storage device.

* As amplifier
* As a microwave oscillator
* In relaxation oscillator circuit.

PHOTO DIODE:

Definition: A photodiode is a reverse bias silicon (or) Germanium, pn junction in which reverse current increases when the junction is exposed to light.

* The reverse current in a photodiode is directly proportional to the intensity of light falling at its pn junction.
* This means that greater the intensity of light falling on the pn junction of photo diode, the greater will be the reverse current.

PHOTO DIODE PACKAGE:

* The figure (a) shows a typical photo diode package

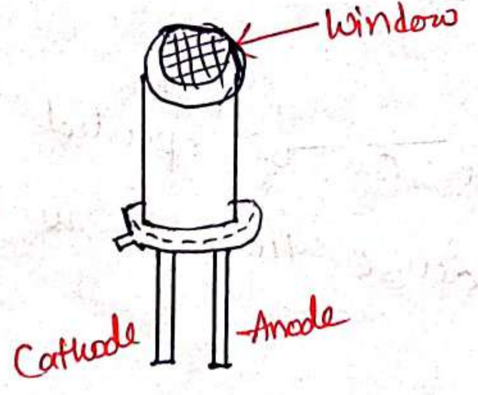


FIG a) PACKAGE

* It consists of a pn junction mounted on an insulated substrate and sealed inside a metal case.

* A glass window is mounted on top of the case to allow light to enter and strike the pn junction. The two leads extending from the case are labelled anode and cathode

* The cathode is typically identified by a tab extending from the side of the case.

SYMBOL:

→ Light source

Anode —▷|— Cathode

PRINCIPLE:

* The photo diode is connected in reverse biased condition. The Depletion region width is large, under normal condition it carries small reverse current due to minority charge carriers.

* When light is incident through glass window on the PN junction photons in the light bombard the p-n junction and some energy is imparted to the valence electrons.

* Due to this, valence electrons are dislodged from the covalent bonds and become free. Thus more electron-hole pairs are generated

* Thus total number of minority charge carriers increases and hence the reverse current increases. This is the basic principle of operation of photo diode

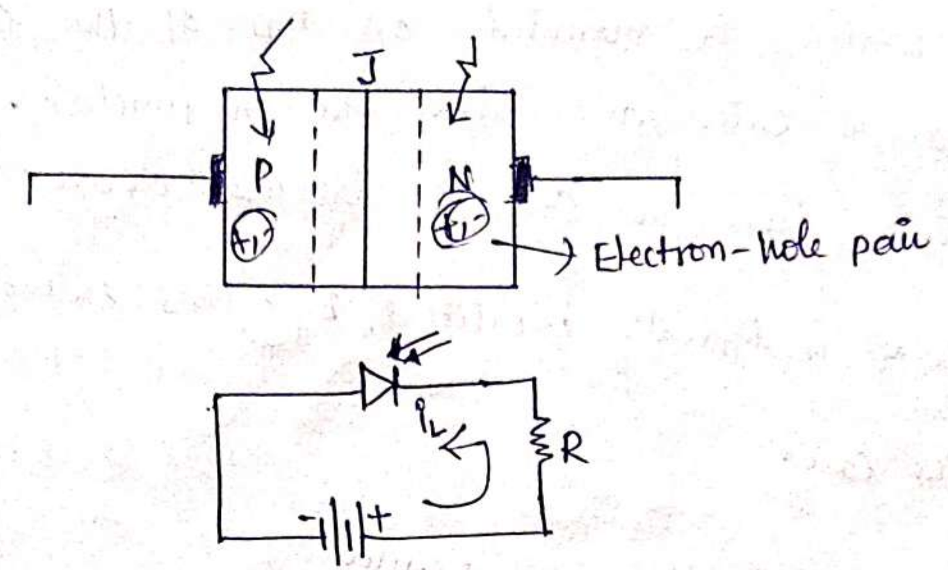
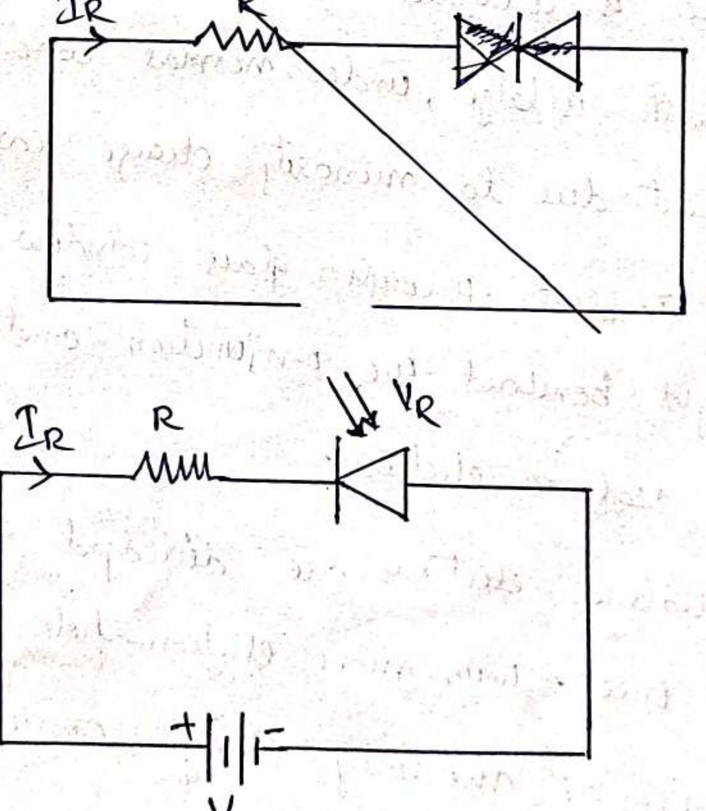


FIG: PRINCIPLE OF OPERATION

OPERATION:

* The basic photo diode circuit is as shown below. The circuit has reverse biased photo-diode, resistor R and d.c supply.



i). When no light is incident on the p-n junction of photo diode the reverse current I_r is extremely small. This is called "Dark current".

*The resistance of photo diode with no incident light is called 7 Dark resistance (R_R).

→ Dark resistance of photo diode $R_R = \frac{V_R}{\text{Dark Current}}$

ii) When light is incident on the p-n junction of photo-diode, the reverse current, I_R is extremely increases i.e, there is a transfer of energy from the incident light (photons) to the atoms in the junction. This will create more free electrons and more holes. This additional free e^- and holes increases the reverse current

iii) As the intensity of light increases, the reverse current I_R increases it till it becomes maximum this is called "Saturation Current".

CHARACTERISTICS OF PHOTODIODE:

i) Reverse current illumination Curve:

* The fig(a) shows the graph between (I_R) and illumination (E) of a photo diode. The reverse current is shown on the vertical axis and is measured in μA. The illumination is indicated on the horizontal axis and is measured in mw/cm². The graph is a straight line passing through the origin.

$$I_R = mE$$

where m = Slope of the straight line

E = Sensitivity of photo diode.

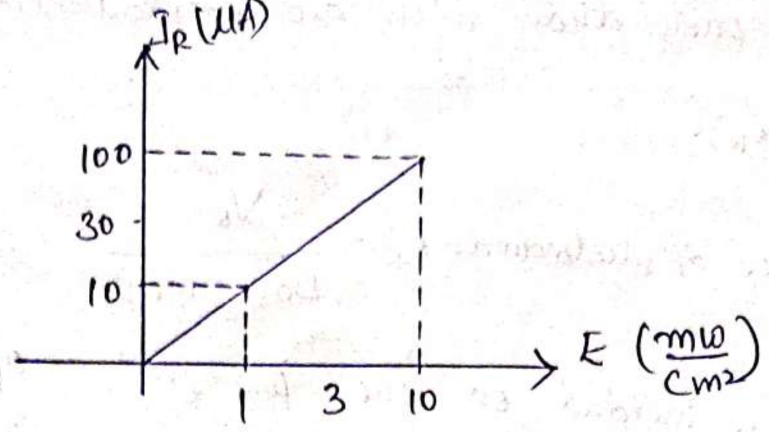


Fig (a). Reverse Current - Illumination Curve

ii) Reverse Voltage and Reverse Current Curve:

* It shows the graph between Reverse current (I_R) and Reverse voltage (V_R), for various illumination levels. It is clear that for given Reverse-biased voltage V_R, the reverse current I_R increases, as the illumination (E) on the pn junction of photodiode increases.

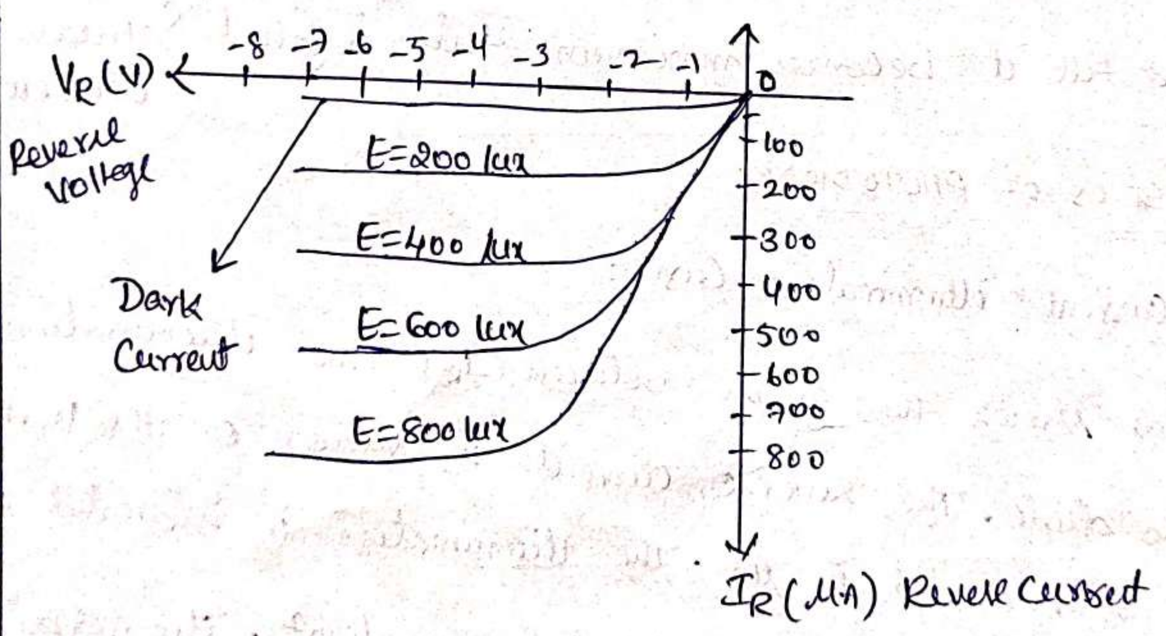


FIG (b): REVERSE VOLTAGE Vs REVERSE CURRENT CURVE

ADVANTAGES:

1. It can be used as a variable resistance device.
2. Highly sensitive to the light
3. The speed of operation is very high. The switching current and hence the resistance value from high to low or otherwise it is very fast.

DIS-ADVANTAGES:

1. The Dark Current I_λ is temperature dependent.
2. The overall photo diode characteristics are temperature dependent hence have poor temperature stability
3. The current and change in current is in the range of μA which may not be sufficient to drive other circuits. Hence amplification is necessary.

APPLICATIONS:

1) Alarm Circuit using photodiode:

1) Alarm Circuit using photo-diode in an alarm System.

* The figure 1. shows the use of photo-diode in an alarm System. Light from a light source is allowed to fall on a photo diode fitted in the doorway. The reverse current I_R will continue to flow so long as the light beam is not broken and the reverse current drops to the dark current level. As a result, an alarm is sounded.

VARACTOR DIODE:

Definition:

* Varactor diode also known as Variable Capacitor diode is a junction diode and its junction capacitance (Transition Capacitance) can be varied electrically (by changing applied voltage).

SYMBOL:

Anode —▷|/|— Cathode

* Here, arrow '↗' indicates variable (can vary the voltage and current) two parallel lines '||' indicates capacitor.

STRUCTURE:

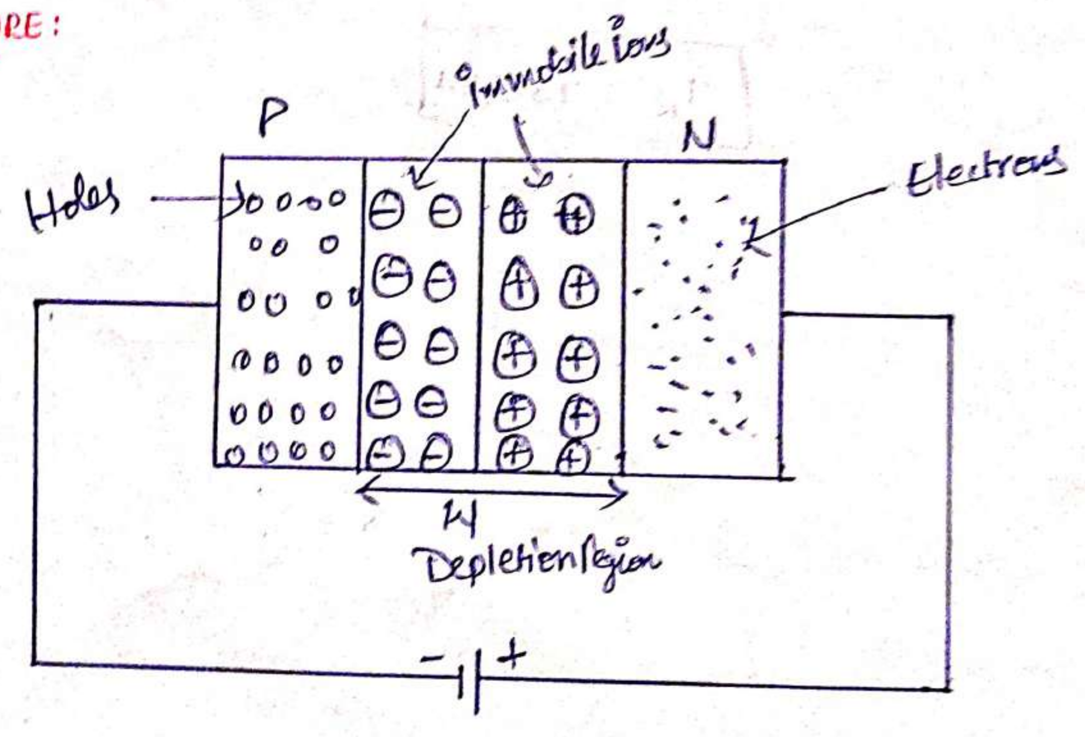


FIG: REVERSE BIASED PN JUNCTION DIODE

* When the diode is reverse biased, a depletion region is formed as shown in figure. The larger the reverse biased across the diode, the width of the depletion region "W" becomes wider.

* By decreasing, the reverse bias voltage, the depletion region width 'W' becomes narrower.

* In this region, the depletion region acts like a insulator preventing conduction between N and P layers of the diode, just like a dielectric.

* The P and N regions layers acts like a plates of the capacitor.

* The structure of the p-n junction diode in reverse biased condition is just like a capacitor. So it is called varactor (or) vari-cap diode i.e., variable capacitor.

* When the reverse bias voltage increases, the width of the depletion region decreases and capacitance becomes smaller.

* The capacitance C_T of a varactor diode is determined by using the equation,

$$C = \frac{\varepsilon A}{}$$

$$C_T \propto \frac{A}{W_d}$$

$$C_T = \frac{\varepsilon A}{W_d}$$

where ε = permitivity of semiconductor material

A = Area of cross section

W = width of the depletion region

* The width of the depletion region increases when the reverse bias voltage is increased.

i.e., $C_T \propto \frac{1}{W}$

* Transition capacitance decreases when the width of the depletion region increases.

∴ Transition capacitance varies inversely with the reverse voltage.

Characteristics:

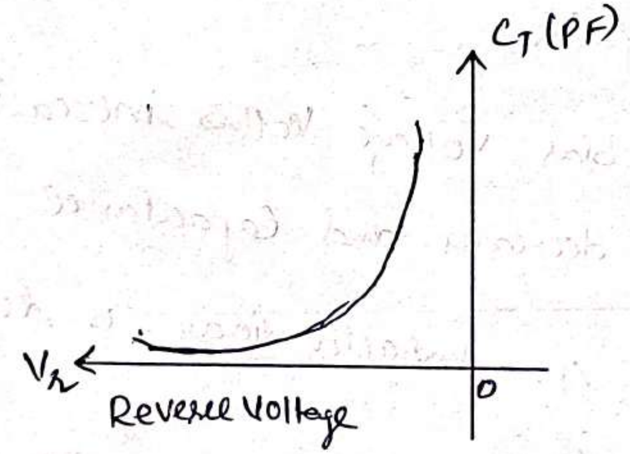


FIG: Characteristics between V_R & C_T

* From the characteristic curve, the capacitance is inversely proportional to the reverse bias voltage.

$$C_T \propto \frac{1}{V_R}$$

$$C_T \propto \frac{1}{W} \rightarrow (1)$$

$$W \propto V_R \rightarrow (2)$$

* If V_R increases then C_T decreases and viceversa.

Advantages:

1. It has low noise i.e., it generates low noise compared to other diodes.
2. It is portable due to small size.
3. Light weight and more reliable.
4. Low cost.

DISADVANTAGES:

* It is specially designed only to work in Reverse bias mode, thus it posses low significance when operated in Forward bias.

APPLICATIONS:

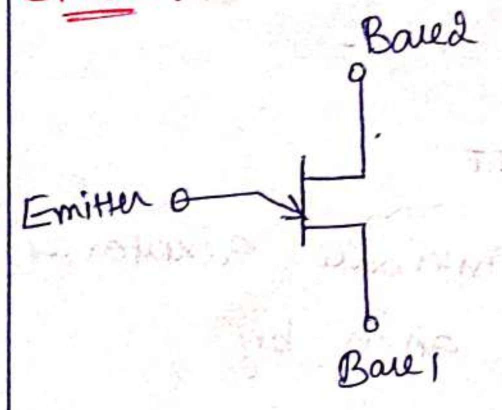
* FM radio & TV receivers.
* Self adjusting bridge circuits
* Adjustable bandpass filters
* Tuning of LC resonant circuits in microwave multipliers
* Very low noise microwave parametric amplifier.

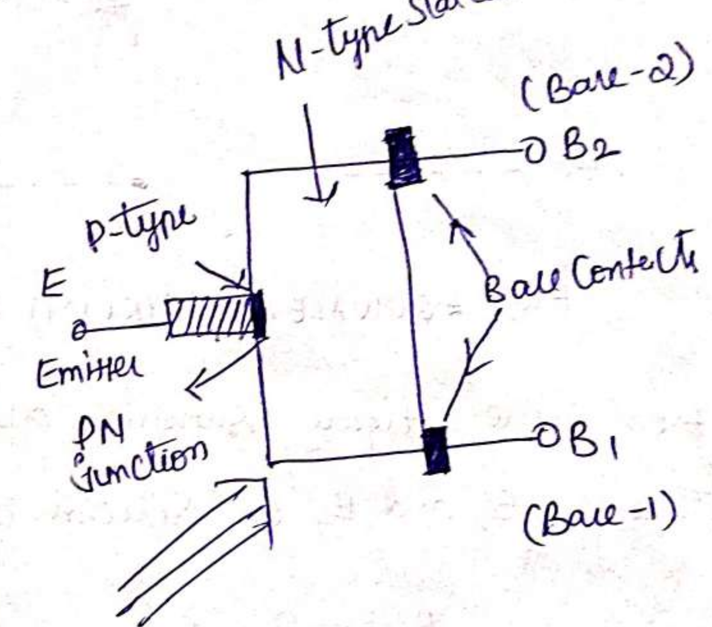
UNI-JUNCTION TRANSISTOR [UJT]

UJT:

* UJT is abbreviated as "Uni-Junction Transistor".
* It is a three terminal device semiconductor switching device.
It has only one PN Junction that's why it is called as a "Uni-Junction Transistor".

SYMBOL:





STRUCTURE:

* The Basic structure of UJT is shown in figure.
* It consists of lightly doped N-type Silicon bar with heavily doped p-type material diffused to its one side closer to B_2 bar producing single PN junction. UJT has 3 terminals. They are Emitter, Base 1, Base 2. (Here the Emitter leg is drawn at an angle to the vertical and arrow indicates the direction of conventional current.

Equivalent Circuit:

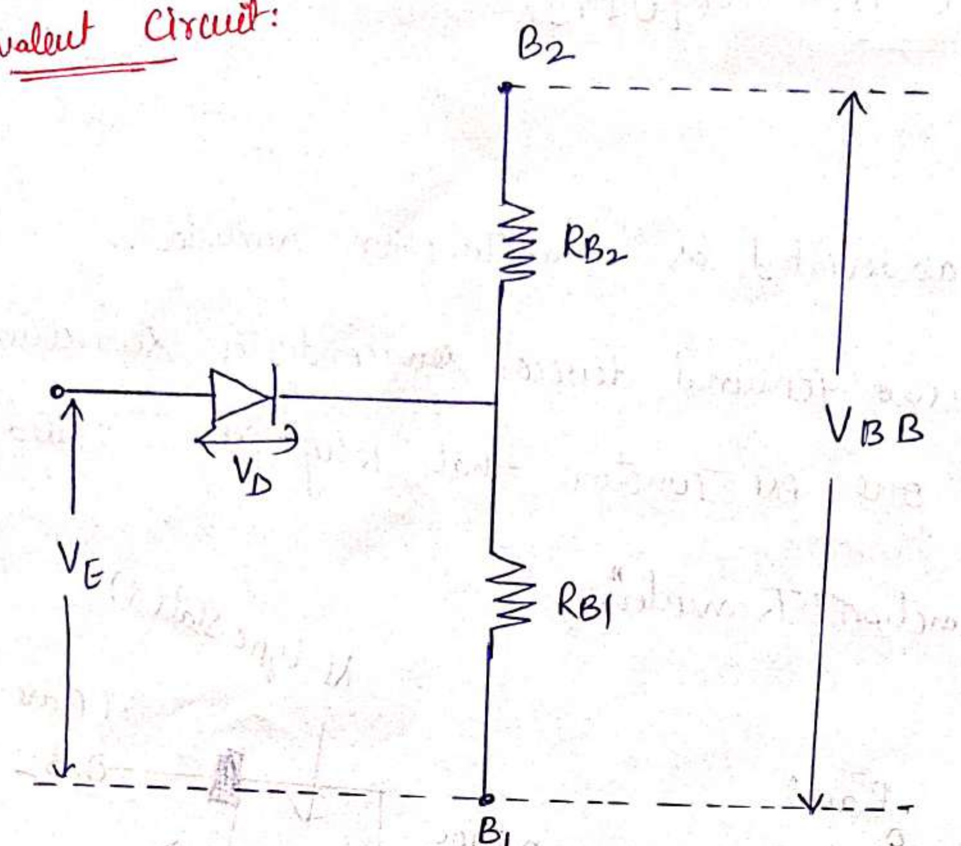


FIG: EQUIVALENT CIRCUIT OF UJT

* From the figure shown above interbase resistances between B_2 and B_1 of Silicon bar is given by,

$$R_{BB} = R_{B1} + R_{B2}$$

* If V_{BB} is applied between two bases, with emitter open voltage gradient is established along the Silicon N-type bar.

* The Voltage across RB1 is given by,

$$V_A = \frac{R_{B1} \cdot V_{BB}}{R_{B1} + R_{B2}} \simeq \left(\frac{R_{B1}}{R_{B1} + R_{B2}}\right) \cdot V_{BB}$$

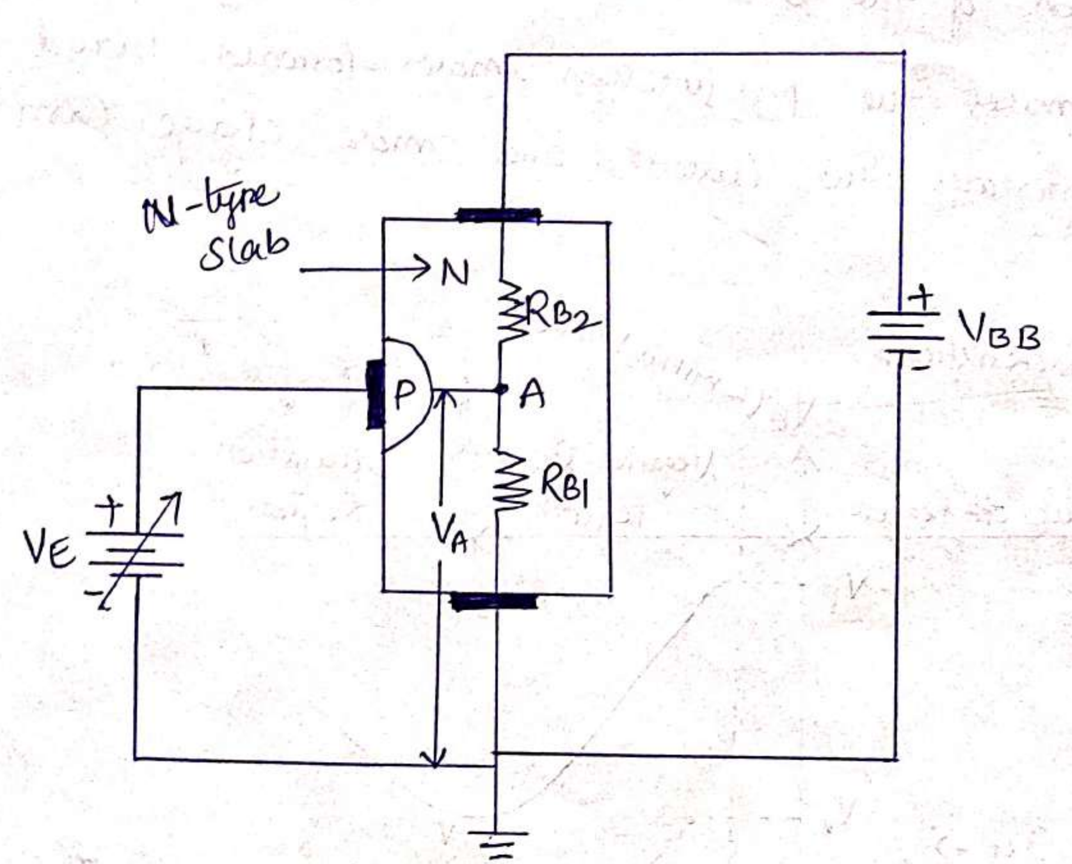
$$\therefore V_A = \eta V_{BB} \qquad \text{where, } \eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

η - is the Intrinsic Standoff Ratio.

$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}}$$

* Typical value of η ranges from 0.56 to 0.75.

OPERATION:



* The supply Voltage V_{BB} is Connected between B_1 & B_2 while variable emitter voltage V_E is applied to Emitter shown in figure.
* The potential of A is decided by η ($V_A = \eta V_{BB}$).

Case (i): when $V_E < V_D + V_{RB1}$ (or) $V_E = 0$

* when no voltage applied at the Emitter, the p-N junction is reverse biased. Hence Emitter current I_E will not flow. Then UJT is said to be "OFF".

Case (ii): $V_E \geq V_D + V_{RB1}$

* The diode drop V_D is generally between 0.3 to 0.7V

$$V_P = V_A + V_D = \eta V_{BB} + V_D.$$

* When $V_E > V_P$ then the P-N junction becomes forward biased and current I_E flows.

* Due to this the charge carriers are injected in the RB1 region of the bar then conductivity increases.

* This makes the p-n junction more forward biased which further increases the current and more charge carrier are injected.

UJT Characteristics:

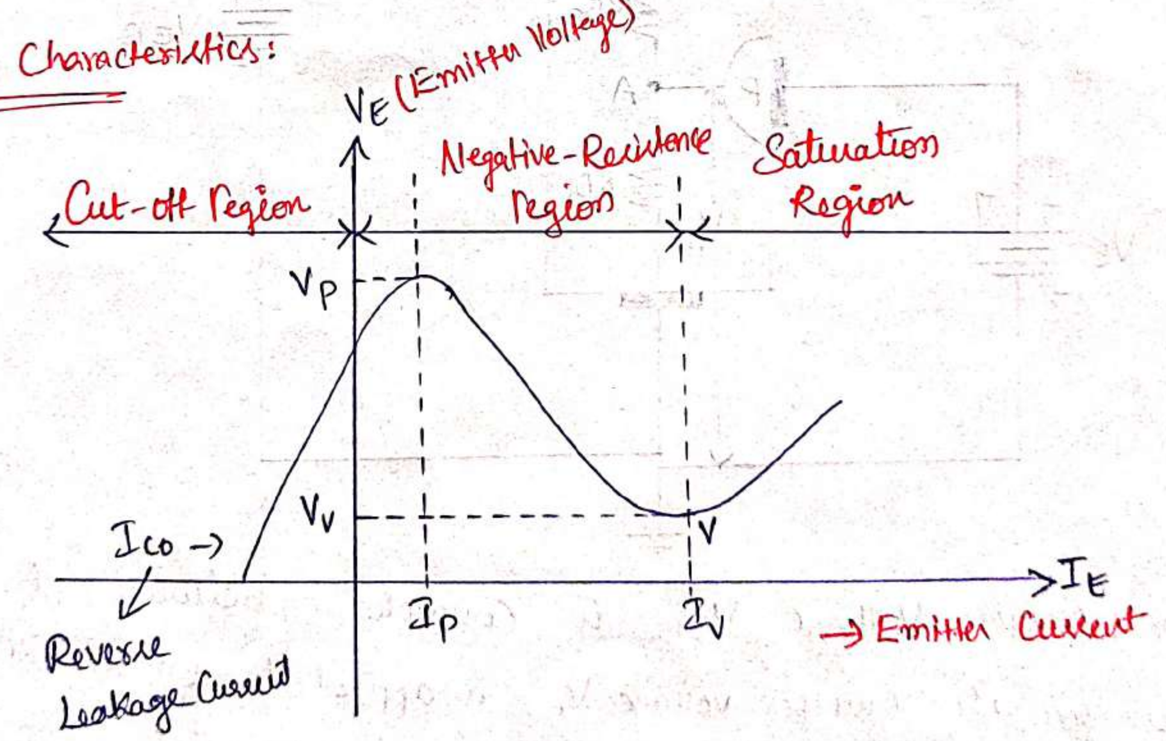


FIG: Characteristics of UJT.

Cut-off Region: The $V_E < V_P$ and the p-n junction is Reverse biased. A small amount of leakage current I_{EO} flows through the device which is Reverse Saturation Current.

* Negative- Resistance Region:

→ When $V_E = V_P$ the P-N junction becomes forward biased and I_E starts flowing. The V_E decreases, I_E increases. Hence the Region is called Negative Resistance Region.

* Saturation Region:-

→ Increases in I_E further valley point current I_V drives the device in the Saturation Region. The Voltage Corresponding to valley point is called "Valley point Voltage" in the valley point, the resistance Changes from negative to positive and after the point V current I_V increases the Voltage also increases.

Advantages:

* It is low Cost device.
* It has Excellent characteristics
* It is a low-power absorbing device under normal operating conditions.
* A negative resistance characteristics
* Very low value of triggering current.

Disadvantages:

* The main disadvantage of UJT is its inability to provide appropriate amplification.

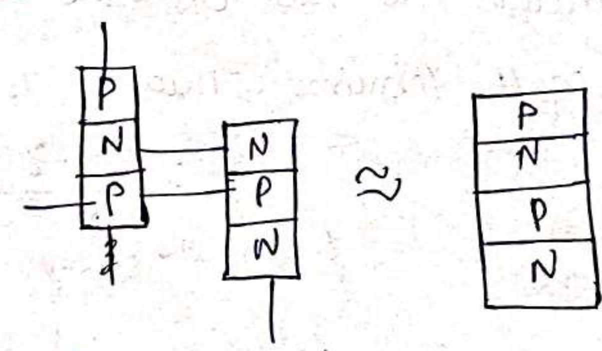
SILICON CONTROLLED RECTIFIER:

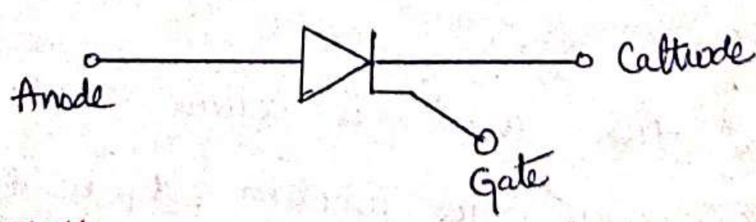
Meaning of SCR: SCR is an unidirectional device like diode. It allows flow of current in only one direction. SCR has a built in feature to switch "ON" and "OFF".

* It belongs to Thyristor family

* Diodes turned as uncontrolled rectifiers as they conduct whenever anode Vtg (i/p) is greater than cathode but in SCR it doesn't conduct even though anode Vtg is greater than cathode Vtg, unless the gate is triggered.

SYMBOL:-





CONSTRUCTION:

* The SCR is a four layer p-n-p-n device where p and N layers are alternately arranged.

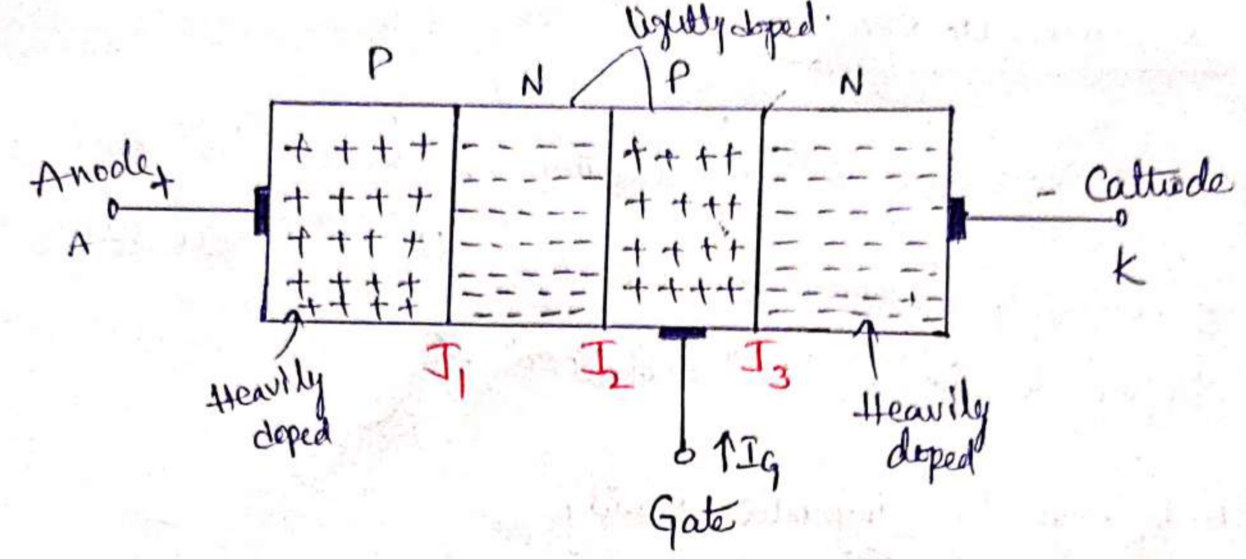


FIG: Physical Structure of SCR.

* The outer layers are heavily doped. There are three P-N junctions called J_1, J_2, J_3. The outer p-layer is called "Anode".

* While outer n-layer is called "Cathode". Middle p-layer is called "Gate".

* Anode must be positive with respect to cathode to forward bias the SCR. But this is not sufficient to turn ON SCR. Current must be passed through the Gate terminal. Thus it is a Current operated device.

OPERATION OF SCR:

* The operation of SCR is divided into two categories.

When Gate is open:

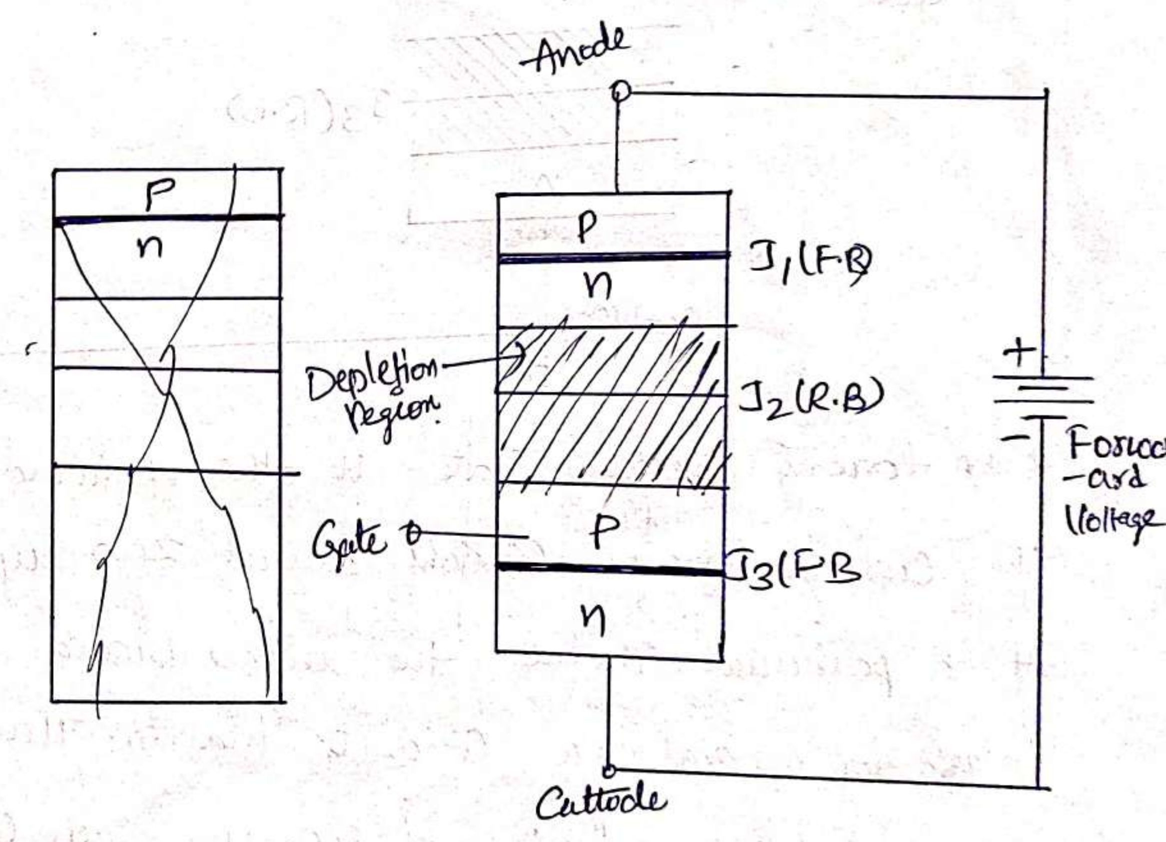
Case (1): Consider that the anode is positive with respect to cathode and gate is open. The junction J_1 is forward bias and J_3 is also in forward bias and junction J_2 is Reverse biased.

$J_1, J_3 \rightarrow$ Forward bias

$J_2 \rightarrow$ Reverse bias

* There is a depletion region around J_2 and only leakage current flows which is negligibly small practically SCR said to be "OFF". This is called the "Forward Blocking State" of SCR.

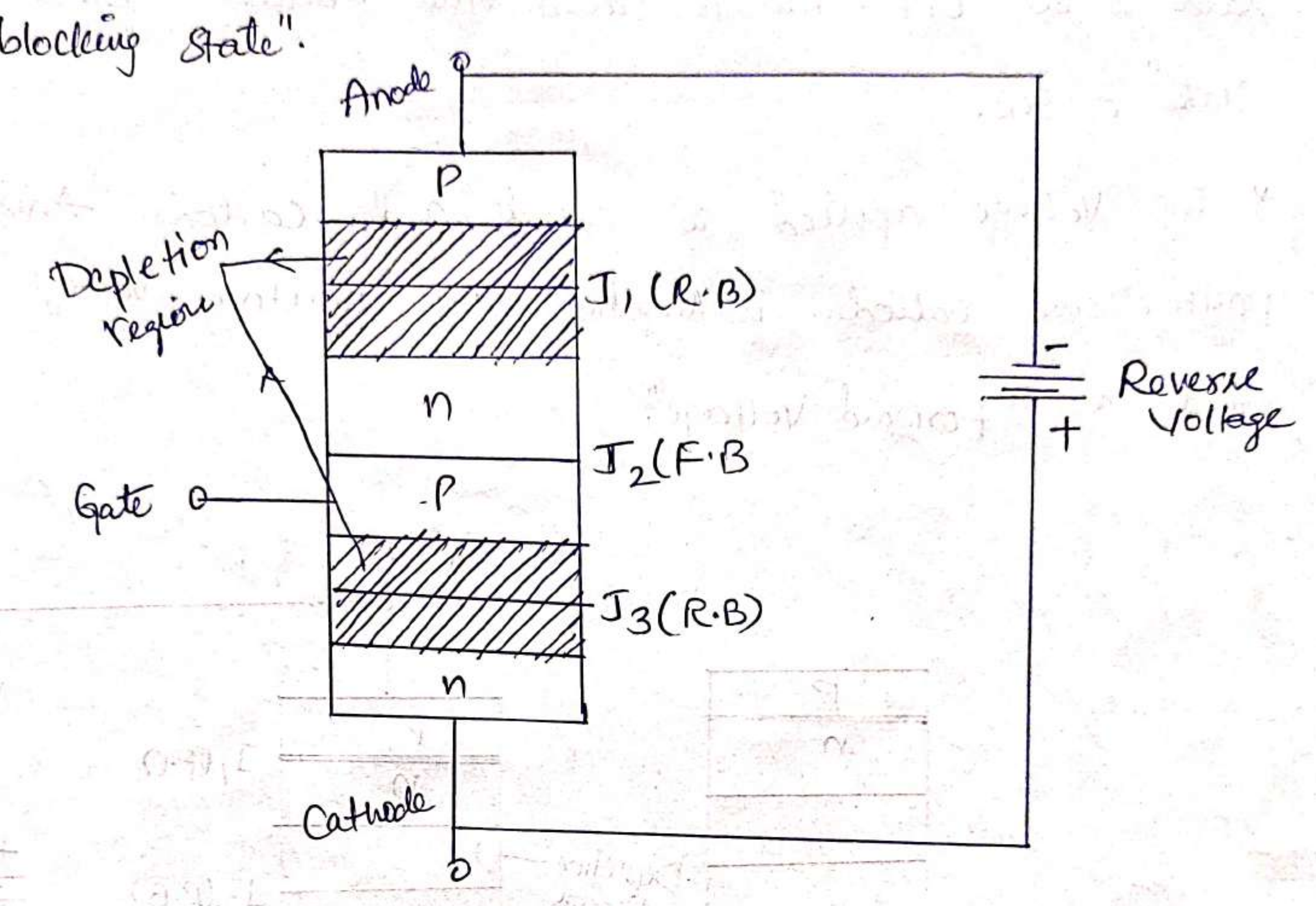
* The voltage applied to anode and cathode. Anode is positive and cathode is negative. The positive voltage is called as "Forward Voltage".



Case(2):

* With gate open, if cathode is made positive with respect to anode. The junction J_1, J_3 becomes reverse biased and J_2 is forward biased. The current flowing is leakage current, which can be neglected because it is very small.

* The voltage applied to make anode positive is called "Reverse Voltage" and SCR is said to be in "Reverse blocking state".

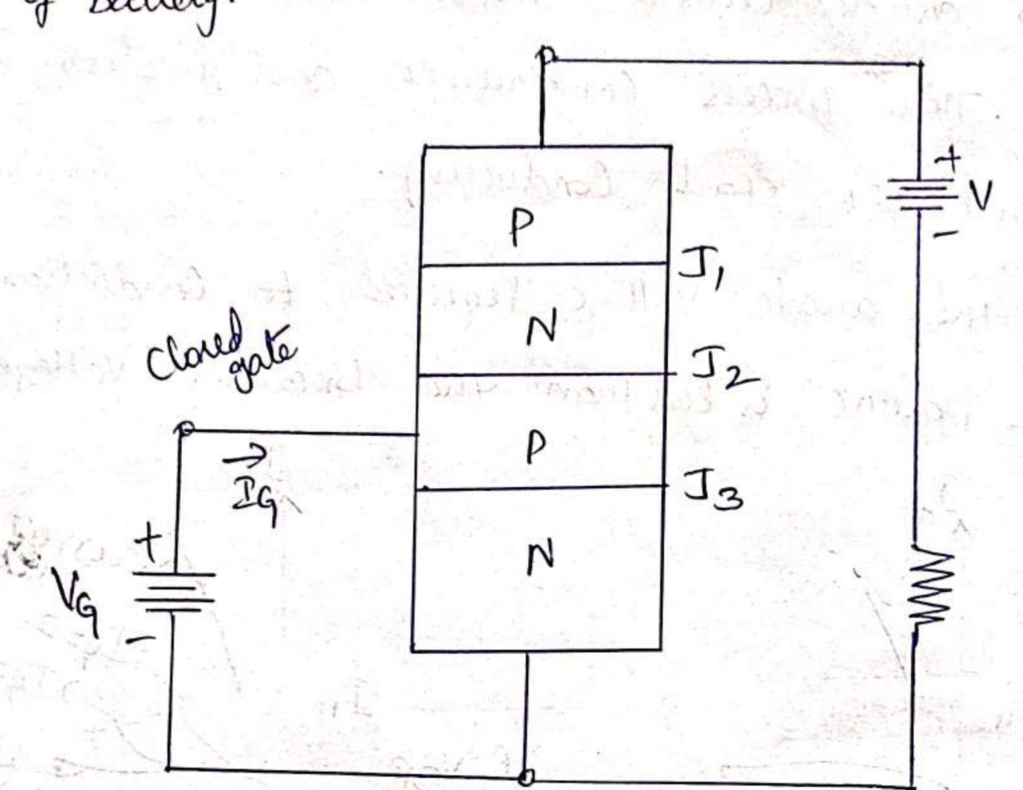


* In forward blocking state. If the forward voltage is increased the current remains constant almost zero upto certain limit. At a particular value the reverse biased junction J_2 breaks down and SCR conducts heavily. This voltage is called "Forward breakover" V_{BO} of SCR. In such case SCR is said to be "ON" or triggered.

2. When Gate is Closed:

* Consider that the applied voltage between gate and cathode when SCR is in forward blocking state. The gate is made positive with respect to the cathode.

* The electrons from n-type cathode which are majority in number, cross the junction J_3 to reach to positive of battery.



* While holes from p-type move towards the negative battery. This constitute the gate current. This current increases the anode current, as some of the electrons cross junction J_2 and the anode current increases. ~~more~~ Due to the regenerative action, within short time, the junction J_2 breaks and SCR conducts heavily.

Characteristics:

* When a small positive voltage is applied to gate and the anode is connected to positive terminal of the supply as shown. The junction J_3 is forward bias, junction J_2 is reverse biased. The electrons from N_2 layer starts moving across the junction J_3 where as the holes from P_2 layer

layer Cross Junction J_3. As a result the gate current starts flowing which increases the anode current.

* The increased anode current make more electrons available at junction J_2. This process continuous and junction J_2 breakdown and SCR starts Conducting.

* Note that the anode Voltage required for Conduction when gate is positive is less than the breakover Voltage.

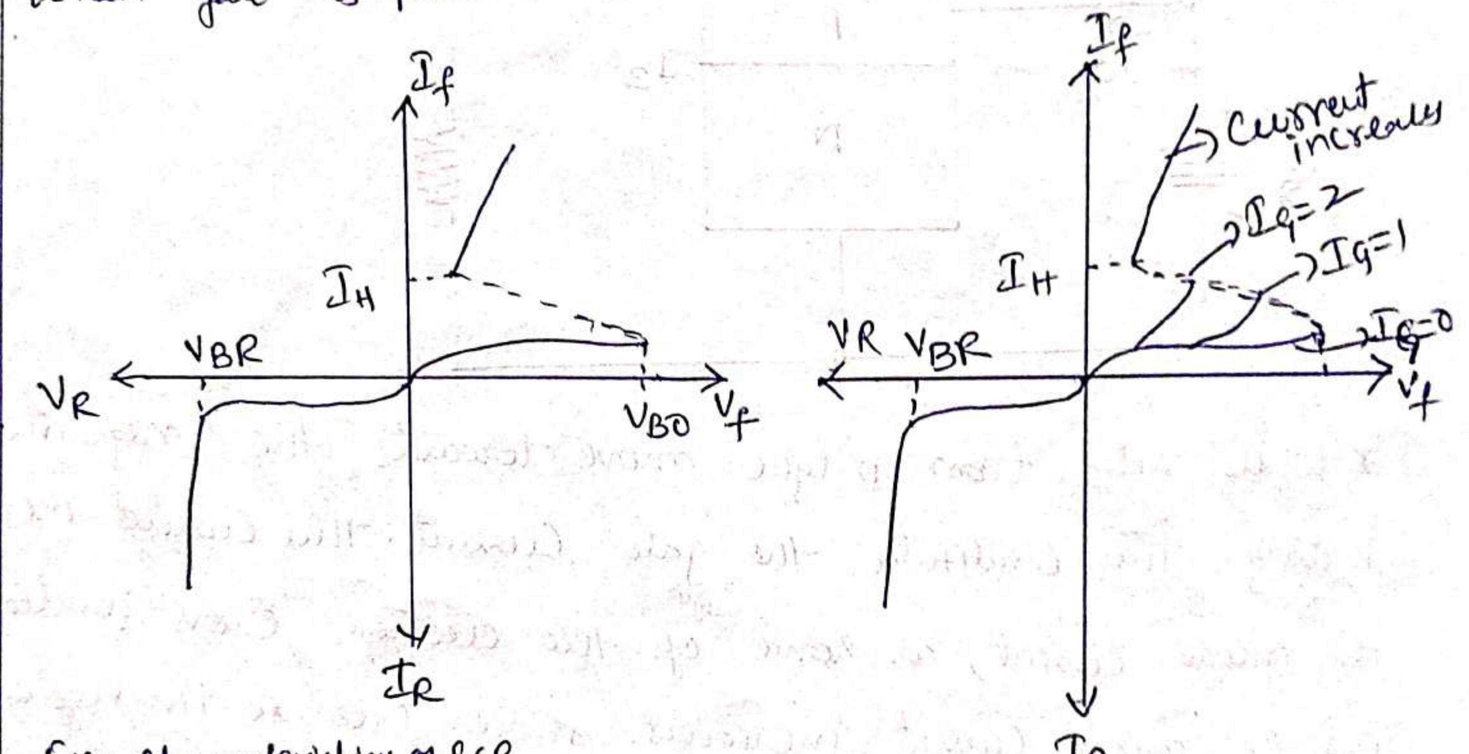


Fig: Characteristics of SCR

Fig: Characteristics of SCR for different values of Ig.

* When anode is negative wrt Cathode, the curve between V and I is known as reverse characteristics. When reverse Voltage is applied to SCR, the current through SCR is very small (leakage current).

* When reverse voltage increases gradually, a stage reached at which the avalanche breakdown occurs and SCR starts conducting heavily. Then the voltage is called reverse breakdown voltage.

Break over Voltage V_{BO}:

* It is defined as the voltage at which the SCR enters the conduction region.

Holding Current (I_H):

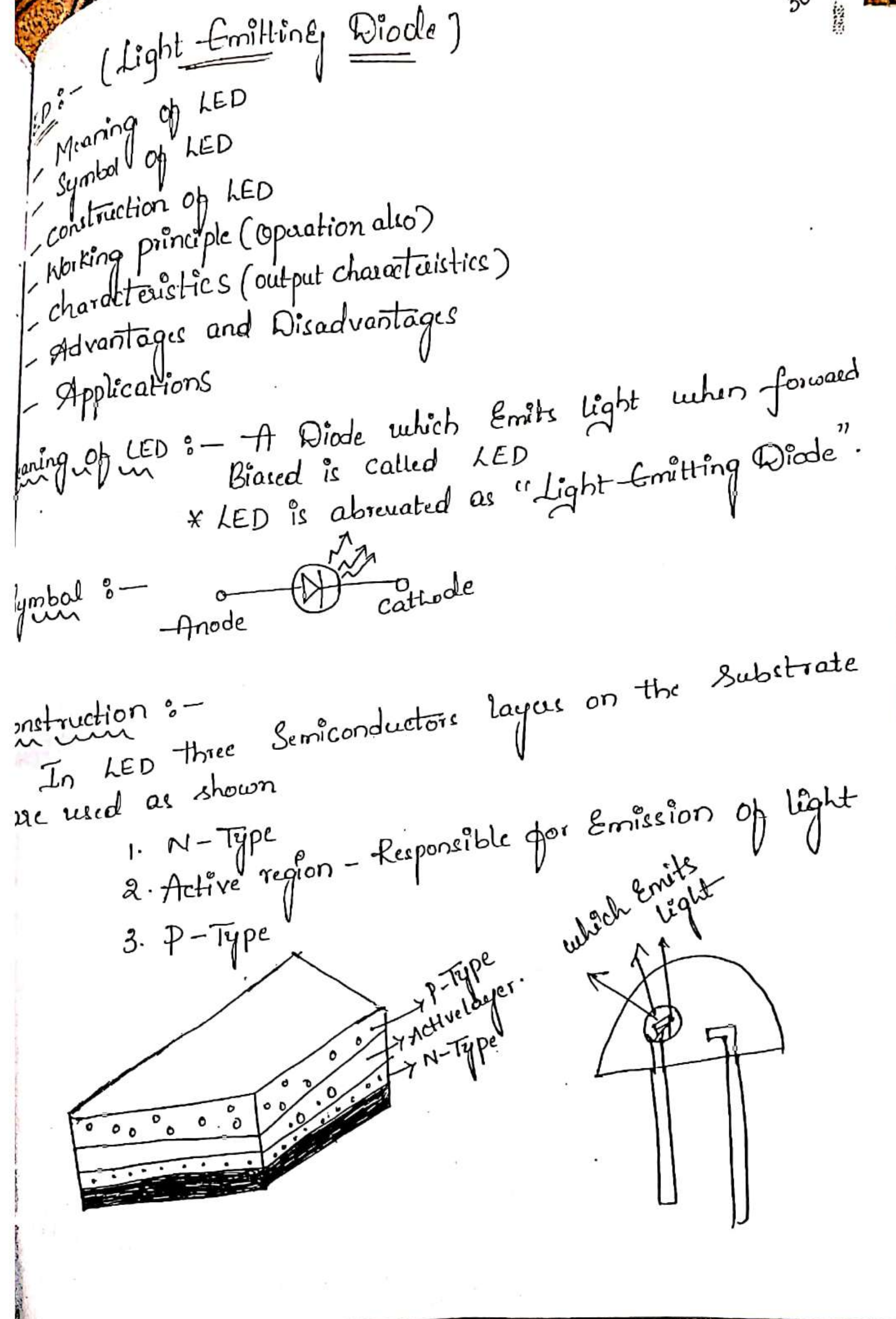
* This is the value of anode current below which SCR switches from ON state to OFF state.

Forward blocking Region:

* The region corresponds to OFF condition of SCR when anode is positive with respect to cathode.

Reverse breakdown Voltage:

* The reverse voltage at which the device breaks into the avalanche region is called "Reverse breakdown voltage".



30

LED :- (Light Emitting Diode)

- Meaning of LED
- Symbol of LED
- construction of LED
- Working principle (operation also)
- characteristics (output characteristics)
- Advantages and Disadvantages
- Applications

Meaning of LED :- A Diode which Emits light when forward Biased is called LED

* LED is abreuated as "Light Emitting Diode".

Symbol :-

Construction :-

In LED three Semiconductors layers on the Substrate are used as shown

1. N-Type
2. Active region - Responsible for Emission of light
3. P-Type

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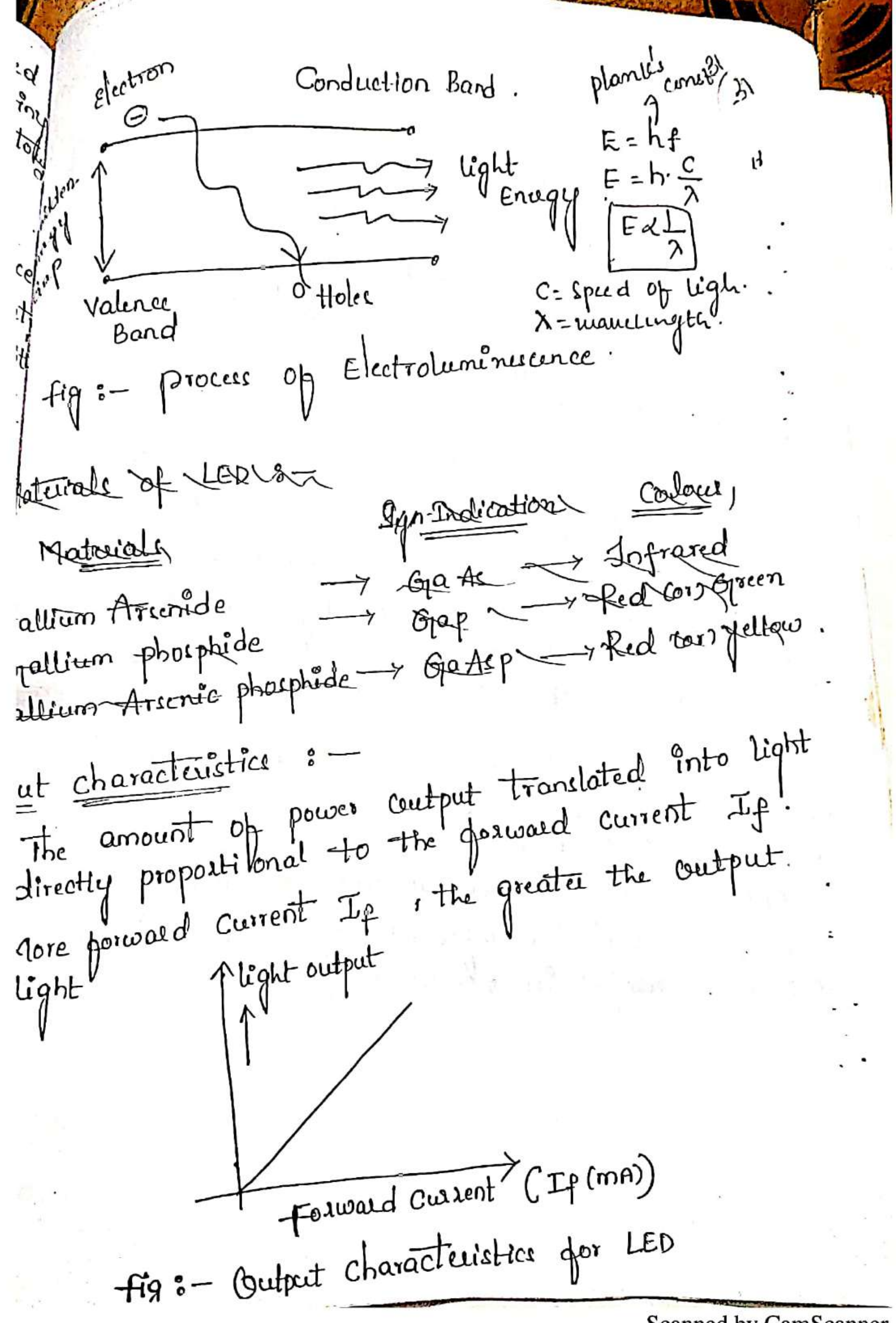
In LED Emits light all the way around the Layered Structure. This layered structure is placed in a [illegible] reflective Cup so that the light gets reflected [illegible] the desired Exit direction.

Working principle :-

* The LED Works on the principle of "Electroluminescence".
* When the p-N junction is forward biased, the electrons in n-region Cross the junction and recombine with Holes in n-region.
* practically when LED is forward biased, the holes from p-region and electrons from n-region Enter active region between p and n regions.
* In the active region recombination of Electrons and holes takes place and the Energy is released in the form of a light.
* The ~~Energy~~ Energy released depends on the forbidden gap - Energy which determines the wavelength and Colour of the Emitted light.
* "Electroluminesense" is an "Electrical phenomenon in which a material Emits light in responce to the passage of an Electric current".

Fig :- Forward-biased LED.



planck's const (h)

$E = hf$

$E = h \cdot \frac{c}{\lambda}$

$E \propto \frac{1}{\lambda}$

C = speed of ligh.
λ = wavelength.

fig :- process of Electroluminescence.

aterials of LED :-

Materials		Sym-Indication		Colour
allium Arsenide	→	GaAs	→	Infrared
Gallium phosphide	→	Gap	→	Red (or) Green
allium Arsenic phosphide	→	GaAsp	→	Red (or) yellow.

ut characteristics :—

The amount of power output translated into light directly proportional to the forward current If. More forward current If, the greater the output light.

fig :- Output characteristics for LED

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dvantages :-

LED's are Small in Size

The LED displays operated under different ambient lighting Conditions.

LED's are fast operating devices (ON/OFF in 1μs)

The LED's are light in weight

The LED's are available in Various colours

The LED's have long life

The LED's are cheap.

Disadvantages :-

* It requires frequent replacement of battery in low power / battery operated devices

Luminous Efficiency of LED is Low (1.5 lum/watt)

The characteristics are affected by Temperature.

Need large power for Operation Compared to normal P-N junction diode.

Applications :-

All kinds of Visual displays i.e Seven Segment displays such as Watches and calculators.

In the optical devices.

ON-OFF indicators in Various types of Electronic circuits.

Some LED's radiates Infrared light which is invisible such LED's useful in remote Control and burglar alarm.

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Manufacturing materials of LED :-

ing Ga As (Gallium Arsenide) — Infrared

Al Ga As (Aluminium Gallium Arsenide) — red.

Ga As, Ga P (Gallium phosphide) — red.

(Al Ga As)
(Ga P)
Al Ga In P)
} — Orange

Ga As P
Al Ga In P
Ga P
} — yellow

Green -

ps Ga In P
Al Ga In P
} — Green

Zn S
Zinc selenide)
b) In Ga N
} — Blue

Indium Gallium Nitrade.

In Ga N — Violate

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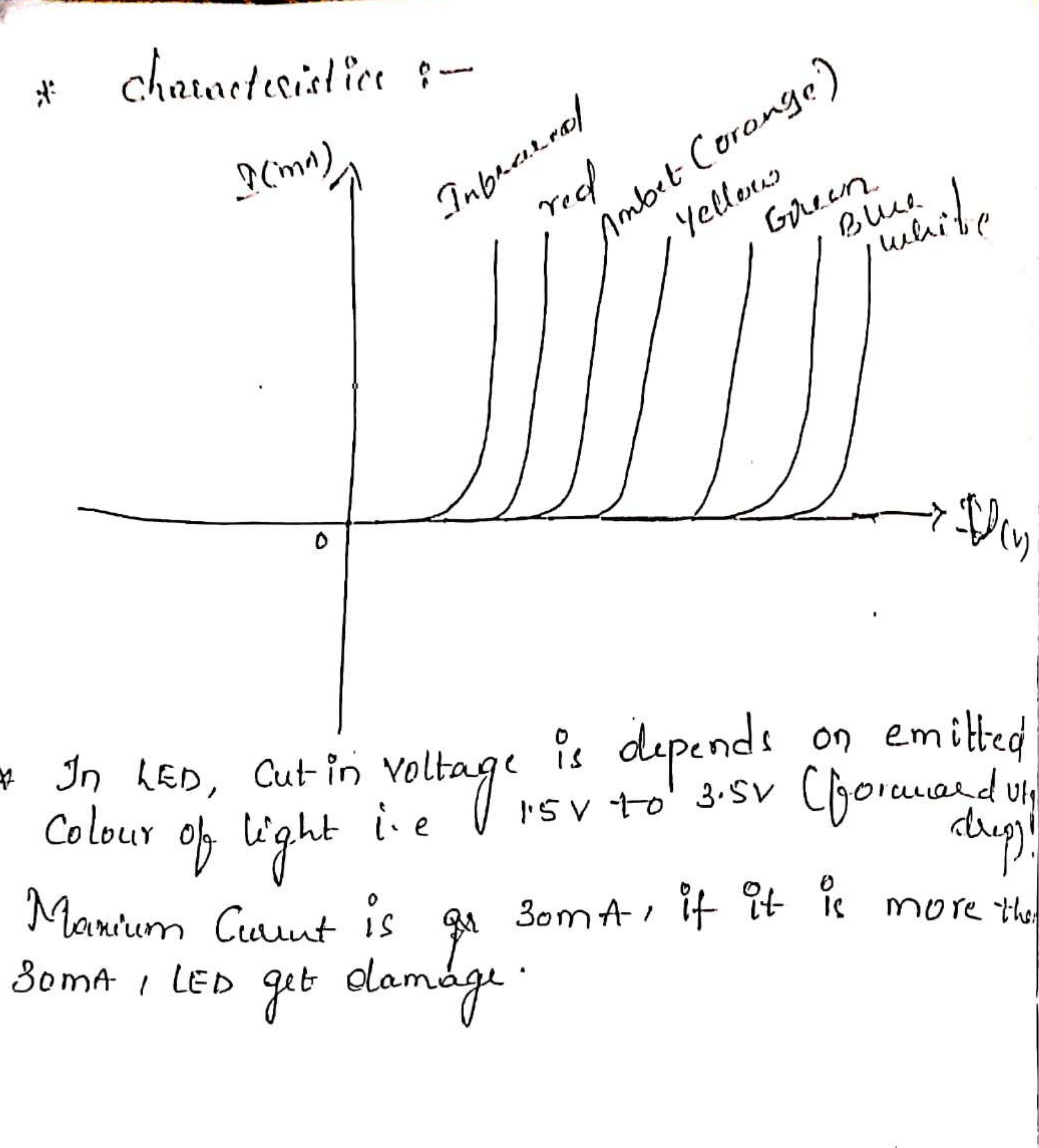
* characteristics :-



* In LED, cut-in voltage is depends on emitted colour of light i.e 1.5V to 3.5V (forward V/g drop).

: Maxium Current is 30mA, if it is more than 30mA, LED get damage.

Liquid Crystal Display [LCD]

- Introduction
- Arrangement of rods
- Types of LCD
- Advantages
- DisAdvantages
- Applications

Introduction :

The liquid crystal are one of the most fascinating material system in nature. having properties of liquid as well as of a solid crystal. The terms liquid crystal refers to the fact that these compounds have crystalline arrangement of molecules, Yet they flow like a liquid. liquid crystal display do not emit or generate light, but rather alter Externally generated illumination. Their ability to modulate light when Electrical signal is applied has made them very useful in flat panel display technology

→ The different Arrangement of these rod like molecules lead to three main categories of liquid crystals

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→ smetic

→ Nematic

→ cholesteric

Smetic :-

In this structure the rod like molecules are arranged in layers, and within each layer there is orientational order over a long range. Thus, in a given layer, the rods are all oriented in the same direction. Also, in the smetic liquid crystals the molecules of different layers are ordered as shown in figure. Thus, both orientation order and positional order is present in the smetic crystals.

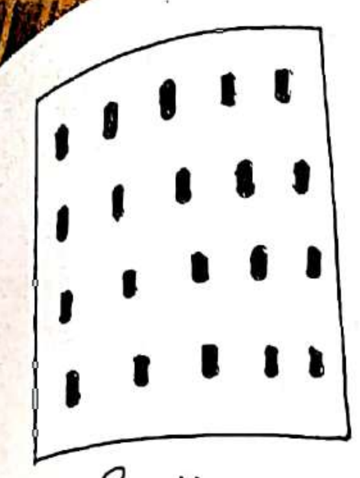
Nematic :-

In the Nematic structure the positional order between layer of molecules is lost, the orientation order is maintained.

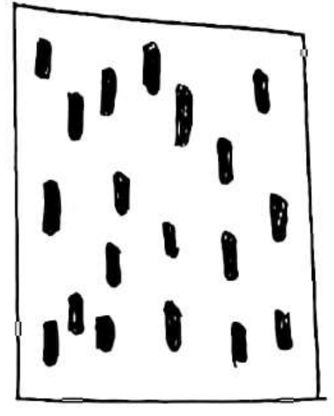
cholesteric :-

In these crystals the rod like molecules in each layer are oriented in a different angle within each layer orientation order is maintained in each layer. The cholestric liquid crystal is related to the nematic crystal, with the difference being the twist of the molecules as one goes from one layer to another.

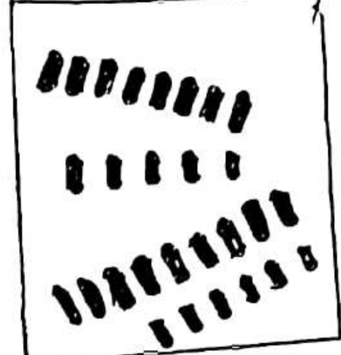
There are



(a) Smetic



(b) Nematic



(c) Cholestric

there are two types of liquid crystal displays according the theory of operation :

1. Dynamic scattering LCD
2. Field Effect LCD

Dynamic scattering LCDS :-

It shows the construction of a typical liquid crystal ell. It consists of a layer of liquid crystal material andwiched between glass sheets with transparent metal ilm Electrodes. usually, an optically thin (about 50 nm) ayer of Indium Tin oxide (ITO) on each surface acts s an Electrode to allow a voltage to be held across the ell. The aligning treatment is then applied on the top f ITO.

when the cell is not activated, the liquid crystal transparent. when it is activated the molecular urbulence causes the light to be scattered in all irections so that the activated areas appear bright. his phenomenon is known as <u>dynamic scattering</u>.

With both glass sheets transparent, the cell is known as a transmittive type cell.

Glass

Indium tin oxide as electrode.

Liquid Crystal Material

layer of aligning Material

Glass

When only one glass plate sheet is transparent and other has a reflective coating, the cell is termed reflective type.

Transmittive Type cell :-

When not activated, cell will simply transmit rear Edge lighting through the cell in straight lines. In this condition the cell will not appear bright. When the cell is activated the incident light scatters and cell appears quite bright.

Transmitted light

Unactivated liquid crystal cell

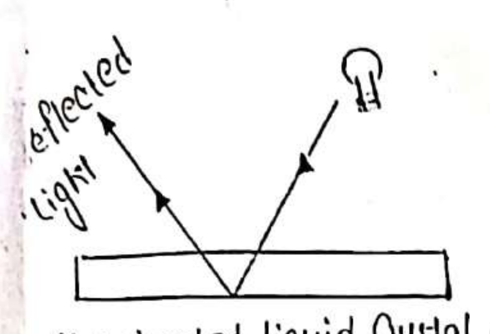
Scattered light.

Activated cell

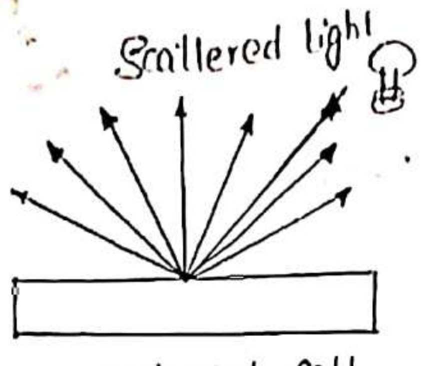
Reflective type cell :-

The reflective type cell operates from light incident on its front surface. When it is not activated, light is reflected in the usual way from the mirror surface, and the cell does not ... When it is activated the dynamic

scattering occurs and cell appears bright.



Unactivated liquid crystal cell



-Activated cell

Field Effect LCD:

and It shows the field effect liquid crystal cell. It consist of two glass plates, a liquid crystal fluid, polarizers and transparent conductors. The liquid crystal fluid is sandwiched between two glass plates. Each glass plate is associated with light polarizer. The this light polarizers are placed at right angle to each other. cell In the absence of electrical excitation, the light coming pears through the front polarizer is rotated through 90° in the fluid and passed through the rear polarizer. It is then reflected to the viewer by the back mirror is shown in figure.

On the Application of Electrostatic field, the liquid ght. crystal fluid molecules get aligned and therefore light through the molecules is not rotated by 90° & it is absorbed by the rear polarizer as shown not in figure. This causes the appearance of dark light on a light background.

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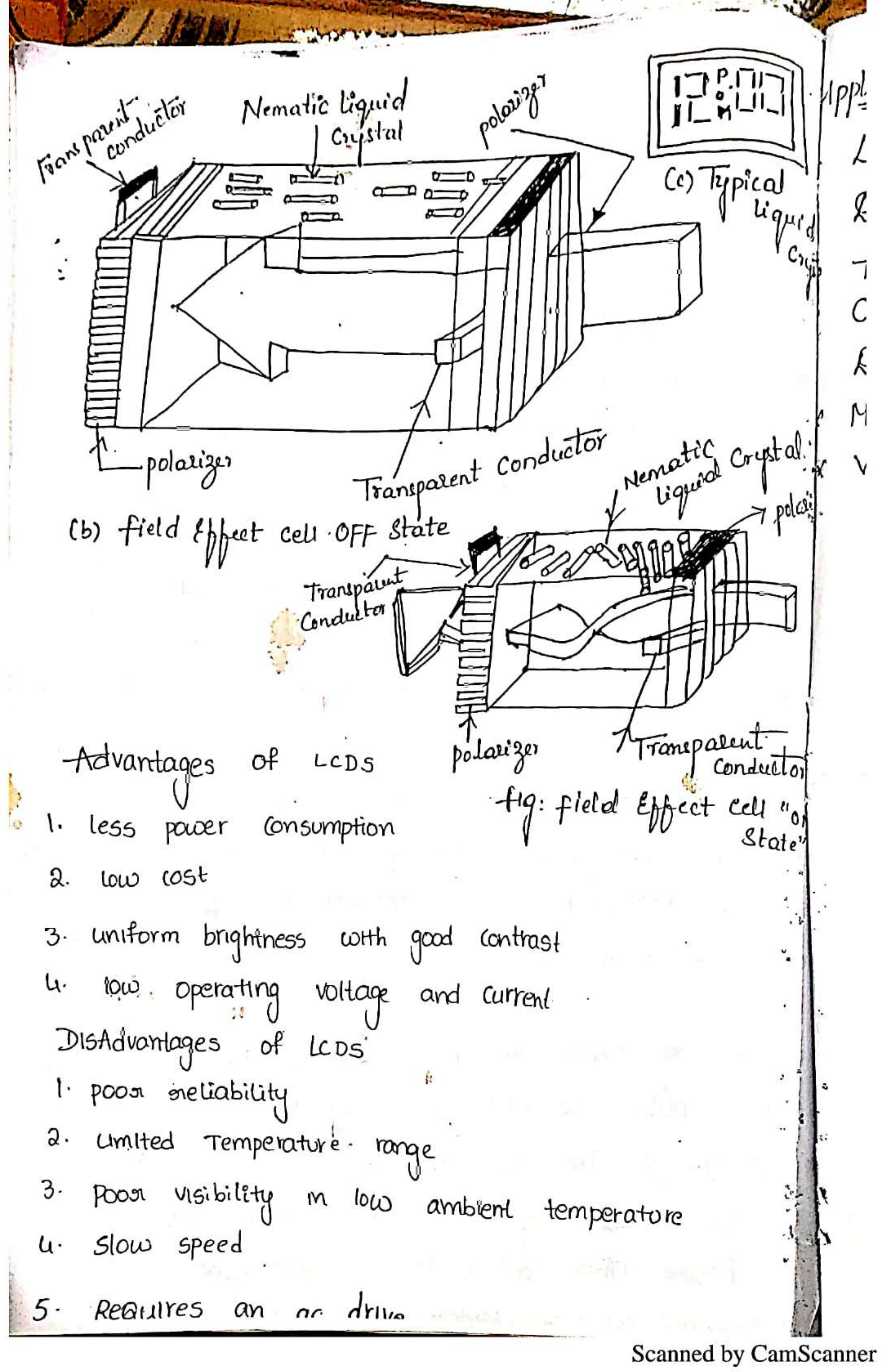

Advantages of LCDS

1. less power consumption
2. low cost
3. uniform brightness with good contrast
4. low operating voltage and current

DisAdvantages of LCDS

1. poor reliability
2. Limited Temperature range
3. Poor visibility in low ambient temperature
4. Slow speed
5. Requires an ac drive

Applications :—

- LCD's are used in Display Screen In calculations
- Digital Cameras
- TV's
- Computer monitor
- Digital wrist watches
- Mobile Screens
- Video players Etc.

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III (A) TRANSISTOR CHARACTERISTICS

UNIT - III - A
[BJT]

INTRODUCTION:

* Transistors are Solid-State devices used for amplifying Controlling and generating electrical Signals. They are used widely in electronic equipments such as pocket Calculators, radios and also in Communication Satellites.

* In 1947, John Bardeen, Walter Brattin were the first to invent the "transistor" by adding another junction to a p-n junction diode which could control the flow of majority Charge Carriers. Later in 1951 william Shockley made the modern version i.e., Junction transistor. It is one of the greatest inventions of the 20th Century.

* The following are the advantages of Transistors.

1. Low operating Voltage.
2. Higher efficiency.
3. Small Size.
4. Does not Require any filament power.

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TRANSISTOR:

Definition:- A transistor is a semiconductor device that regulates current or voltage flow used to switch or amplify the electronic signals.

* Transistor is nothing but transfer of Resistance. As it transfers the resistance from one region to other region.

* Transistor is a three terminal device, they are

1. Emitter
2. Base
3. Collector.

* TRANS-ISTOR

↓ transfer property

↳ means resistance property offered to the junctions.

EMITTER:

* The terminal of the transistor which supplies or emits the charge carriers is called "Emitter" terminal.

* It is Heavily doped and moderate in size.

* It is always in forward bias with respect to base in order to supply charge carriers.

* Because of Heavy doping it can supply large amount of charge carriers.

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BASE:

* The terminal which lies in between Emitter and Collector is called Base terminal of the transistor.

* It is lightly doped and very thin in size.

* The charge carriers emitted by the emitter passes through the base.

* To reduce the recombination of charge carriers it is lightly doped.

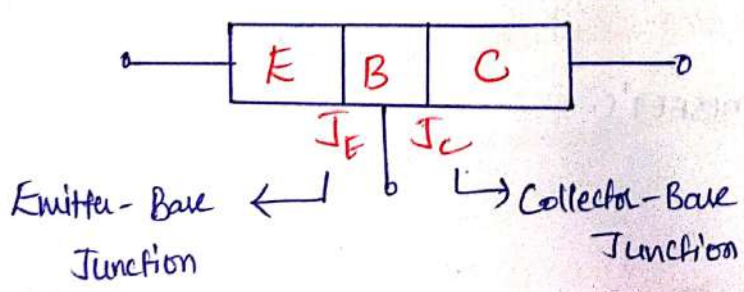
COLLECTOR:

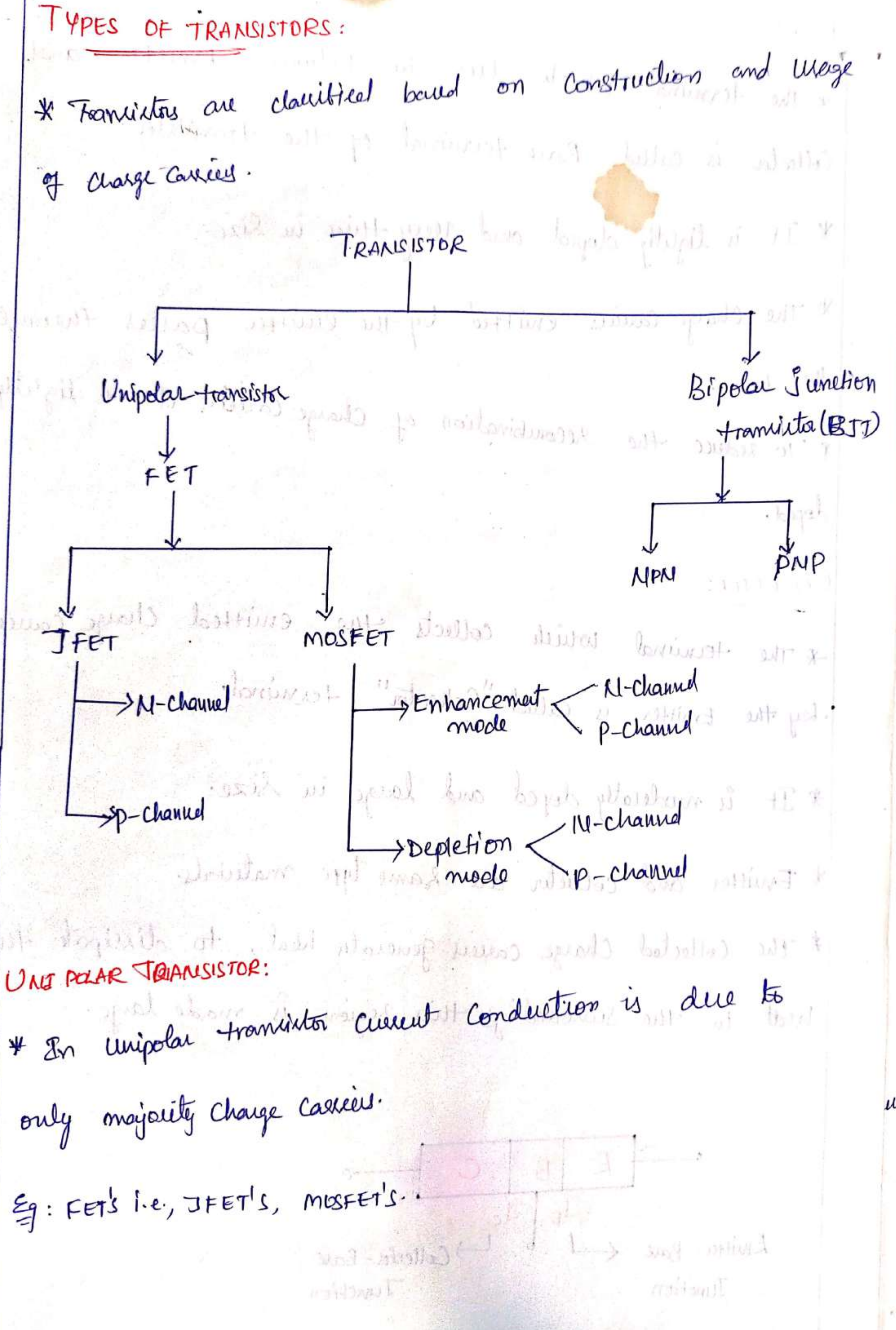
* The terminal which collects the emitted charge carriers by the Emitter is called "Collector" terminal.

* It is moderately doped and large in size.

* Emitter and collector are same type materials.

* The collected charge carriers generates heat, to dissipate this heat to the surroundings this region is made large.





TYPES OF TRANSISTORS:

* Transistors are classified based on construction and usage of charge carriers.

UNIPOLAR TRANSISTOR:

* In unipolar transistor current conduction is due to only majority charge carriers.

Eg: FET's i.e., JFET's, MOSFET's.

BIPOLAR JUNCTION TRANSISTOR:

* In Bipolar junction transistor (BJT's) current conduction is due to both majority and minority charge carriers.

* BJT is a current-controlled device because its output characteristics ~~depends on the~~ are determined by the input current.

Definition: A Bipolar junction transistor is a three terminal semiconductor device consisting of two P-N junctions which is able to amplify or magnify a signal.

* BJT is analogous to the vaccum triode and is comparitively small in size. It is used in amplifier and oscillator circuits and as a switch in digital circuits.

* Based on the construction it is classified into two types
    1. N-P-N Transistor,
    2. P-N-P Transistor.

NPN Transistor:

Definition: A thin layer of p-type material is sandwiched between two layers of N-type material then it is called as a NPN transistor.

* It is made up of silicon or germanium crystal.

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SYMBOL:

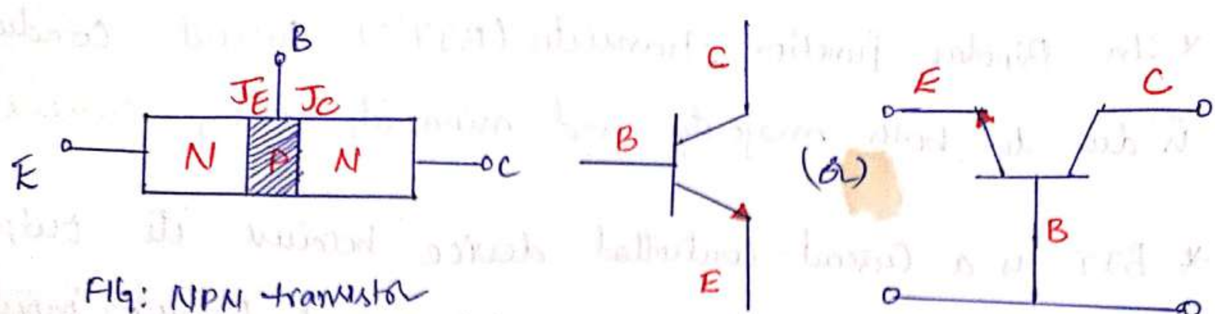


FIG: SYMBOL OF NPN TRANSISTOR.

* The arrow in the symbol indicates the direction of current flow when the Emitter-Base junction is forward biased.

PNP TRANSISTOR:

Definition: A thin layer of N-type material is sandwiched between two layers of P-type material then such type of transistor is called PNP transistor.

SYMBOL:

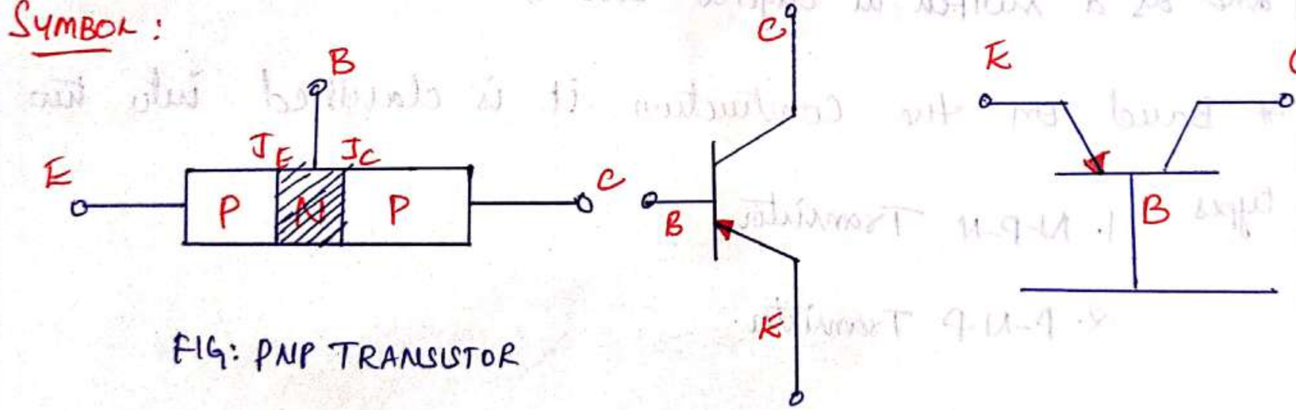
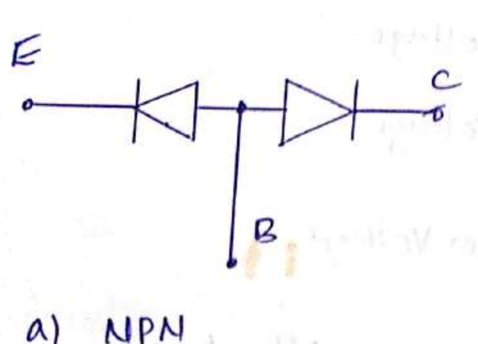


FIG: SYMBOL OF PNP TRANSISTOR.

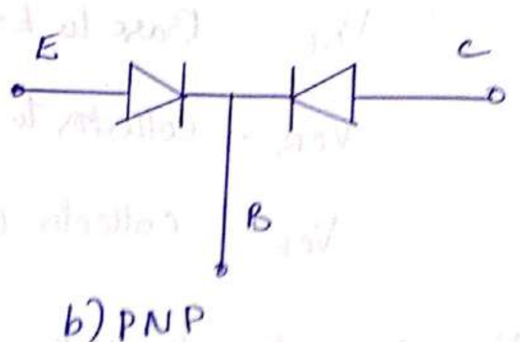
DIODE-EQUIVALENT REPRESENTATION OF NPN & PNP TRANSISTORS:

* A transistor looks like two PN junction diodes connected back to back.

* It has two PN junctions.



a) NPN



b) PNP

1. A junction between Emitter and Base is called as Emitter to Base junction (EB) or V_{BE} or Simply "Emitter junction."

2. A junction between Collector and Base is called as Collector to Base junction or V_{BC} or "Collector junction".

CIRCUIT REPRESENTATION

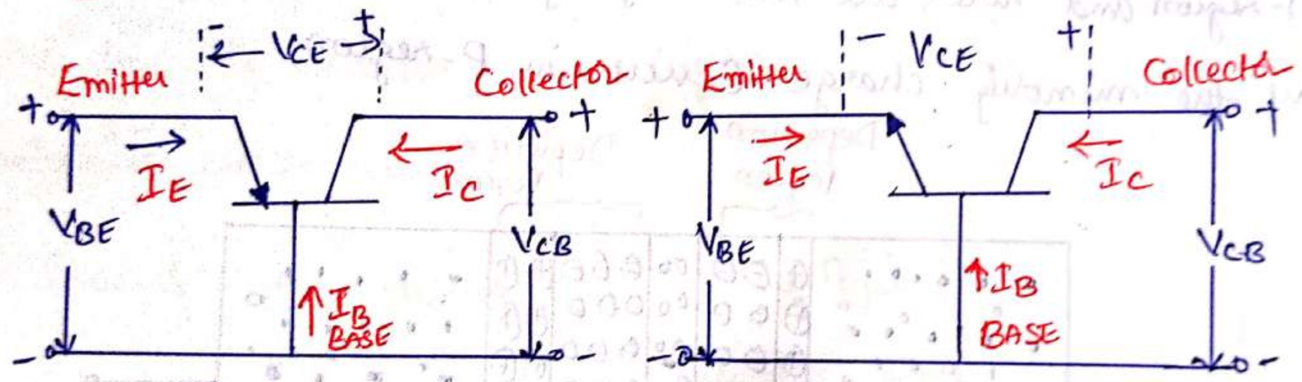


Fig: Circuit Representation of PNP & NPN Transistors

* The arrow on the Emitter lead specifies the direction of current flow when the Emitter-Base junction is forward biased.

I_E - Emitter current

I_B - Base current

I_C - Collector current.

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V_{BE} - Base to Emitter Voltage

V_{CB} - Collector to Base Voltage

V_{CE} - Collector to Emitter Voltage.

* V_{EB} represents the voltage drop from emitter to base.

UNBIASED TRANSISTOR:

* When External Voltage is not applied to the transistor then it is called Unbiased transistor.

* In NPN transistor, free electrons are the majority charge carriers and holes are the minority charge carriers in n-region and holes are the majority charge carriers and electrons are the minority charge carriers in p-region.

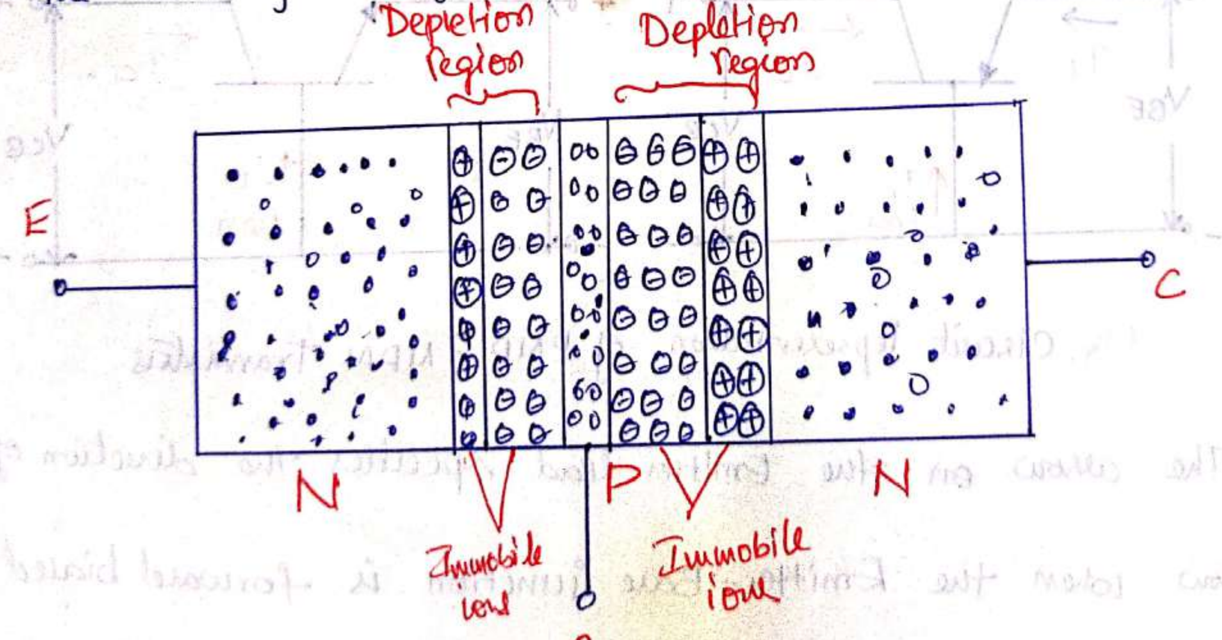


FIG: UNBIASED NPN TRANSISTOR.

* Transistor is like a p-N junction diodes Connected front to front (or) back to back.

* So two junctions are formed, they are Emitter junction and Collector junction.

* The junction between Emitter and base is called as "Emitter to base junction" or Input junction (or) Emitter junction.

* The junction between Collector and base is called as "Collector to base junction" (or) Collector junction (or) "output junction"

* At room temperature, the electrons in n-type (i.e., emitter region) move towards the base region and combine with the holes in base region and thus forms the depletion region ~~between~~ at emitter base junction.

* Similarly, the electrons in collector region move towards the base region and combine with the holes in base region thus depletion region is formed at Collector base junction.

* The depletion region is more towards the base region than the emitter and collector regions as shown in figure.

* This is because of heavy doping in Emitter and Collector regions than the base regions.

BIASING OF TRANSISTORS (&) OPERATING MODES OF TRANSISTOR:

* Transistor is operated in three modes depending on biasing voltage.

* In order to operate transistor properly as an Amplifier, it is necessary to correctly bias the two p-n junctions with external voltages.

* Depending on external bias voltage, polarities used, the transistor works in one of the three regions.

REGION	Emitter-Base Junction	Collector-Base Junction
Active	Forward biased	Reverse biased
Cut-off	Reverse biased	Reverse biased
Saturation	Forward biased	Forward biased

1. ACTIVE REGION:

* The region in which transistor, Emitter to base junction is forward biased (V_{BE}) and Collector to base junction (V_{CB}) is Reverse biased then that region is called Active Region.

* In Active Region transistor acts as "Amplifier".

E N P N C

B

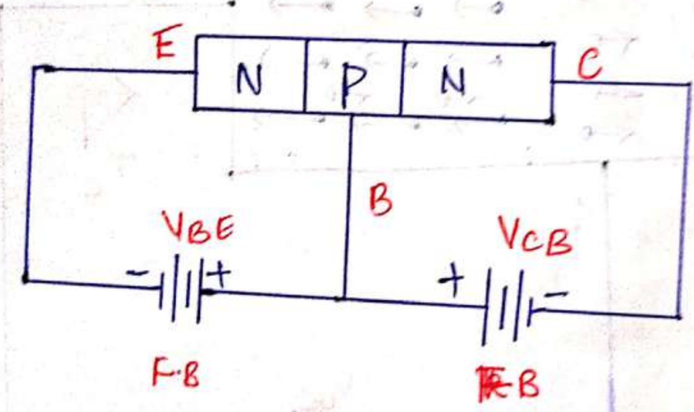
V_{BE} V_{CB}

F.B R.B

2. Saturation Region:

* The Region in which transistor, both emitter to base junction and Collector to base junction are forward bias that region is called "Saturation Region".

* In Saturation region transistor acts as "ON" Switch.



3. Cut-off Region:

* The Region in which transistor, both emitter to base junction and Collector to base junctions are reverse biased, that region is called "Cut-off Region".

* In Cut-off region transistor acts as "OFF" Switch.

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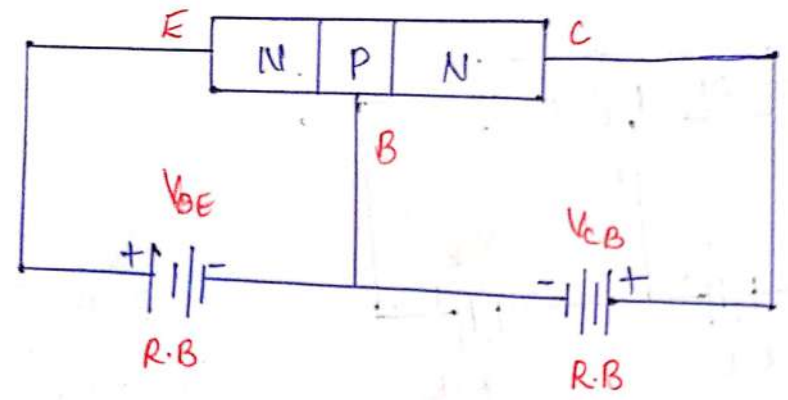

OPERATION OF AN NPN TRANSISTOR:

* NPN transistor with base to emitter junction in forward bias and Collector to emitter junction is reverse bias as shown below.

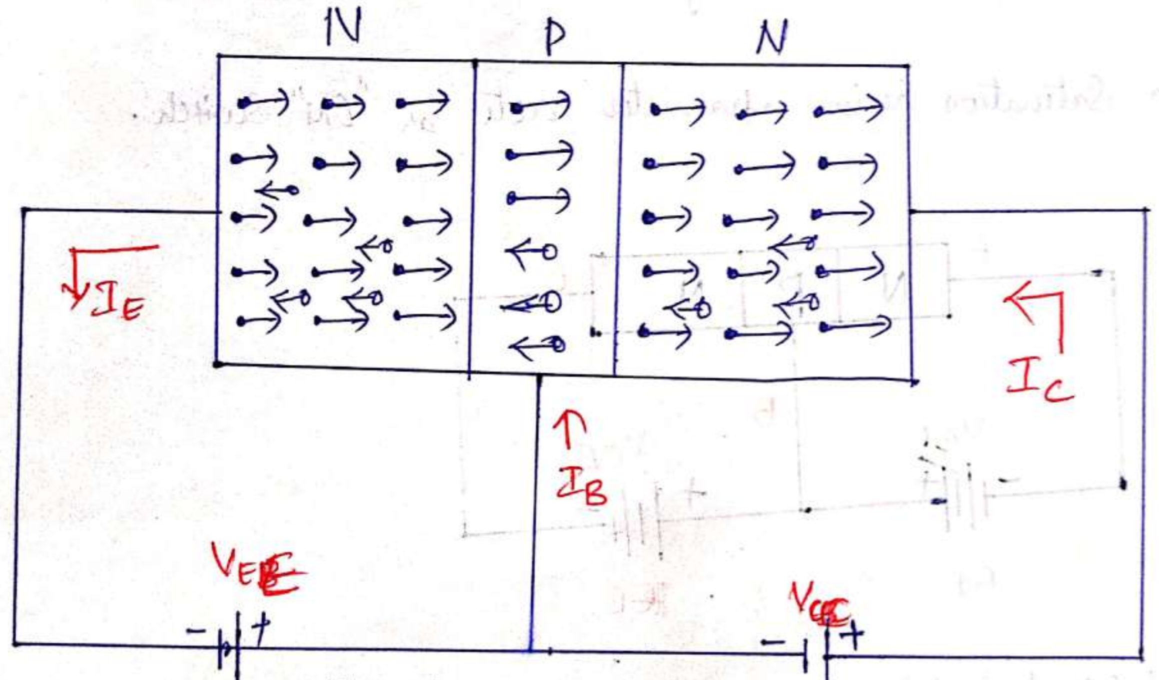

FIG: CURRENT IN NPN TRANSISTOR.

* The forward bias applied to the Emitter-base junction of an NPN transistor Causes a lot of electrons from the emitter region to cross over to the base region.

* So, the majority carriers electrons in n-type flow towards the base and constitutes "Emitter Current" (I_E).

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* The base is lightly doped with p-type material, the number of holes in the p-region is very small and hence, the number of electrons that combine with holes in the p-type region is also very small.

* Hence, a few electrons combine with holes to constitute a "Base Current" (I_B). i.e., only 2% will combine with holes in the base region.

* The remaining electrons (more than 95%) cross over into the collector region.

* Hence, these electrons constitute the "Collector Current" I_C.

* So, the electrons which are emitted by the Emitter, some combine with holes in p-region gives base current and remaining electrons reaches collector and constitutes collector current.

* Thus, Emitter current is the sum of base current and collector current.

$$I_E = I_B + I_C$$

where $I_E \rightarrow$ Emitter Current

$I_B \rightarrow$ Base Current

$I_C \rightarrow$ Collector Current

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OPERATION OF PNP TRANSISTOR:

* In PNP transistor, base to emitter junction is forward bias and Collector to base junction is reverse biased.

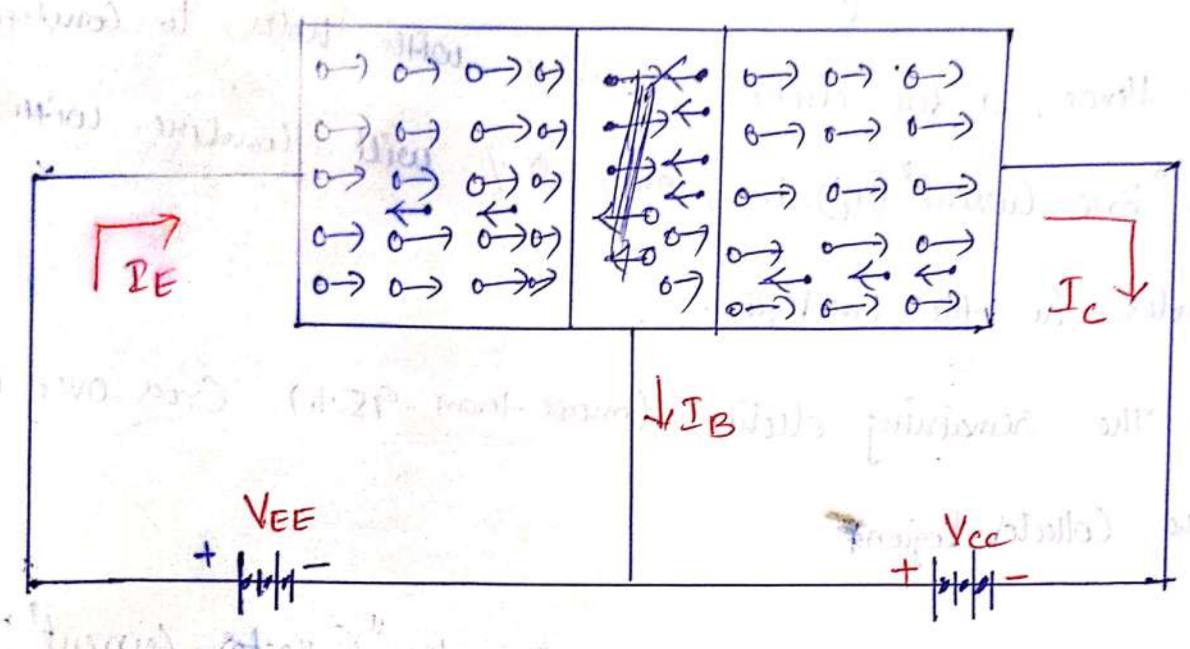


FIG: CURRENT IN PNP TRANSISTOR

* The forward bias applied to the Emitter-base junction of an PNP transistor causes a lot of holes from the emitter region to cross over to the base region.

* So, the majority carriers holes in p-type flow towards the base and constitutes "Emitter Current" (I_E).

* The base is lightly doped with n-type material, the number of electrons in n-region is very small, and hence the number of holes that combine with electrons also small in n-region.

* Hence, a few holes combine with electrons to constitute a "Base Current" i.e., only 5% will combine with electrons in n-region

* The remaining holes (more than 95%) cross over into the collector region.

* Hence, these holes constitute the "collector current" I_C.

* So, the holes which are emitted by the Emitter, some of them combined with the electrons in base region, which gives base current and remaining holes reaches collector and constitutes collector current.

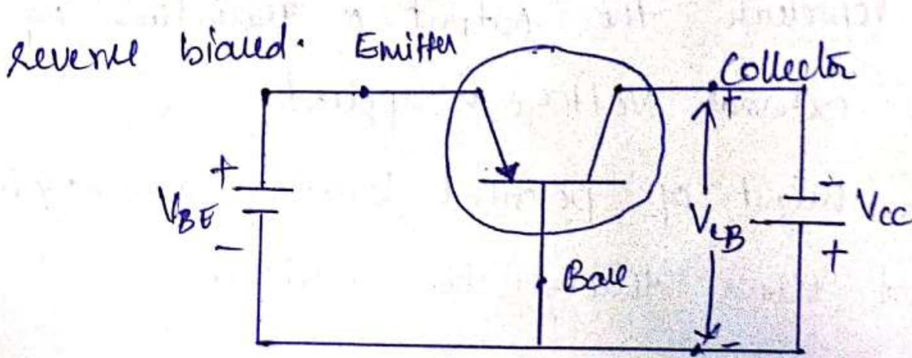
* Thus, Emitter current is sum of base current and collector current.

$$I_E = I_B + I_C$$

where I_E is Emitter current
I_B is Base current
I_C is collector current.

POTENTIAL DISTRIBUTION THROUGH A TRANSISTOR.

* Consider a p-n-p transistor with emitter to base junction is forward biased and collector to base junction is reverse biased.



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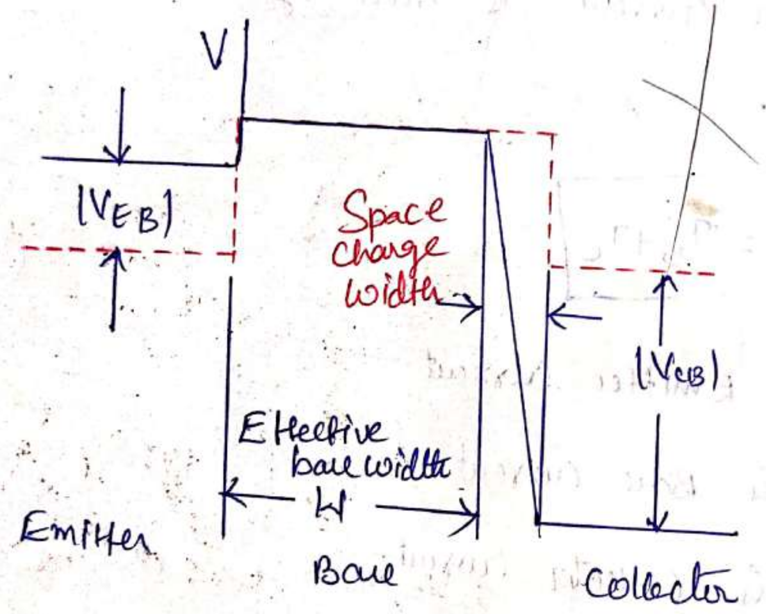
* Fig(b) represents the variation of potential when no voltage is applied across the transistor (unbiased).

V
V_0
Emitter Base Collector

V
V_0
Emitter Base Collector

fig(b): Variation of potential for unbiased transistor

* The potential variation of biased transistor is as follows.



Fig(c) potential variation of biased PNP transistor

* In fig(c) dashed curve represents the case before the external voltage is applied.

* The solid curve represents the output or variation of potential when the external voltage is applied.

* "V_0" represents the height of potential barrier (may be of few volts) so that no current flows through the junction.

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* If the emitter is open-circuited so that $I_E = 0$, then I_{pc} would be zero. Under these circumstances the base and collector would act as a reverse biased diode, the reverse saturation current I_{co} flows.

where $$\boxed{I_{co} = I_{nco} + I_{pco}} \rightarrow (2)$$

where I_{co} - Reverse Saturation Current

$I_{pco} \rightarrow$ Current caused by the holes moving from p-region to n-region.

$I_{nco} \rightarrow$ Current caused by the electrons moving from n-region to p-region.

In general, it is represented as, $I_c = I_{nc} + I_{pc}$

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PARAMETERS OF CURRENT COMPONENTS:

1. EMITTER EFFICIENCY (γ):

Definition: The Ratio of current of injected carriers at Emitter - base junction (J_E) to the total emitter current is defined as the "Emitter efficiency" (γ).

$$\text{Emitter Efficiency } \gamma = \frac{\text{Current of injected Carriers at } J_E}{\text{Total Emitter Current}}$$

In Case of p-n-p transistor

$$\gamma = \frac{I_{PE}}{I_{PE} + I_{nE}}$$

where $I_E = I_{PE} + I_{nE}$

$$\boxed{\gamma = \frac{I_{PE}}{I_E}}$$

where I_{PE} is Injected hole diffusion current at emitter junction

I_{nE} is Injected electron diffusion current at emitter Junction.

2. TRANSPORT FACTOR (β^*) :

Definition: The Ratio of injected carrier current reaching at collector junction J_C to the injected carrier current at emitter base junction J_E.

$$\beta^* = \frac{\text{Injected carrier current at } J_C}{\text{Injected carrier current at } J_E}$$

In case of p-n-p transistor

$$\boxed{\beta^* = \frac{I_{pC}}{I_{pE}}}$$

3. LARGE SIGNAL CURRENT GAIN (α):

Definition: The ratio of current due to injected carriers I_{pC} to the total emitter current I_E.

$$\alpha = -\frac{(I_C - I_{CO})}{I_E}$$

where $I_C = I_{CO} - I_{PC}$

$$I_{PC} = I_{CO} - I_C$$

$$\boxed{\alpha = \frac{I_{pC}}{I_E}} \longrightarrow (1)$$

* α ranges from 0.90 to 0.995 and it is positive.

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dividing eq (1) both neumerator and denominator by I_{PE}

$$\alpha = \frac{I_{PC}}{I_{PE}} * \frac{I_{PE}}{I_E}$$

$$\alpha = \beta^* * \gamma \qquad \left(\because \beta^* = \frac{I_{PC}}{I_{PE}} \text{ \& } \gamma = \frac{I_{PE}}{I_E}\right)$$

∴ The relation between α, β & γ is given by,

$$\boxed{\alpha = \beta^* \gamma}$$

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TYPES OF TRANSISTOR AMPLIFIER CONFIGURATIONS:

* When a transistor is to be connected in a circuit, one terminal is used as an Input terminal, the other terminal is used as an output terminal and the third terminal is common to both the input and output terminals.

* Depending upon the input, and output and common terminal a transistor amplifier can be connected in three configurations

* They are 1) Common Base (CB) Configuration
  2) Common Emitter (CE) Configuration
  3) Common Collector (CC) Configuration

* Transistor acts as Amplifier in Active mode.

1. COMMON BASE (CB) CONFIGURATION:

Definition: The Configuration in which emitter acts as Input terminal, Collector as the output terminal and base terminal is Common for both input and output terminals then such Configuration is said to be Common Base (CB) Configuration.

* Common Base Configuration is also called as "Grounded Base Configuration".

*

CIRCUIT DIAGRAM :

* Transistor works as an Amplifier in its Active mode of operation.

* So, while representing amplifier configurations the Emitter junction must be forward biased and Collector junction must be Reverse biased.

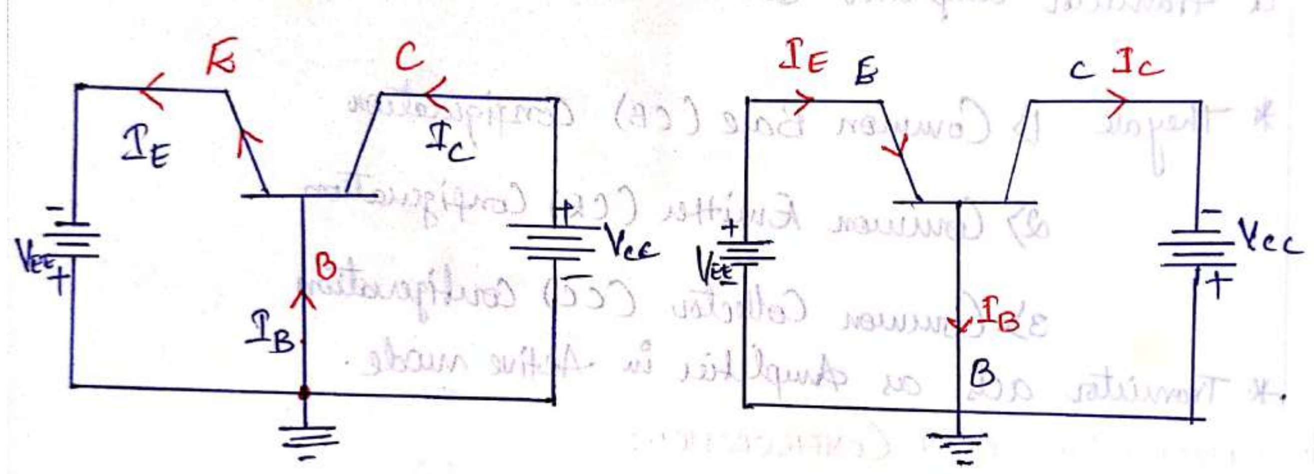

FIG: CB CONFIGURATION FOR NPN TRANSISTOR

FIG: CB CONFIGURATION FOR PNP TRANSISTOR

* The fundamental relation between Emitter, base and Collector Currents is given by

$$I_E = I_B + I_C$$

* According to transistor equation

$$I_C = -\alpha I_E + I_{CBO}\left(1 - e^{V_C/V_T}\right)$$

where I_{CBO} is the reverse saturation current flowing in CB Configuration

∵ I_{CBO} is very much less than the emitter current.

$$I_{CBO} << I_E$$

$$I_C = -\alpha I_E$$

$$\alpha = -\frac{I_C}{I_E}$$

where α values ranges from 0.95 to 0.98 which is +ve.

CURRENT AMPLIFICATION FACTOR:

Definition : The Ratio of change in output current to the change in Input current is known as the Current Amplification factor.

$$\alpha = \frac{\Delta I_C}{\Delta I_E}$$

CIRCUIT DIAGRAM TO DETERMINE STATIC CHARACTERISTICS:

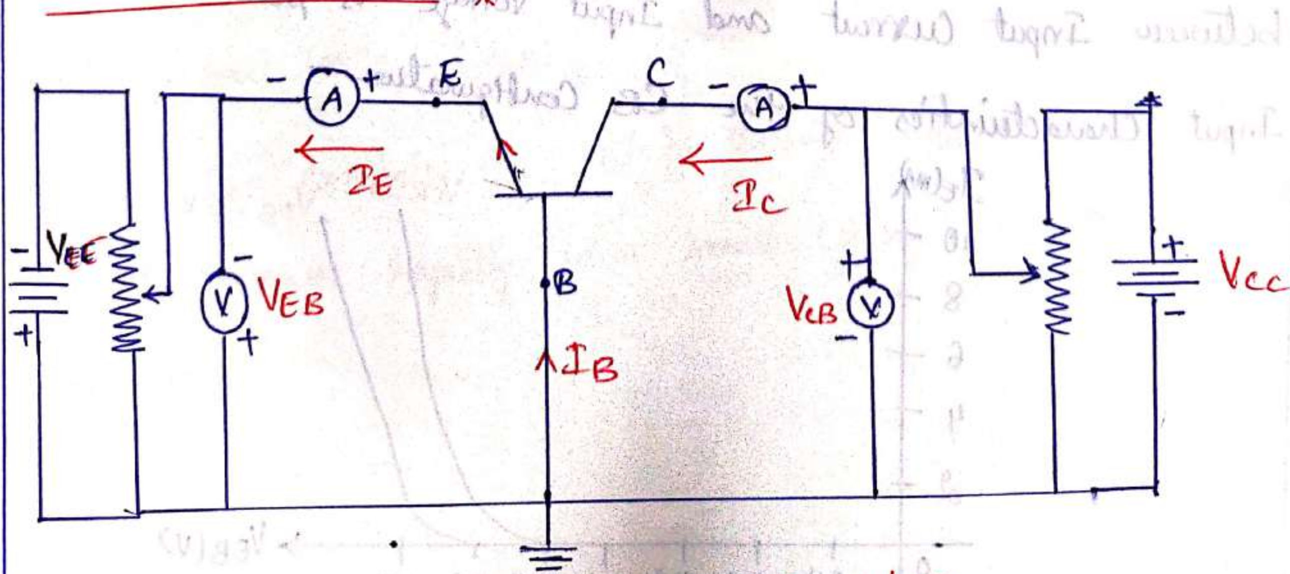

FIG : CIRCUIT DIAGRAM OF NPN Transistor in CB CONFIGURATION

* The working of CB configuration can be explained with the help of Static Characteristic Curves.

INPUT CHARACTERISTICS:

Definition: The graphical representation of Input currents to the I/p voltages i.e (V-I Characteristics)

* In CB Configuration, INPUT terminal - Emitter

  Common terminal - Base

  OUTPUT terminal - Collector

* Input current - I_E

  Input Voltage - V_{EB}

  Output current - I_C

  Output Voltage - V_{CB}

Definition: The Graphical representation which explains the relation between Input current and Input voltage is said to be Input characteristics of the CB Configuration.

FIG: CB INPUT CHARACTERISTICS

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* To determine the Input Characteristics,

1. The Collector to Base Voltage (V_{CB}) is kept constant at 0V.

2. The Emitter Current I_E is increased by increasing the Emitter to base Voltage (V_{EB}) in suitable steps.

3. This is repeated for higher values of V_{CB}.

4. A curve is drawn between Emitter current I_E and Emitter - base Voltage (V_{EB}) at constant collector to base voltage (V_{CB}).

* CASE : 1 When $V_{CB} = 0V$

* When Collector to base voltage is zero volts and the Emitter-Base junction is ~~reverse~~ forward biased, the Emitter junction (J_E) behaves as a forward biased PN diode.

* So, Emitter current I_E increases rapidly with small increase in Emitter-Base voltage (V_{EB}).

* When V_{EB} exceeds the cut-in voltage then the emitter current increases rapidly for a small change in emitter to base voltage (V_{EB}).

Case:2 When $V_{CB} > 1V$

* When collector-base voltage is increased more from zero volts by keeping V_{EB} constant.

* The curve shifted towards left as shown in the input characteristics when V_{CB} is increased.

* This effect is due to the decrease in width of the base region, because of this I_E also increases.

* This effect is called Early effect or Base width modulation.

OUTPUT CHARACTERISTICS:

Definition: The Graphical representation which explains the relation between output current I_C and output voltage V_{CB} is said to be output characteristics of CB configuration.

* In CB configuration, output current I_C
Output voltage V_{CB}.

* To determine output characteristics,

1) The Emitter current I_E is kept constant at a suitable value by adjusting the emitter-base voltage V_{EB}.

2) Then collector to base voltage V_{CB} is increased in suitable steps and the collector current I_C is noted.

3) This is repeated for different fixed values of I_E.

4) Now the curves of I_C Vs V_{CB} are plotted for constant values of I_E.

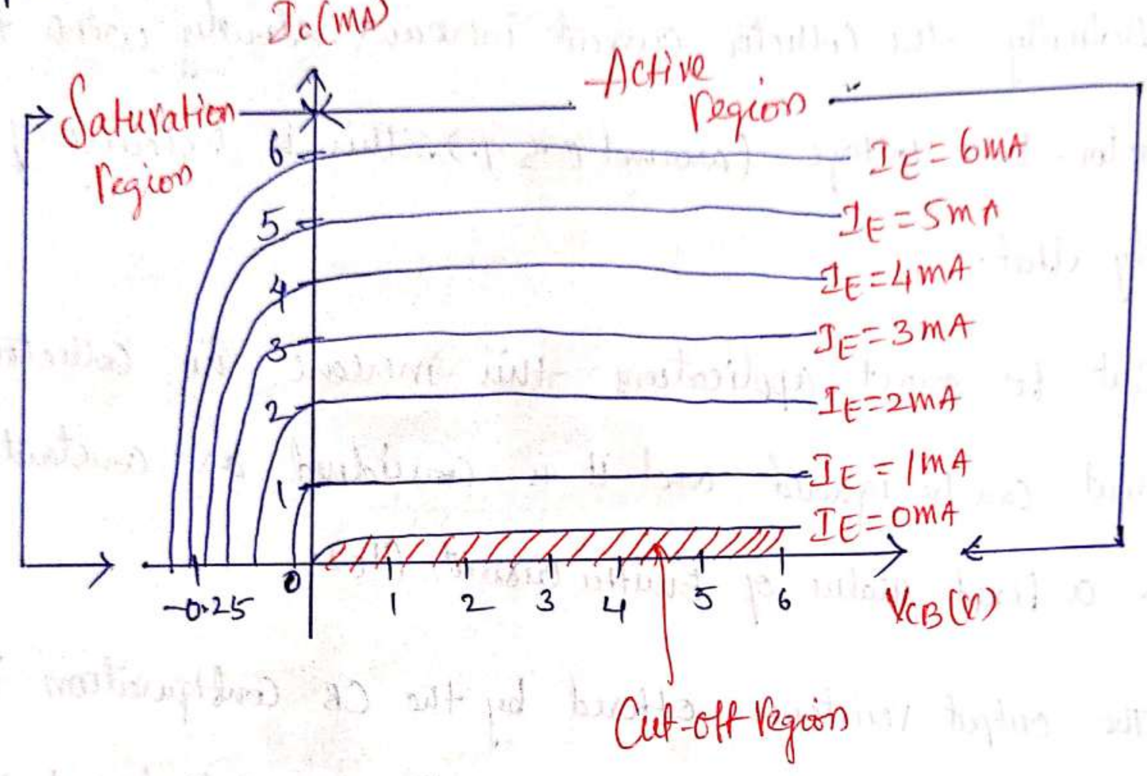

FIG: CB OUTPUT CHARACTERISTICS

* The output characteristics can be divided into three regions
  1. Active Region
  2. Cut-off Region
  3. Saturation Region.

ACTIVE REGION:

* In active region, the collector-base junction is reverse biased and Emitter-base junction is forward biased.
* The collector current (I_C) is almost independent of the collector-base voltage (V_{CB}) and depends on the value of the

Emitter current I_E.

* Therefore, the output characteristics are straight parallel lines in the active Region.

* Actually the collector current increases slowly with the collector-base voltage (around 0.5%). This is because of the early effect.

* But for most applications this increase in collector current can be ignored and it is considered as constant for a fixed value of Emitter current (I_E).

* The output resistance offered by the CB configuration is very high as a very large change in the collector-base voltage produces a very small change in the collector current.

* ~~When the emitter current is zero ($I_E = 0$)~~

Cut-off Region:

* In cut-off region both the Emitter-base junction and collector to base junction are Reverse biased.

* When both the junctions are reverse biased they act as a reverse biased diodes.

* In this condition $I_E = 0$ because of this there is no current flow theoretically zero current.

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* But practically because of minority charge carriers small amount of current flows that current is called as Reverse Saturation Current I_{CBO}.

* This Reverse Saturation Current I_{CBO} increases rapidly with increase in temperature.

* The dashed lines below $I_E = 0$ mA curve represents the cut-off region in the o/p characteristics curve.

* In this region, transistor doesn't conduct.

SATURATION REGION:

* In saturation region, both the collector-to base junction and Emitter-to base junctions are forward biased.

* The region left to the $V_{CB} = 0V$ line corresponds to the saturation region in the characteristic curve.

* From the figure, the collector-base voltage is ~~Negative~~ slightly negative in the saturation region, this is because the collector-to-base junction is also forward biased.

* There is an exponential increase in the collector current with a small increase in the collector-base voltage.

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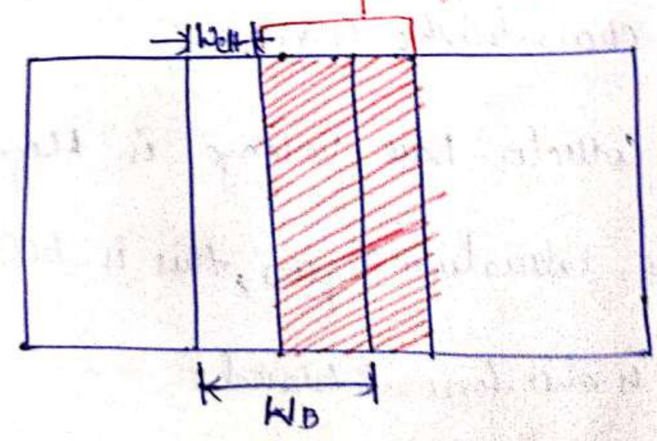
The EARLY EFFECT OR BASE-WIDTH MODULATION:

* In, I/P Characteristic Curves of Configurations the Curve shift left towards the Curve, this is because of "Early effect" or "Base-width Modulation".

DEFINITION: The Variation in the effective width of the Base Region in a Bipolar junction transistor due to a variation in the applied reverse biased collector to base voltages at the collector junction is called "Early Effect" or "Base-Width modulation".

* Basically, Base is a lightly doped Region in the BJT. When Collector to base junction is reverse biased the width of the depletion Region is more.

* This depletion Region is penetrated more into the base Region because of lightly doping of base Region.



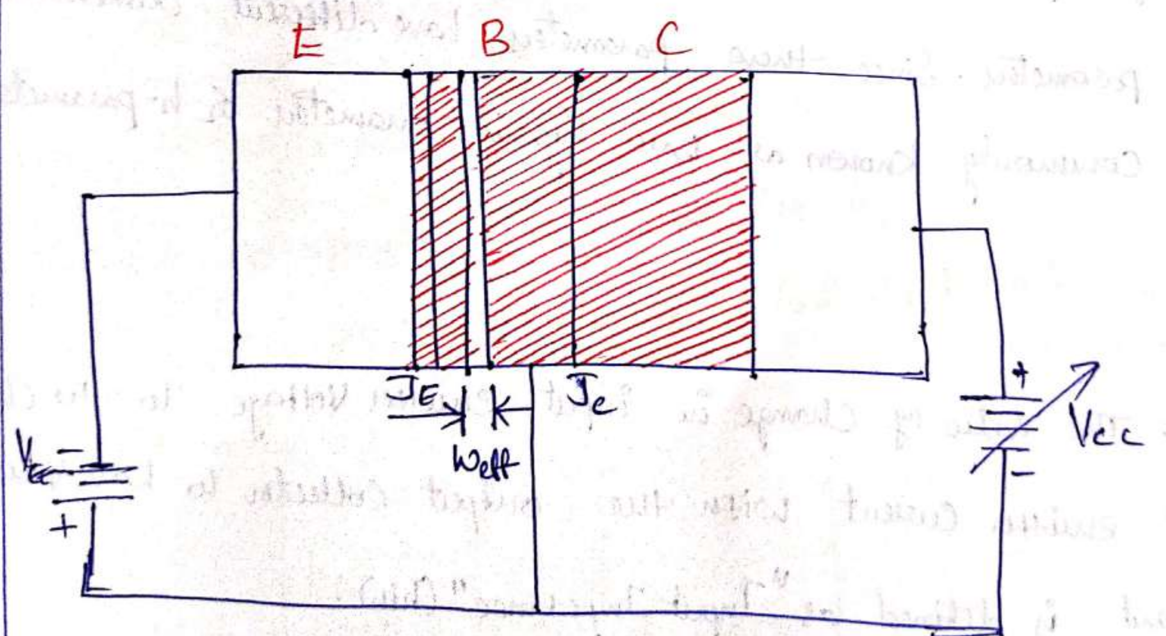
* As the Collector Voltage V_{CC} is made to increase the reverse bias, the space charge width i.e., Depletion Region width tends to increase.

* According to transistor Construction, Base Region is made very thin and very light doping.

* Because of this increase in reverse bias voltage, depletion Region tries to penetrate more into the base Region which reduces the effective Electrical width of the Base.

* At the Emitter Junction, this Reduction in base width affects the barrier potential among the depletion Region.

* This barrier potential at the J_E junction also decreases because of this I_E also increases and enters into conduction earlierly.



* This dependency of base width on Collector to base Voltage is known as Early effect.

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* This decrease in Effective base-width has three Consequences.

1. There is less chance for recombination within the base region. Hence α increases with increasing $|V_{CB}|$.

2. The charge gradient is increased within the base, and consequently, the current of minority carriers injected across the emitter junction increases.

3. For extremely large voltages, the effective base width may be reduced to zero, causing voltage breakdown in the transistor. This phenomenon is called the punch through.

TRANSISTOR PARAMETERS:

* The slope of the CB characteristics will give the following four transistor parameters. Since these parameters have different dimensions, they are commonly known as base hybrid parameters or h-parameters.

1. INPUT IMPEDANCE (h_{ib}):

Definition: The ratio of change in input emitter voltage to the change in input emitter current with the output collector to base voltage as constant is defined as "Input Impedance" (h_{ib}).

$$\text{Input Impedance } h_{ib} = \left.\frac{\Delta V_{EB}}{\Delta I_E}\right|_{V_{CB} = \text{Constant}}$$

* CB configuration has low input impedance. The typical value of h_{ib} ranges from $20\,\Omega$ to $50\,\Omega$.

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2. OUTPUT ADMITTANCE * [h_{ob}]:-

Definition: The ratio of change in the output collector current to the corresponding change in the output collector voltage with the input emitter current I_E kept constant is defined as output admittance (h_{ob}).

$$h_{ob} = \left.\frac{\Delta I_C}{\Delta V_{CB}}\right|_{I_E = \text{Constant}}$$

* The typical value of this parameter is of the order of 0.1 to 10 μmhos.

3. FORWARD CURRENT GAIN (h_{fb}):

Definition : The ratio of change in the output collector current to the corresponding change in the input emitter current keeping the output collector voltage V_{CB} constant is defined as Forward current gain.

$$h_{fb} = \left.\frac{\Delta I_C}{\Delta I_E}\right|_{V_{CB} = \text{Constant}}$$

* Its typical value ranges from 0.9 to 1.0

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4. REVERSE VOLTAGE GAIN: (h_{rb}):-

Definition: The ratio of change in the input emitter Voltage and the corresponding change in output collector Voltage with constant input emitter current I_E is defined as Reverse Voltage Gain (h_{rb}).

$$h_{rb} = \frac{\Delta V_{EB}}{\Delta V_{CB}} \Bigg|_{I_E = \text{Constant}}$$

* Its typical value is of the order of 10^{-5} to 10^{-4}.

2. COMMON EMITTER (CE) CONFIGURATION:

Definition: The configuration in which base acts as Input terminal, Collector as the output terminal and Emitter terminal is Common for both i/p and o/p terminals such configuration is called as "Common Emitter Configuration."

* Common Emitter configuration is also called as "Grounded Emitter Configuration".

CIRCUIT DIAGRAM

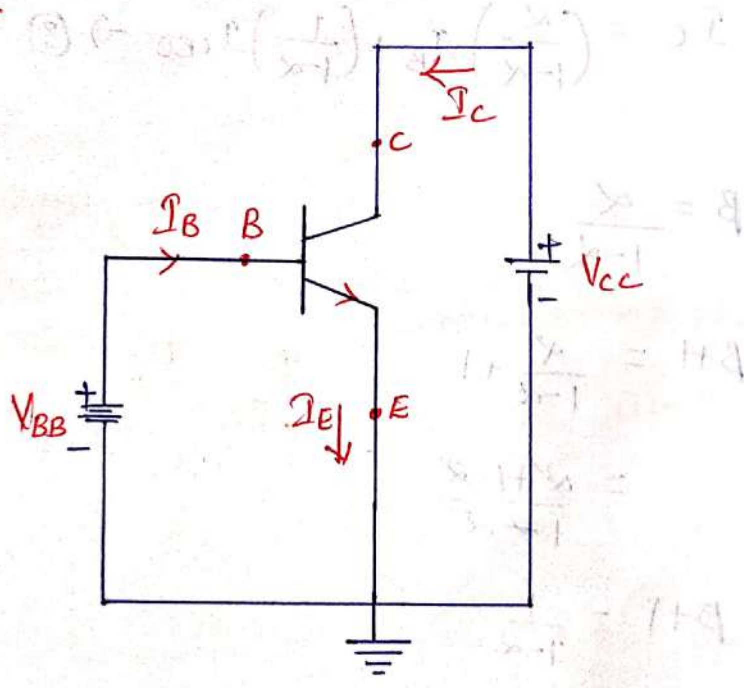

FIG: CE CONFIGURATION FOR NPN TRANSISTOR

RELATION BETWEEN I/P & O/P CURRENTS:

=) In CE Configuration, Input current is I_B and o/p current is I_C

From fundamental relation of currents in transistor

$$I_E = I_B + I_C \longrightarrow (1)$$

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$$I_C = \alpha I_E + I_{CBO} \rightarrow (2)$$

Substituting eq (1) in eq (2)

$$I_C = \alpha(I_C + I_B) + I_{CBO}$$

$$I_C = \alpha I_C + \alpha I_B + I_{CBO}$$

$$I_C - \alpha I_C = \alpha I_B + I_{CBO}$$

$$I_C(1-\alpha) = \alpha I_B + I_{CBO}$$

$$I_C = \left(\frac{\alpha}{1-\alpha}\right) I_B + \left(\frac{1}{1-\alpha}\right) I_{CBO} \rightarrow (3)$$

$$\because \beta = \frac{\alpha}{1-\alpha}$$

$$\beta + 1 = \frac{\alpha}{1-\alpha} + 1$$

$$= \frac{\alpha + 1 - \alpha}{1-\alpha}$$

$$\beta + 1 = \frac{1}{1-\alpha}$$

$\therefore$ equation (3) becomes

$$I_C = \beta I_B + (1+\beta) I_{CBO} \rightarrow (4)$$

* In CE Configuration, I_B is the i/p current and I_C is the o/p current.

* If the base circuit is open i.e., $I_B = 0$, then a small collector current flows from the collector to emitter. This is denoted by I_{CEO}.

∴ Equation (4) becomes

$$I_C = \beta I_B + I_{CEO}$$

where $I_{CEO} = (1+\beta) I_{CBO}$

Since $I_B >> I_{CEO}$

$$I_C = \beta I_B$$

$$\beta = \frac{I_C}{I_B}$$

CURRENT AMPLIFICATION FACTOR:

Definition: The ratio of change in o/p current (I_C) to the change in i/p current (I_B) is defined as current amplification factor

$$\beta = \frac{\Delta I_C}{\Delta I_B}$$

Relation between α & β:

By definition $I_C = \alpha I_E$

$$I_E = I_B + I_C$$

$$I_E = I_B + \alpha I_E$$

$$I_E - \alpha I_E = I_B$$

$$I_B = (1-\alpha) I_E \rightarrow (1)$$

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Dividing both sides of eq(1) by I_C, we get

$$\frac{I_B}{I_C} = \frac{I_E}{I_C}(1-\alpha)$$

$$\frac{1}{\beta} = \frac{1}{\alpha}(1-\alpha)$$

$$\boxed{\beta = \frac{\alpha}{1-\alpha}}$$

$$\boxed{\alpha = \frac{\beta}{1+\beta}}$$

$(\because \beta = \frac{I_C}{I_B}$

$\frac{1}{\beta} = \frac{I_B}{I_C}$

$\because \alpha = \frac{I_C}{I_E}$

$\frac{1}{\alpha} = \frac{I_E}{I_C}$

INPUT CHARACTERISTICS: *

DEFINITION: The Graphical Representation which explains the relation between the I/p current (I_B) and I/p Voltage (V_{BE}) is said to be the Input characteristics of CE Configuration.

* In CE configuration, I/p terminal - BASE
  Common terminal - EMITTER
  O/p terminal - COLLECTOR

∴ Input current - I_B

Input Voltage - V_{BE} (Base to Emitter Voltage)

output current - I_C

output Voltage - V_{CE} (Collector to Emitter Voltage)

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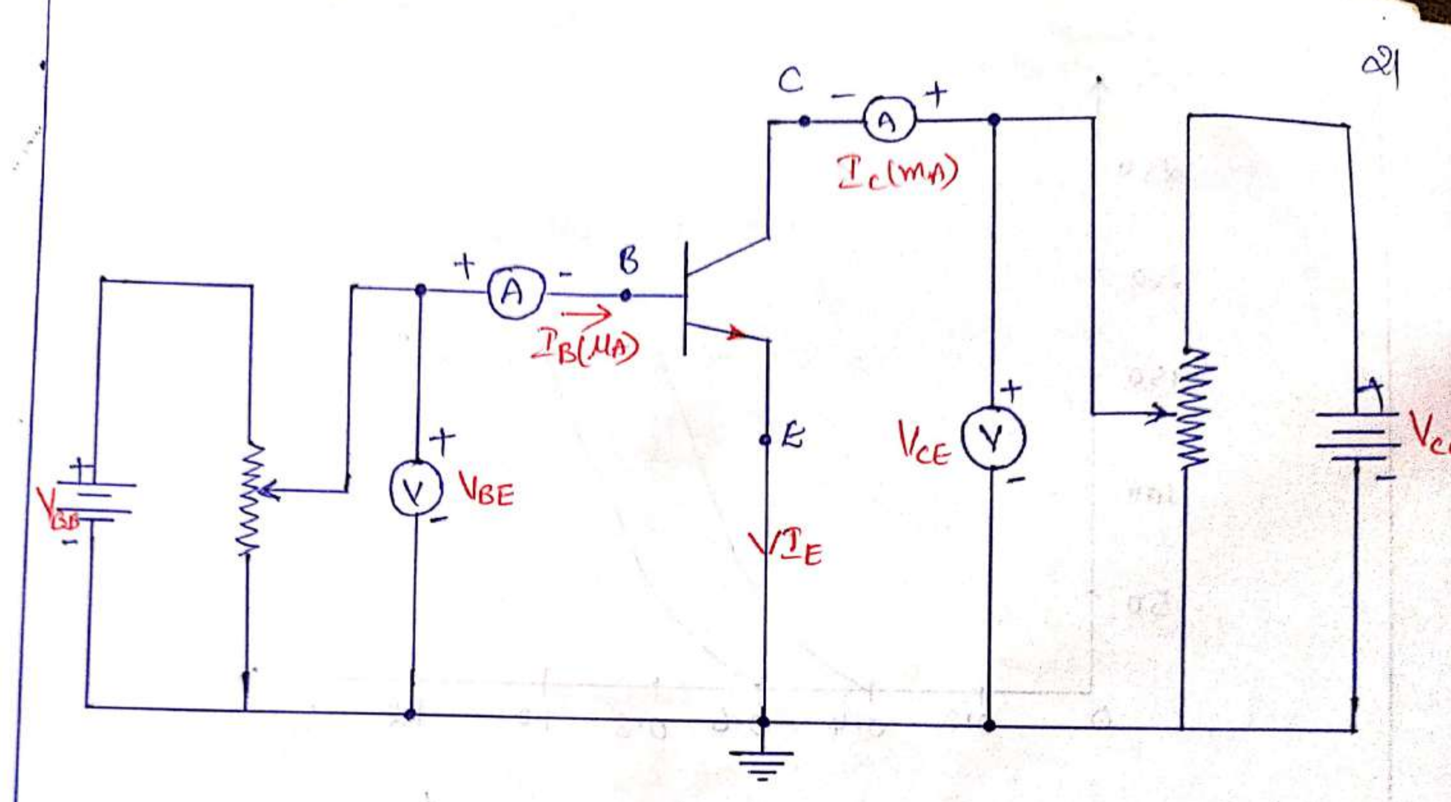

FIG: CIRCUIT TO DETERMINE CE STATIC CHARACTERISTICS

* To determine Input characteristics,

1) Keep the output Voltage i.e., Collector to ~~base~~ Emitter Voltage (V_{CE}) constant at zero Volts.

2) Increase the Input current i.e, base current in equal steps from zero by increasing Input voltage i.e, Base to Emitter Voltage V_{BE}.

3) Note the corresponding V_{BE} and I_B values.

4) This procedure is repeated for higher fixed values of V_{CE} and the curves of I_B Vs V_{BE} are drawn.

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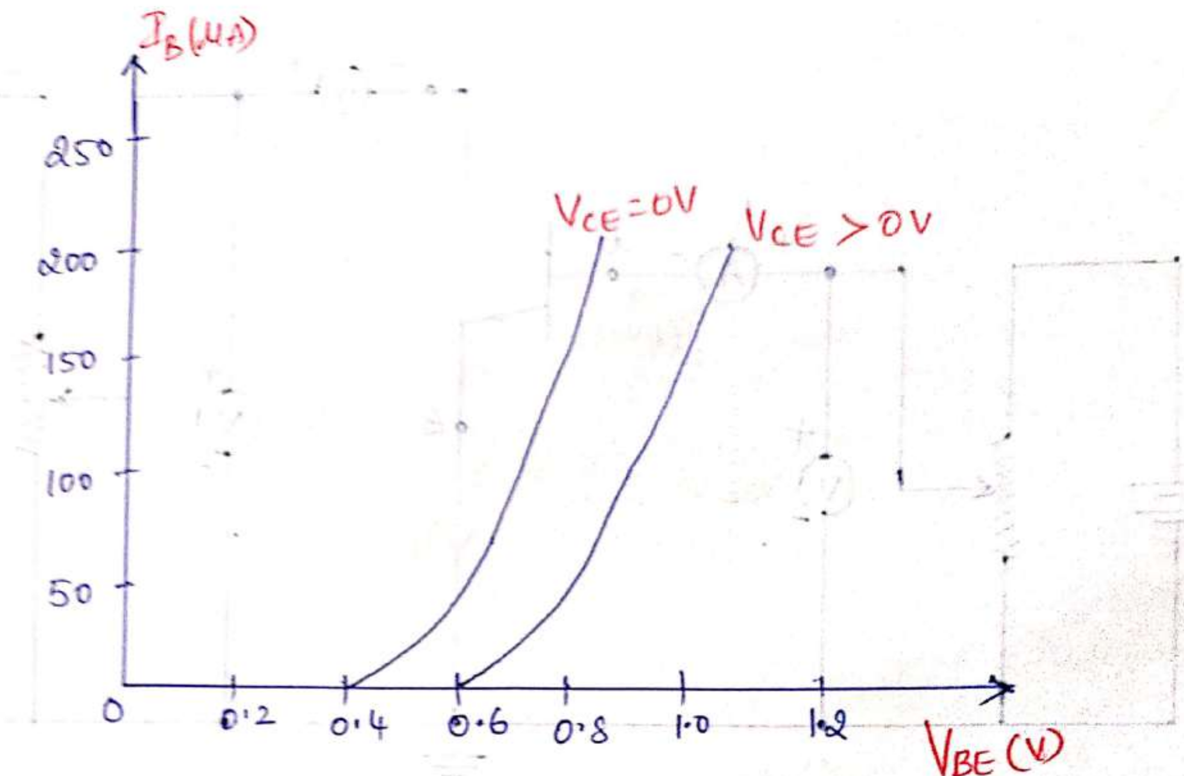

FIG: CE INPUT CHARACTERISTICS-

CASE:1 When $V_{CE}=0V$

* When $V_{CE}=0V$, the emitter-base junction is forward biased and the junction behaves as a forward biased diode.

* Hence the Input characteristic curve for $V_{CE}=0V$ will be similar to that of a forward biased diode.

* The current (I_B) increases exponentially when V_{BE} exceeds the cut-in voltage.

Case:2 When $V_{CE}>0V$

* When collector to emitter voltage (V_{CE}) is increased, the width of the depletion region at the reverse biased collector-base junction will also increase.

* Because of this, effective width of the base decreases.

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* This effect causes a decrease in the base current I_B.

* Hence to get the same value of I_B for $V_{CE} = 0$, V_{BE} should be increased.

(Eg: $V_{BE} = 0.4V, I_B = 0 \mu A$; $V_{BE} = 0.6V, I_B = 0 \mu A$).

* As a result the curve shifts to right as V_{CE} increases.

OUTPUT CHARACTERISTICS:

DEFINITION: The Graphical Representation which explains relation between output current I_C and output voltage V_{CE} by keeping I/P current I_B constant is said to be "Output characteristics of CE configuration"

* In CE configuration, output current is collector current (I_C) and output voltage is collector to emitter voltage (V_{CE}).

* To determine the output characteristics,

1) Keep the base current I_B constant at a suitable value by adjusting base-emitter voltage V_{BE}.

2) Increase the collector to emitter voltage (V_{CE}) from zero and note the corresponding collector current values (I_C).

3) Repeat the same procedure for different fixed values of I_B.

4). Now the curves of I_C Vs V_{CE} are plotted for constant values of I_B.

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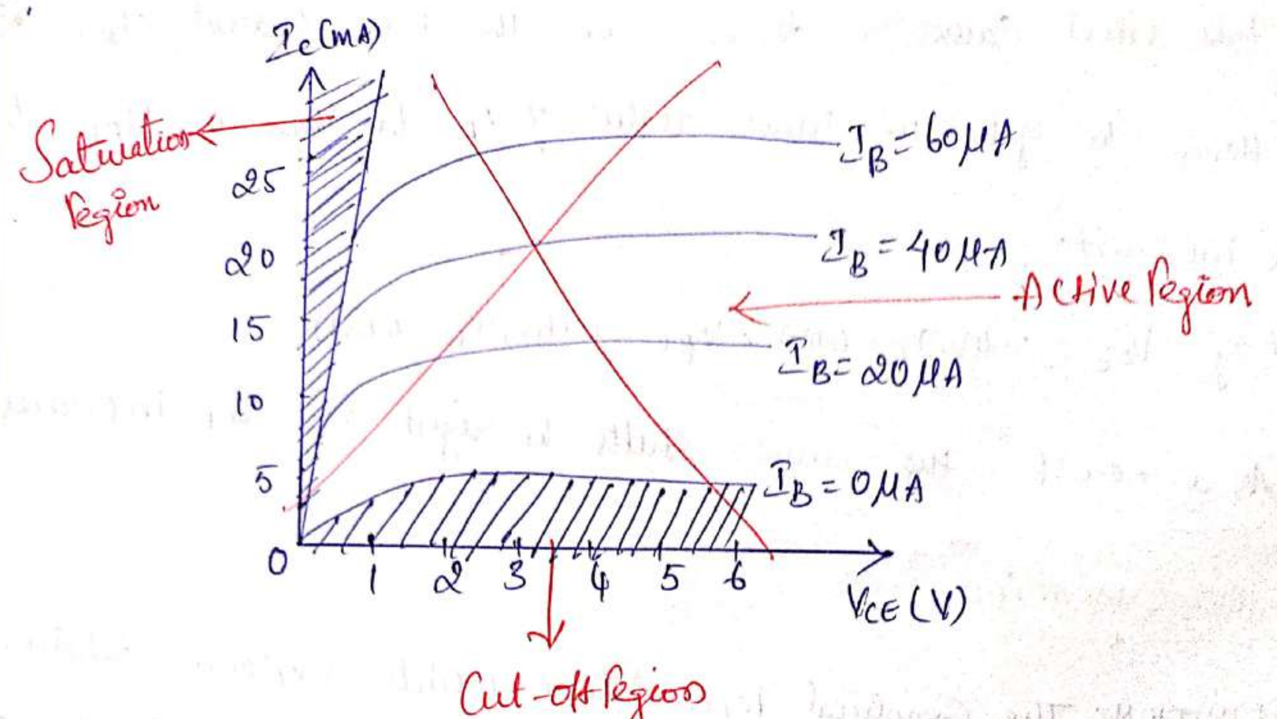

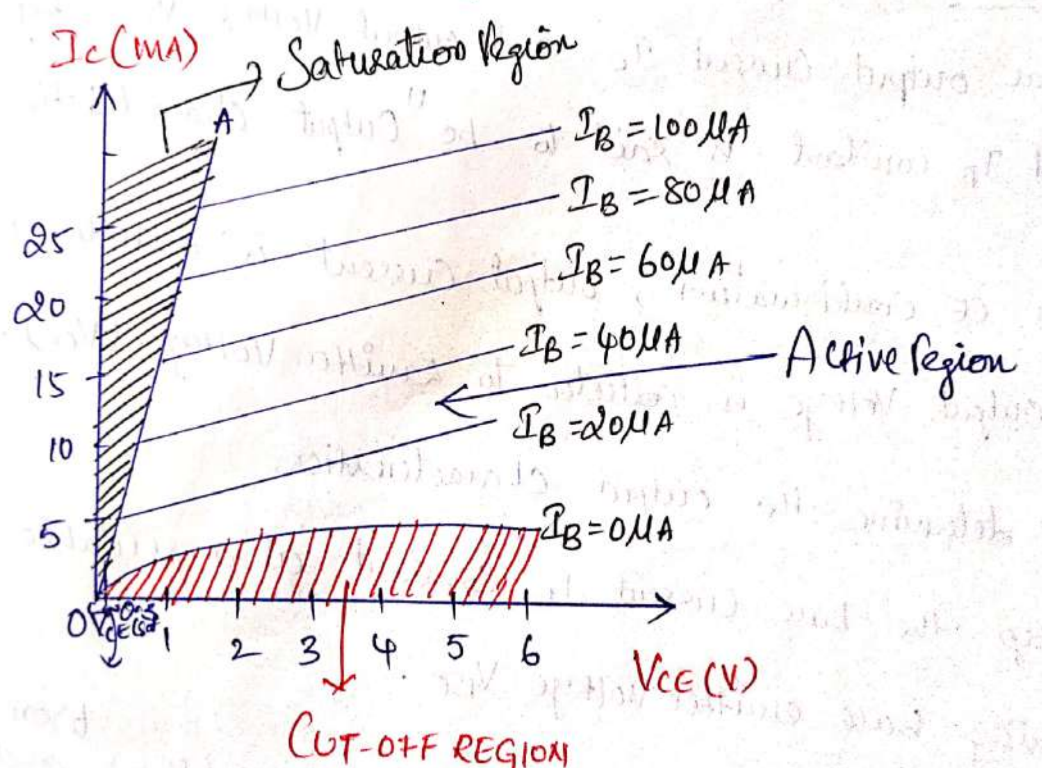

FIG: CE OUTPUT CHARACTERISTICS

* For larger values of V_{CE}, due to Early effect, a very small change in α is reflected in a very large change in β

* For Eg: when $\alpha = 0.98$ $\beta = \frac{0.98}{1-0.98} = 49$

$\alpha = 0.98$ $\beta = \frac{0.98}{1-0.98} = 49$

* Here, a slight increase in α results in an more increase in β. 23
* Hence, the o/p characteristics of CE configuration shows a larger slope when compared with CB configuration.
* The output characteristics have three regions namely,

1. Active Region
2. Saturation Region
3. Cut-off Region.

1. ACTIVE REGION:

* In this Region emitter-base junction is forward biased and collector-base junction is reverse biased.
* The central region in the o/p characteristics where the curves are uniform in spacing is called Active Region
* As V_{CE} is increased, reverse bias increases at collector junction. This causes depletion region to spread more in base than in collector, reducing the chances of recombination in the base.
* This early effect causes collector current to rise more sharply with increasing V_{CE} in the active region.

2. SATURATION REGION:

* In saturation region both the emitter-base junction and collector-base junctions are forward biased.

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* If V_{CE} is reduced to a small value such as 0.2V, then collector-base junction becomes forward biased, since the emitter-base junction is already forward biased.

* The input junction in CE configuration is base to emitter junction, which is always forward biased to operate transistor in active region.

* The reduced V_{CE} voltage is called as saturation voltage i.e., $V_{CE(sat)}$ whose value ranges from 0.1 to 0.3V

* In saturation region, the value of the collector current is independent of the base current and depends on the value of saturation resistance.

* Saturation Resistance: The ratio of saturation voltage $V_{CE(sat)}$ to the collector current I_C is called saturation resistance.

$$\text{Saturation resistance } R_{CE(sat)} = \frac{V_{CE(sat)}}{I_C}$$

* The region of OA line in the curve represents the saturation region.

3. CUT-OFF REGION:

* The region in which the emitter-base junction and collector base junction are reverse biased is called cut-off region

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* Also the i/p current I_B e, base current $I_B = 0$ in this region.

* We know that, $I_C = \beta I_B + (\beta+1) I_{CBO}$

When $I_B = 0$; $I_C = \beta(0) + (\beta+1) I_{CBO}$

$$I_C = (\beta+1) I_{CBO}$$

$$\because (\beta+1) I_{CBO} = I_{CEO} \qquad (\because (\beta+1) I_{CBO} = I_{CEO})$$

$$I_C = I_{CEO}$$

* In cut-off region the collector current is equal to reverse saturation current i.e., leakage current I_{CEO}.

* This is considerable amount of collector current flowing through the transistor.

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TRANSISTOR PARAMETERS:

a) INPUT IMPEDANCE (hie):

Definition: The ratio of change in input base to emitter Voltage to the change in input base current with the o/p voltage constant i.e., V_{CE} is called Input Impedance.

$$h_{ie} = \left. \frac{\Delta V_{BE}}{\Delta I_B} \right|_{V_{CE} \text{ is Constant}}$$

RANGE: The typical value of hie ranges from 500 to 2000 Ω

b) OUTPUT ADMITTANCE:

Definition: The ratio of change in the output collector current to the corresponding change in the output collector to emitter Voltage with the input base current I_B kept constant is called as output Admittance.

$$h_{oe} = \left. \frac{\Delta I_C}{\Delta V_{CE}} \right|_{I_B \text{ is Constant}}$$

RANGE: The typical value of hoe ranges from 0.1 to 10 µmhos.

c) FORWARD CURRENT GAIN:

Definition: The ratio of the change in the collector current to the corresponding change in the base current keeping the output collector to emitter Voltage constant is called "forward current gain".

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$$h_{fe} = \frac{\Delta I_C}{\Delta I_B}\Bigg|_{V_{CE} = \text{Constant}}$$

Range: The typical value of h_{fe} ranges from 20 to 200.

d) REVERSE VOLTAGE GAIN:

Definition: The ratio of change in input Base to Emitter Voltage to the corresponding change in output Collector to Emitter Voltage with constant input current I_B is defined as Reverse Voltage gain.

$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}\Bigg|_{I_B \text{ Constant}}$$

Range: The typical value of h_{re} ranges from 10^{-5} to 10^{-4}

ADVANTAGES OF CE

1. A Common Emitter amplifier is inverting and has low i/p Impedance.
2. ~~High~~ moderate output Impedance.
3. High Voltage gain.
4. High Current gain.

DISADVANTAGES

1. It has a high o/p resistance.
2. It responds poorly to high frequencies
3. It has high thermal instabilities
4. It's voltage gain is very unstable.

APPLICATIONS :

1. The common emitter circuit is popular because it's well-suited for voltage amplification, especially at low frequencies.
2. Common emitter amplifiers are also used in Radio frequency transceiver circuits
3. It is commonly used in low-noise amplifiers.

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3. COMMON COLLECTOR CONFIGURATION:

Definition: The Configuration in which base acts as a Input terminal, emitter as a output terminal and collector is common to both input and output terminals then such configuration is called "Common collector configuration".

* Common collector configuration is also called as "Emitter follower" & "Grounded collector configuration".

CIRCUIT DIAGRAM:

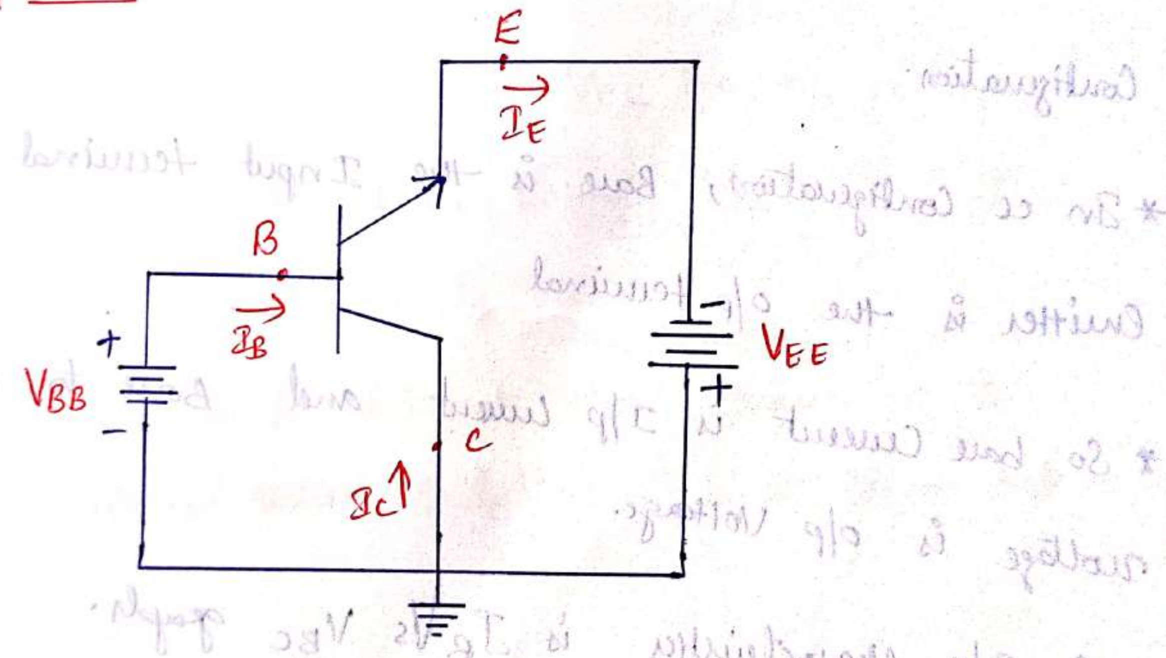

FIG: CE CONFIGURATION FOR NPN TRANSISTOR

* we know that $I_E = I_B + I_C \rightarrow ①$

$$I_C = \alpha I_E + I_{CBO} \rightarrow ②$$

Sub eq ② in eq①

$$I_E = I_B + (\alpha I_E + I_{CBO})$$

$$I_E - \alpha I_E = I_B + I_{CBO}$$

$$I_E(1-\alpha) = I_B + I_{CBO}$$

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$$I_E = \frac{1}{1-\alpha} I_B + \frac{1}{1-\alpha} I_{CBO}$$

$$I_E = (\beta+1) I_B + (\beta+1) I_{CBO} \quad (\because \gamma = \beta+1)$$

$$\boxed{I_E = \gamma I_B + \gamma I_{CBO}}$$

$\because I_B >> I_{CBO} \Rightarrow I_E = \gamma I_B$

$$\boxed{\gamma = \frac{I_E}{I_B}}$$

INPUT CHARACTERISTICS:

Definition: The Graphical Representation which explains the relationship between Input current i.e., base current and Input Voltage i.e., Base to collector V_{BC} defines the I/p characteristics of CC Configuration.

* In CC Configuration, Base is the Input terminal and emitter is the o/p terminal
* So base current is I/p current and Base to collector voltage is o/p Voltage.
* So I/p characteristics is I_B Vs V_{BC} graph.
* The circuit to determine the Static characteristics of CC is as shown below.

Current Amplification factor: The ratio of change in o/p current I_E to the change in i/p current I_B is called current amplification factor.

$$\boxed{\gamma = \frac{\Delta I_E}{\Delta I_B}}$$

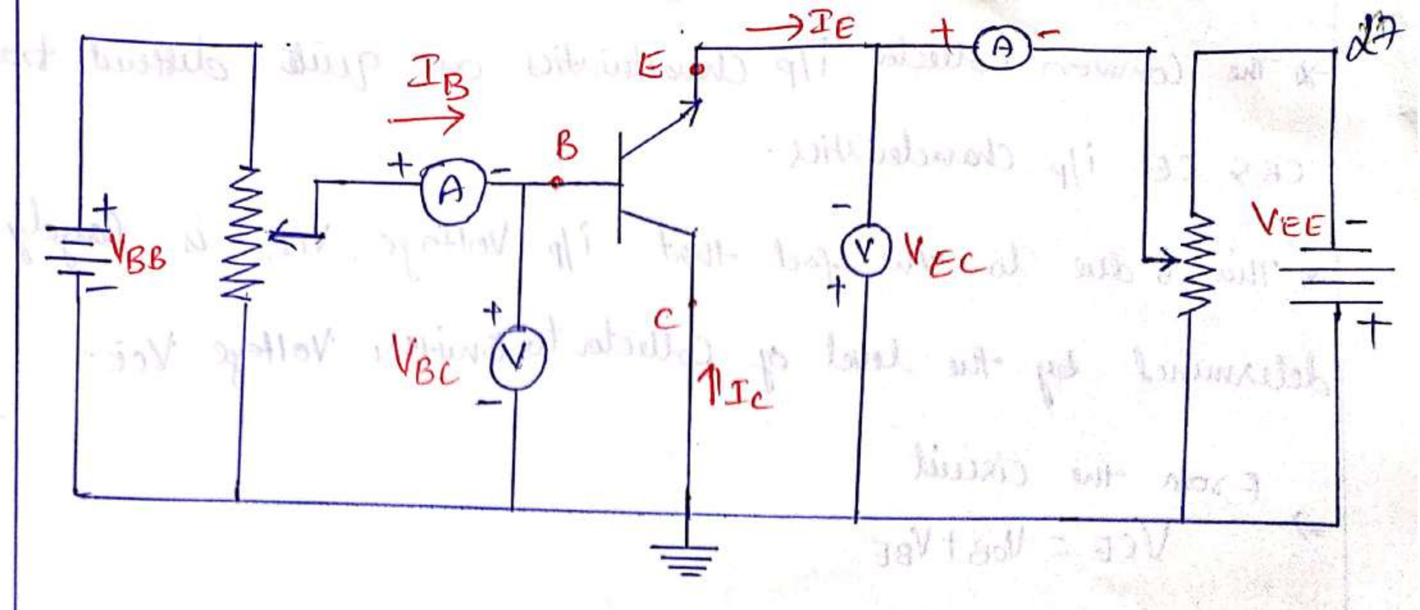

FIG: CIRCUIT TO DETERMINE CC STATIC CHARACTERISTICS

* To determine the Input characteristics,

1. Keep Emitter to collector Voltage V_{EC} i.e., o/p Voltage.

2. Increase the Base to collector Voltage V_{BC} in equal steps and note the corresponding I_B values.

3. This is repeated for different fixed values of V_{EC}.

⇒ Plots for different values of I_B Vs V_{EC} is as shown below

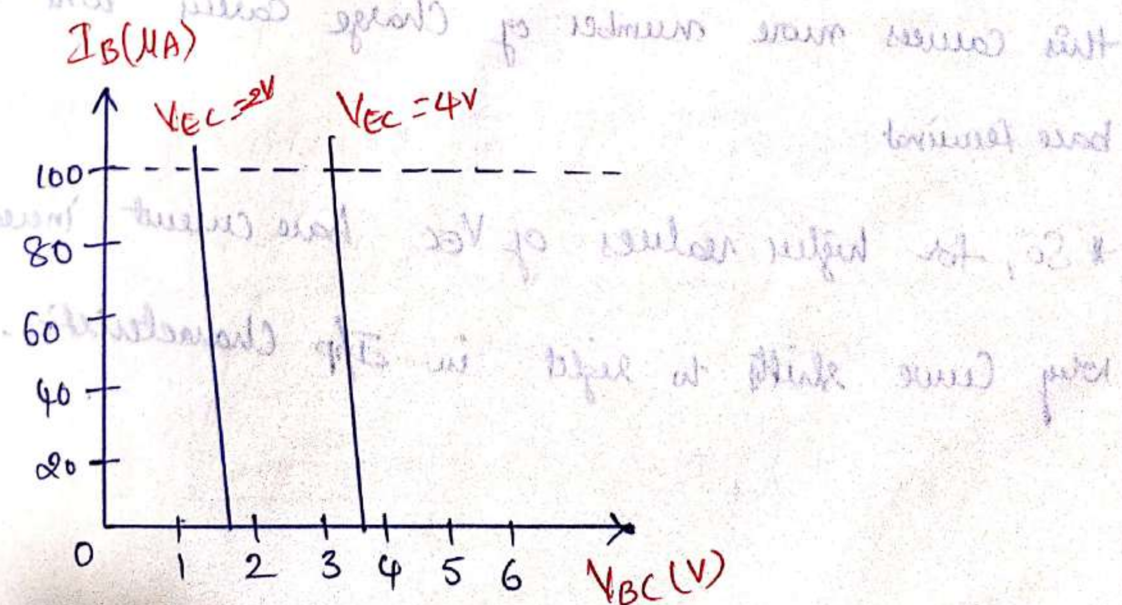

FIG: INPUT CHARACTERISTICS OF CC CONFIGURATION

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* The Common Collector i/p Characteristics are quite different from CB & CE i/p Characteristics.

* This is due to the fact that i/p Voltage V_{CB} is largely determined by the level of Collector to Emitter Voltage V_{CE}.

From the circuit

$\Rightarrow$ $V_{CE} = V_{CB} + V_{BE}$

Case 1 When $V_{EC} = 2V$

* If Collector to base Voltage V_{CB} is increased then the depletion width increases this will reduce the effective width of the base.

* So, the probablity of recombination in base region also reduces. due to this base current I_B reduces.

Case 2 When $V_{EC} = 4V$

* When forward biased voltage at emitter junction increases this causes more number of charge carriers will reach the base terminal

* So, for higher values of V_{EC} base current increases thats why Curve shifts to right in I/p characteristics.

OUTPUT CHARACTERISTICS:

* We know that $I_C = \alpha I_E + I_{CBO}$

$$I_E >> I_{CBO}$$

$$I_C = \alpha I_E$$

* α ranges from 0.95 to 0.98 which is approximately equal to unity

$$I_C \simeq I_E$$

* Because of this o/p ~~ef~~ Emitter current is almost equal to Collector current.

* plot is ~~equ~~ similar to the o/p curves of CE configuration

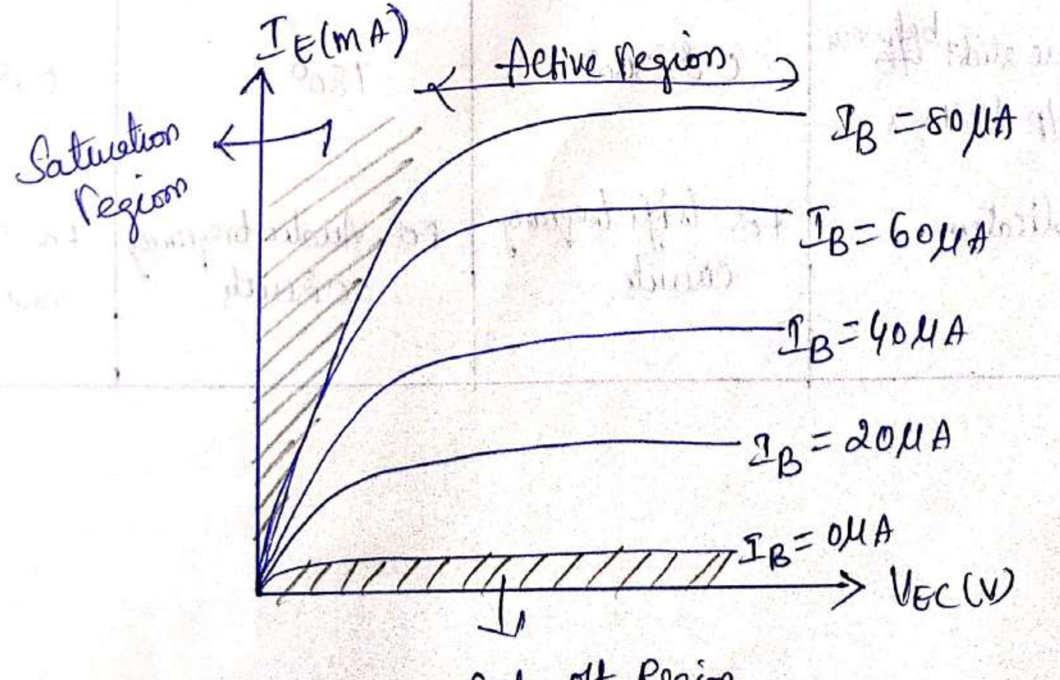

FIG: OUTPUT CHARACTERISTICS OF CC CONFIGURATON

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ADVANTAGES

1. It has high current gain
2. It has lowest O/p impedance
3. The Voltage gain of a CC is at best slightly lesser than one.

COMPARISON OF CB, CE and CC Configurations:

PROPERTY	CB	CE	CC
1. Input Resistance	Low (about 100 Ω)	Moderate (about 750 Ω)	High (about 750 kΩ)
2. Output Resistance	High (about 450 kΩ)	Moderate (about 45 kΩ)	Low (about 25 Ω)
3. Current gain	1	High	High
4. Voltage gain	About 150	About 500	Less than one
5. phase shift between i/p & o/p Voltages	0 & 360°	180°	0 & 360°
6. Applications	For high frequency circuits	For Audio frequency circuits	For Impedance matching

Relation between α, β & γ:

* In CC configuration current amplification factor is given by γ

$$\gamma = \frac{I_E}{I_B} \rightarrow (1)$$

W.K.T $I_E = I_B + I_C$

$$I_B = I_E - I_C \rightarrow (2)$$

Sub eq 2 in eq (1)

$$\gamma = \frac{I_E}{I_E - I_C} \rightarrow (3)$$

divide eq 3 Numerator & denominator with I_E

$$\gamma = \frac{I_E / I_E}{\frac{I_E}{I_E} - \frac{I_C}{I_E}}$$

$$\boxed{\gamma = \frac{1}{1-\alpha}} \quad \left(\because \alpha = \frac{I_C}{I_E}\right)$$

Similarly $\gamma = \frac{I_E}{I_B}$

$$\gamma = \frac{I_B + I_C}{I_B}$$

divide numerator & denominator with I_B

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$$\gamma = \frac{\frac{I_B}{I_B} + \frac{I_C}{I_B}}{\frac{I_B}{I_B}}$$

$$\boxed{\gamma = 1+\beta} \quad \left(\because \beta = \frac{I_C}{I_B}\right)$$

BASE SPREADING RESISTANCE:

Definition: The Resistance offered by the narrow path region of base terminal is called "Base spreading Resistence".

* It is designated by "r_b'".

Emitter depletion region, Collector depletion region

N P N

E C B

V_{EB} V_{CB}

* we know that width of the base region of a transistor is extremely small. Therefore, the current which enters the base region, across the emitter-base junction, has a narrow path to reach the base terminal.

* The value of base spreading resistance can be increased by increasing the reverse-bias voltage (V_{CB}) across the collector-junction.

* The width of collector-base depletion layer increases and it penetrates more into the base region from that of collector. Because of this cross-sectional area of base reduces.

* The small cross-sectional area means a large base-spreading resistence. It is about 50 to 150 Ω, in some cases it may be 1000 Ω

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* When a current passes through the base spreading resistance, it produces a voltage drop across it.
* It has been observed that the effect of Base spreading resistance is significant in high frequency circuits. At low frequencies, it has practically no effect.

EBERS-MOLL MODEL:

* Ebers-moll model is a transistor model which describes the operating states of a transistor.
* This model is useful to obtain information about the dc characteristics of a transistor.
* The transistor operates in active region when emitter junction is forward biased and collector junction is reverse biased.
* This model generalizes the behaviour of a transistor by taking into account the inverted mode of operation of transistor.

FIG: EBERS MOLL MODEL OF A PNP TRANSISTOR

By applying KCL at collector node

Collector current $I_C = -\alpha_N I_E + I$

$$I_C = -\alpha_N I_E + I_0 (e^{V_C/V_T} - 1)$$

=) where I is the diode current. as I_0 is the magnitude of reverse saturation current then $I = -I_{CO}$, then

$$I_C = -\alpha_N I_E - I_{CO} (e^{V_C/V_T} - 1)$$

* The base spreading resistances has been omitted and the difference b/n I_{CBO} & I_{CO} have also been neglected.
* From the fig, it is evident that dependent current sources can be eliminated from the fig provided $\alpha_N = \alpha_I = 0$.
* In such a condition,
* For example, by making the width of the base much larger than the diffusion length of the minority carriers in the base, all the minority carriers will recombine in the base and none will survive to reach the collector.
* In such as condition transport factor β and then also current gain factor α will be zero.
* Thus under these conditions, the transistor action ceases and we simply have two diodes placed back to back

* The dependency of the currents in a transistor is upon the junction voltages & vice-versa may be obtained by starting with the equation here,

$$I_C = -\alpha_N I_E - I_{CO}\left(e^{V_C/V_T} - 1\right) \rightarrow ① \quad (\because I_C = \alpha I_E + I_{CO})$$

* Here N in α_N indicates the normal mode of operation of the transistor and minus (-) sign indicates its direction

* For Inverted mode of operation, equation will be,

$$I_E = -\alpha_I I_C - I_{EO}\left(e^{V_E/V_T} - 1\right) \rightarrow ②$$

* Here α_I is the inverted common base current gain, just like α_N in normal operation.

$I_{EO} \rightarrow$ Reverse saturation current flowing at emitter junction

$V_E \rightarrow$ Voltage drop at the emitter junction

* Ebers moll model involves two ideal diodes connected back to back with reverse saturation currents I_{EO} and I_{CO}.
* Two dependent current controlled current sources shunting the ideal diodes. The current sources account for the minority carrier transport across the base.

* From above discussion, it is clear that a transistor cannot be constructed by simply connecting two seperate diodes back to back.

TRANSISTOR AS AN AMPLIFIER:

AMPLIFIER: An Amplifier is an electronic device or circuit which is used to increase the magnitude of the signal applied to its input.

* For a transistor to act as an amplifier, it should be properly biased.

* A transistor acts as an amplifier by raising the strength of a weak signal.

* The DC bias voltage applied to the emitter base junction, makes it remain in forward biased condition.

* This forward biased is maintained regardless of the polarity of the signal.

* The below figure shows how a transistor looks like when connected as an amplifier.

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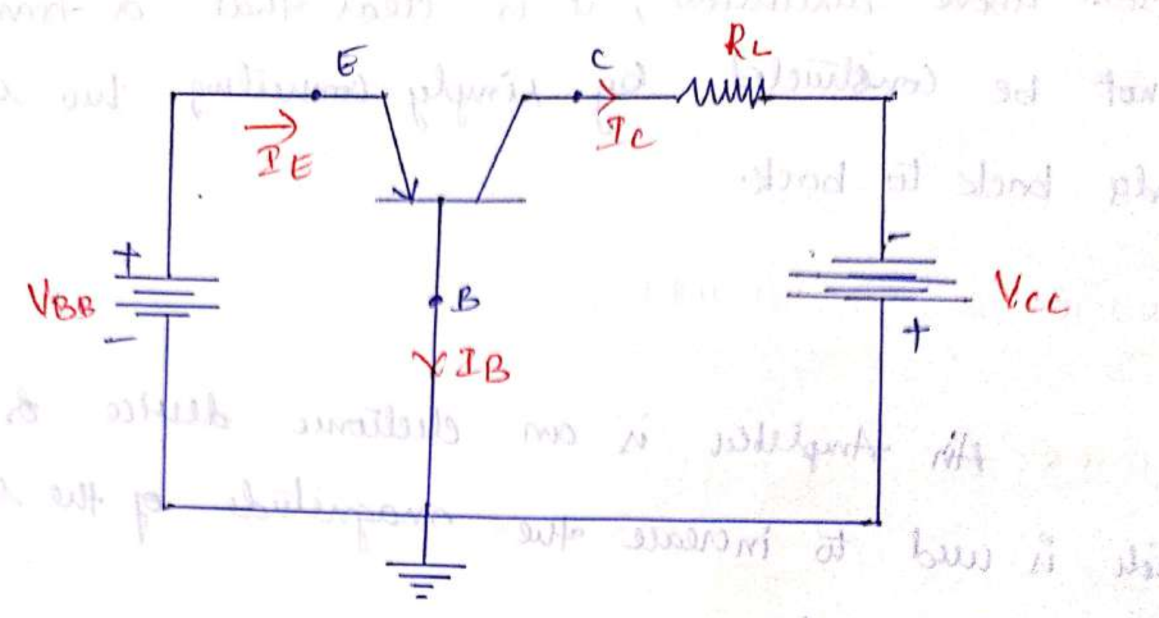

FIG: TRANSISTOR AS AN AMPLIFIER

* To explain the amplification process consider a p-n-p transistor connected to a load resistor (R_C).
* The load resistor "R_L" is connected in series with the collector power supply (V_{CC}).
* When emitter to base junction is in forward bias V_{BE} and collector to base junction (V_{CB}) is in reverse bias the transistor is operated in active region and acts as a Amplifier.
* The emitter current caused by the input signal contributes the collector current, which when flows through the load resistor R_L, results in a large voltage drop across it.

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* A small change in the I/p Voltage between emitter and base (ΔV_i) causes a large change in emitter current (ΔI_E).

* A fraction of this change in current is collected and passed through R_L and it is denoted as α'.

* The change in Voltage across load resistor R_L due to this current is

$$\boxed{\Delta V_0 = \alpha' R_L \Delta I_E} \rightarrow ①$$

* The Voltage amplification factor $\boxed{A_V = \frac{\Delta V_0}{\Delta V_i}} \rightarrow ②$

* If $\frac{\Delta V_0}{\Delta V_i} > 1$, then Voltage amplification takes place.

* The change in i/p Voltage (ΔV_i) across the dynamic resistance r_e' at emitter Voltage is,

$$\boxed{\Delta V_i = r_e' \Delta I_E} \rightarrow ③$$

Substituting eq ① & ③ in eq ② we get,

$$A_V = \frac{\Delta V_0}{\Delta V_i} = \frac{\alpha' R_L \Delta I_E}{r_e' \Delta I_E} = \frac{\alpha' R_L}{r_e'} > 1$$

* From the above equation A_V is greater than unity so transistor acts as amplifier.

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LIMITS OF OPERATION (BREAKDOWN IN TRANSISTORS):-

* There is a possiblity of voltage breakdown in the transistor at high voltages even though the rated dissipation of the transistor is not exceeded.
* Therefore, there is an upper limit to the maximum allowable collector junction voltage.
* There are two types of breakdown, namely
  1. Avalanche multiplication (or) Avalanche Breakdown
  2. Reach through (or) Punch through.

1. AVALANCHE MULTIPLICATION (OR) BREAKDOWN:

* When the diode is reverse biased, there is a limit on the voltage that can be applied which is the avalanche voltage.
* Similarly, in the transistor, the maximum reverse biasing voltage which may be applied before breakdown voltage between the collector and base terminals with the emitter open is called breakdown voltage BV_{CBO}.
* Therefore, an upper limit is set on the collector voltage V_{CB} by avalanche breakdown in the reverse biased collector-base junction.

* Breakdown may occur because of Avalanche multiplication of the current I_{co} that cross the collector junction.

* ~~As a result of this multiplication of the current I_{co} that crosses the collector junction~~

* As a result of this multiplication, the current becomes MI_{co}.

  where M is the multiplication factor.

* At the breakdown voltage BV_{CBO}, multiplication factor M becomes infinite and the current rises abruptly in the breakdown region. There will be large changes in current with small changes in applied voltage.

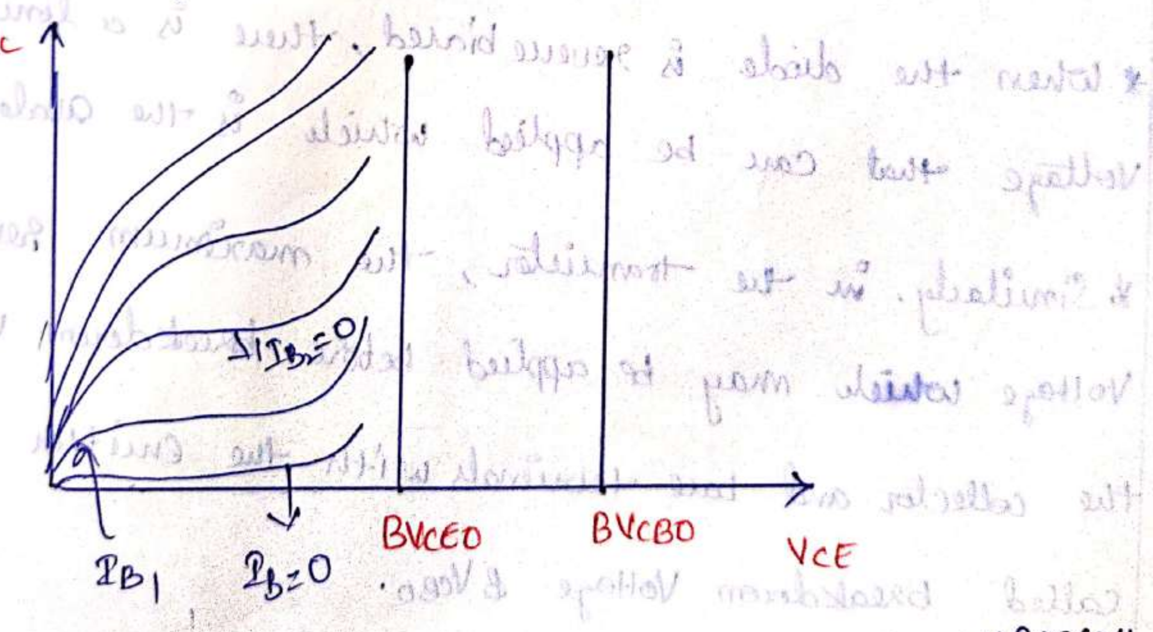

FIG: CE CHARACTERISTICS IN THE BREAKDOWN REGION

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* The Avalanche multiplication factor depends on the Voltage V_{CB} between collector and base, which has been found to be given empirically by,

$$M = \frac{1}{1 - \left[\frac{V_{CB}}{BV_{CBO}}\right]^n} \rightarrow (1)$$

* where the empirical constant n depends on the lattice material and the Carrier type, which is usually in the range of about 2 to 10.

For N-type $n = 4$

p-type $n = 2$

* For the CE Configuration, the collector to emitter breakdown Voltage BV_{EO} with base open is,

$$BV_{CEO} = BV_{CBO} \sqrt[n]{\frac{1}{h_{FE}}}$$

* In general, BV_{CEO} is 40 to 50% of BV_{CBO}. This is the upper limit of V_{CE} that can be placed across the transistor without damaging it.

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2. ## REACH THROUGH (OR) PUNCH THROUGH:

* According to Early effect, the width of the collector-junction transition region increases with increased collector-junction voltage.
* As the voltage applied across the junction V_{CB} increases the transition region penetrates deeper into the base and will have spread completely across the base to reach the emitter junction, as the base is very thin.
* Thus, the collector voltage has reached through the base region.
* This effect, known as reach-through, also effects the o/p characteristics of a transistor.
* It is possible to raise the punch-through voltage by increasing the doping concentration in the base, but this automatically reduces the Emitter efficiency.
* Punch through takes place at a fixed voltage between collector and base and is not dependent on circuit configuration.
* Whereas Avalanche multiplication takes place at different voltages depending upon the circuit configuration.

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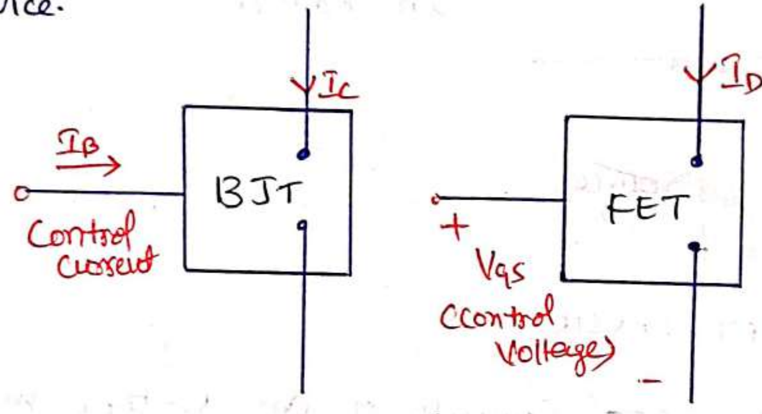
JUNCTION FIELD EFFECT TRANSISTOR

INTRODUCTION:

* The field effect transistor (FET) is a three terminal device used for a variety of applications.

* The primary difference between BJT and JFET is BJT is a Current controlled device whereas FET is a Voltage Controlled device.



* For BJT, the current I_C is a direct function of the level of I_B. For FET, the current I_D will be a function of the voltage V_{GS} applied to the input circuit

* FET is a unipolar device depending solely on either electron (n-channel) or hole (p-channel) conduction.

* For the FET an electric field is established by the charges present that will control the conduction path of the output circuit without the need for direct contact between the controlling and controlled quantities.

* Depending upon the charge carriers, JFET is classified into 1. N-channel JFET 2. P-channel JFET

CONSTRUCTION OF N-CHANNEL JFET:

* The JFET is a three terminal device with one terminal Capable of Controlling the Current between other two.

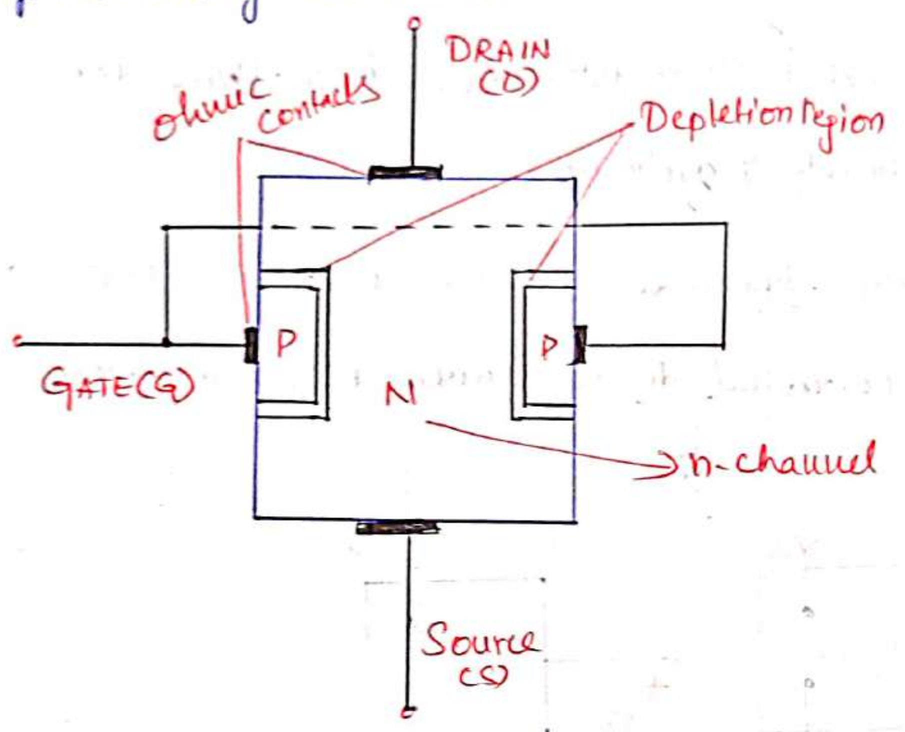


FIG: JFET CONSTRUCTION

* The major part of the JFET Consists of an N-type material that forms the Channel between the embedded layers of p-type material.
* Ohmic contacts are made at the two ends of N-type material forms the terminals Drain(D) and Source. The two p-type materials are Connected together to form the Gate(G) terminal.

SOURCE(S): This terminal is Connected to the negative pole of the battery. Electrons which are majority charge carriers in N-type enters through this terminal.

DRAIN(D): This terminal is connected to the positive pole of the battery. The majority charge carriers leaves from this terminal.

GATE(G): Heavily doped p-type silicon is diffused on both sides of the N-type silicon by which PN Junctions are formed. These layers are joined together and called the gate (G).

CHANNEL: The region in which the majority charge carriers move from source to drain when a potential difference V_{DS} is applied between the source and drain.

OPERATION:-

* When $V_{GS}=0V$ and $V_{DS}=0V$:

* In the absence of any applied potentials to the JFET, it has two P-N junctions under No-bias condition.

* The thickness of the depletion region around the PN junction is uniform.

2. When $V_{DS}=0V$ and V_{GS} is decreased from zero:

* In this case, the PN junctions are reverse biased and hence the thickness of the depletion region increases.

* As V_{GS} is decreased from zero, the reverse bias voltage across the PN junction is increased.

* Hence the thickness of the depletion region in the channel also increases until the two depletion regions make contact with each other. In this condition, the channel is said to be cut-off.

* The value of V_{GS} which is required to cut off the channel is called the cut-off voltage V_C.

3. When $V_{GS}=0$ and V_{DS} is increased from zero:

* Drain is positive with respect to the source with $V_{GS}=0$. Now the majority carriers (electrons) flow through the N-channel from source to drain.

* Therefore, the conventional current I_D flows from drain to source.

* The magnitude of the current will depend upon the following factors

1. The number of majority carriers (electrons) available in the channel i.e., the conductivity of the channel
2. The length L of the channel
3. The cross-sectional area A of the channel.
4. The magnitude of the applied voltage V_{DS}.

* Thus the channel acts as a resistor of resistance R given by,

$$R = \frac{\rho L}{A}$$

$$I = \frac{V_{DS}}{R} = \frac{V_{DS}}{\rho L/A} = \frac{A \cdot V_{DS}}{\rho L}$$

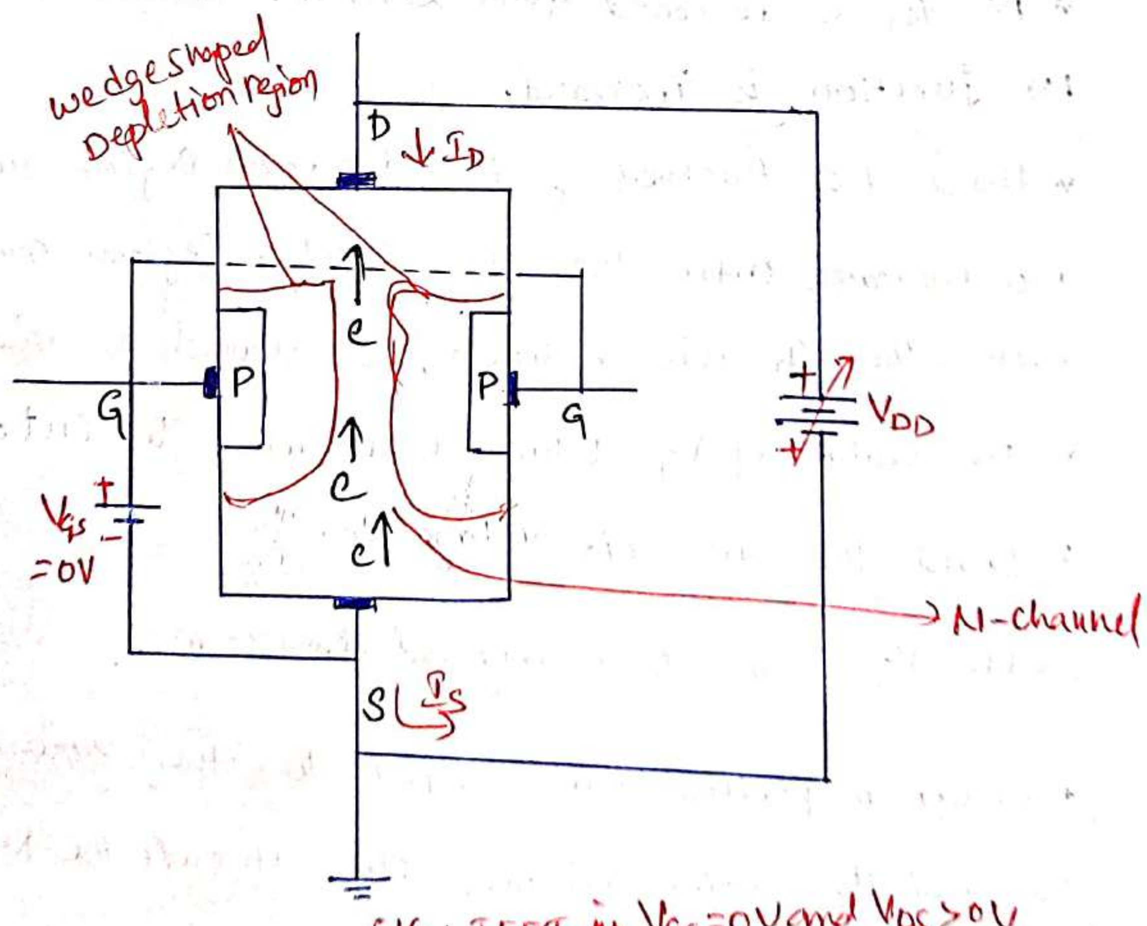


FIG: JFET in $V_{GS} = 0V$ and $V_{DS} > 0V$

* Because of the resistance of the channel and the applied Voltage V_{DS}, there is a gradual increase of potential along the channel from source to drain.

* Thus, the reverse Voltage across the PN junction increases and hence the thickness of depletion region also increases.

* Therefore, the channel is wedge shaped. As V_{DS} is increased, the cross-sectional area of the channel will be reduced. At a certain value of V_{DS} the cross sectional area of channel becomes minimum

* At this Voltage, the channel is said to be "pinched off" and the drain voltage is called pinch off Voltage (V_p).

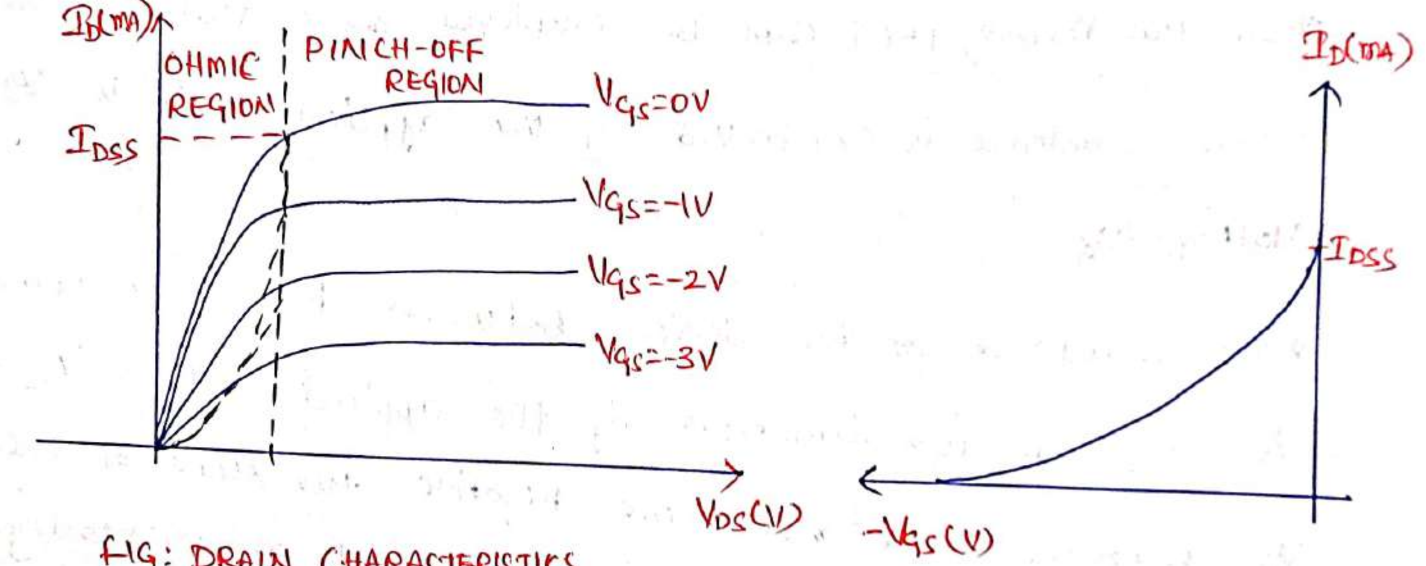


FIG: DRAIN CHARACTERISTICS

FIG: TRANSFER CHARACTERISTICS

* When the gate is maintained at a negative Voltage less than the negative cut-off Voltage, the reverse Voltage across the junction is further increased, Hence for a negative values of V_{GS} the curve of I_D Vs V_{DS} is similar to that for V_{GS} =0V.

* From the Curves, it is seen that above the pinch off Voltage, at a constant value of V_{DS}, I_D increases with an increase in V_{GS}.

* The expression for drain current is given by,

$$I_{DS} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

where I_{DS} is the saturation drain current

I_{DSS} is value of I_{DS} when $V_{GS} = 0$

V_P is the pinch-off voltage.

FET AS A VOLTAGE VARIABLE RESISTOR:

* The region left to the pinch-off region in drain characteristics curve is a ohmic region or voltage-controlled resistance region.

* In this region, JFET can be employed as a variable resistor whose resistance is controlled by the applied gate to source voltage (V_{GS}).

* The resistance of the device between drain and source for $V_{DS} < V_P$ is a function of the applied voltage V_{GS}. As V_{GS} becomes more and more negative the slope of each curve becomes more and more horizontal with an increasing resistance level.

TRANS-CONDUCTANCE (g_m):- The ratio of small change in drain current to the corresponding small change in the gate voltage at a constant drain voltage is called trans conductance (g_m)

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \Bigg|_{V_{DS}\ \text{Constant}} \qquad \text{Units: mhos } (\mho)$$

DRAIN RESISTANCE: The ratio of small change in drain voltage to the corresponding small change in the drain current at a constant gate voltage is called Drain resistance (r_d).

$$r_d = \frac{\Delta V_{DS}}{\Delta I_D} \Bigg|_{V_{GS}\ \text{Constant}} \qquad \text{Units: ohms } (\Omega)$$

AMPLIFICATION FACTOR (μ): The ratio of small change in the drain voltage to the corresponding small change in the gate voltage at a constant drain current.

$$\mu = \frac{\Delta V_{DS}}{\Delta V_{GS}} \Bigg|_{I_D\ \text{Constant}}$$

$$\boxed{\mu = g_m * r_d}$$

4B. BIASING THE FET

Need of Biasing :— (FET)

* For the proper functioning of a linear FET amplifier it is necessary to maintain the operating point 'Q' stable in the central portion of the pinch-off region.
* The 'Q' should be independent of device parameters Variation ~~Variations~~ and ambient temperature changes.
* For achieving proper amplification :—

In order to achieved proper amplification property to the transistor (FET) by suitably selecting the (V_{gs}) and drain current (I_D) i.e

Suitably selecting the operating point Q (V_{gs}, I_D) in the middle of the "Active region".

Fixing the Q-point :—

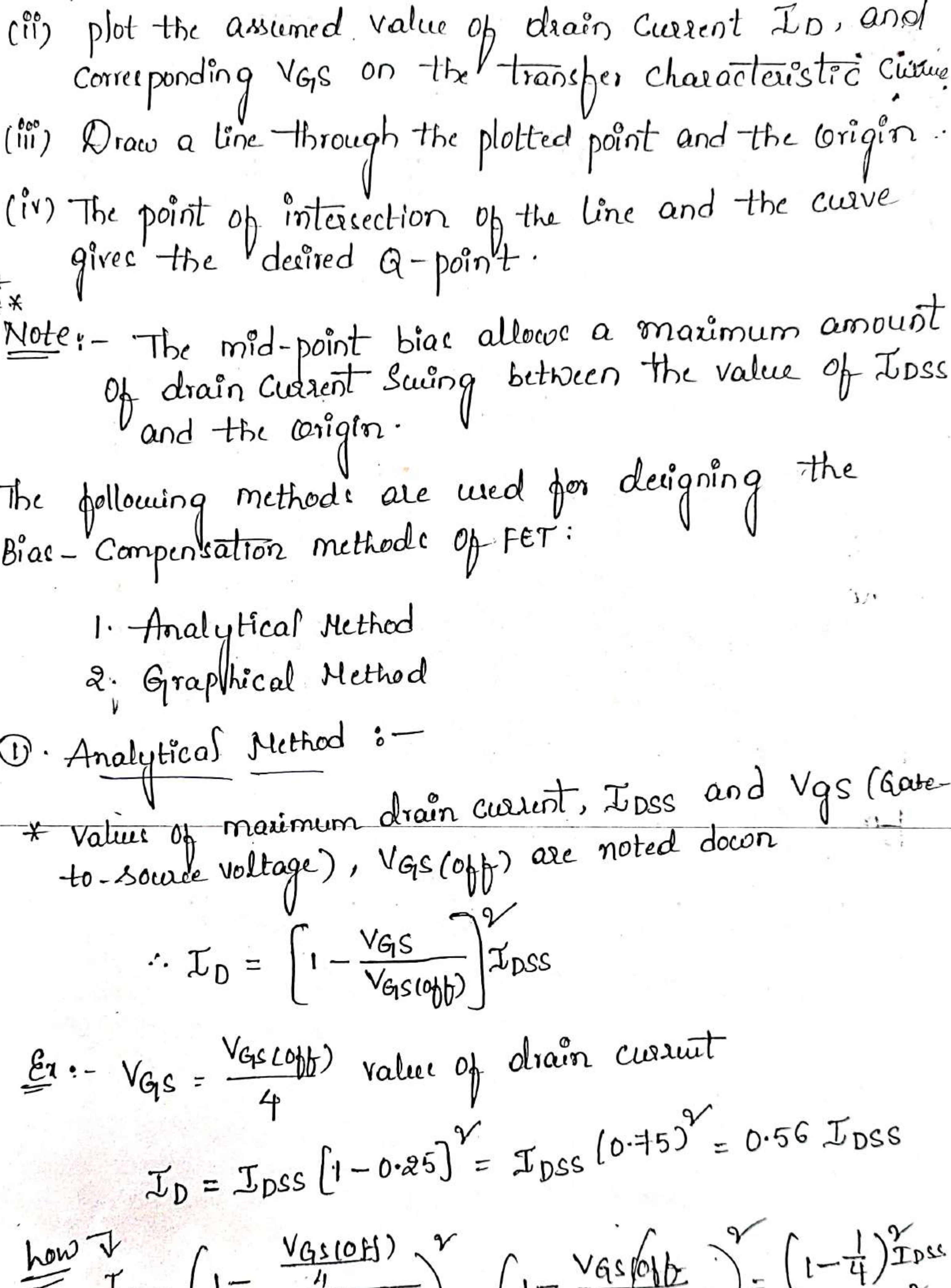
* The 'Q' point, (or) Quiescent point (or) operating point for a self-biased JFET is Established by determining the value of I_D (Drain current) for a desired value of V_{GS} (Gate-to-Source voltage).

procedure :—

i) * Select a Convenient value of drain current, whose value is generally taken as half of the maximum possible value of drain current I_{DSS},

Then find the $V_S = I_D \cdot R_S$

Gate Source Voltage $V_{GS} = -V_S$



(ii) plot the assumed value of drain current I_D, and corresponding V_{GS} on the transfer characteristic curve.

(iii) Draw a line through the plotted point and the origin.

(iv) The point of intersection of the line and the curve gives the desired Q-point.

Note:- The mid-point bias allows a maximum amount of drain current swing between the value of I_{DSS} and the origin.

The following methods are used for designing the Bias-Compensation methods of FET:

1. Analytical Method
2. Graphical Method

① Analytical Method :-

* Values of maximum drain current, I_{DSS} and V_{GS} (Gate-to-source voltage), $V_{GS(off)}$ are noted down

$$\therefore I_D = \left[1 - \frac{V_{GS}}{V_{GS(off)}}\right]^2 I_{DSS}$$

Ex:- $V_{GS} = \frac{V_{GS(off)}}{4}$ value of drain current

$$I_D = I_{DSS}\left[1 - 0.25\right]^2 = I_{DSS}(0.75)^2 = 0.56\, I_{DSS}$$

how ↓

$$I_D = \left(1 - \frac{\frac{V_{GS(off)}}{4}}{V_{GS(off)}}\right)^2 = \left(1 - \frac{V_{GS(off)}}{4(V_{GS(off)})}\right)^2 = \left(1 - \frac{1}{4}\right)^2 I_{DSS}$$

$$= (1 - 0.25)^2 I_{DSS}$$

$$I_D = 0.56\, I_{DSS}$$

Here, the drain current is slightly more than one-half of I_{DSS} ($\because I_D = 0.56 I_{DSS} \approx \frac{1}{2} I_{DSS}$) or

i.e The value of drain resistor, R_D, is selected in such a way that - the drain voltage V_D is equal to half the drain supply voltage R_D.

(and R_G must be large).

(2) Graphical Method :—

* A self-bias line is drawn such that it intersects the transfer characteristic curve near its mid-point gives the required Q-point.
* The value of source resistance, R_S is expressed by the ratio of gate to source voltage, V_{GS} to the drain current I_D.

$$R_S = \frac{V_{GS}}{I_D}$$

I_D

Exactly mid point 'Q'. (operating point)

$Q(V_{GSQ}, I_{DQ})$.

V_{GS} (negative)

Q

fig:— V_{GS} Vs I_D transfer characteristic

The Source Resistance $\left(R_S = \frac{V_{GS(off)}}{I_{DSS}} \right)$.

Fixed bias :-

* The following figure shows the fixed bias circuit for the n-Channel JFET.
* This is simplest biasing arrangement
* To make gate-Source junction reverse-biased, a Separate supply V_{GG} is Connected such that gate is more negative than the Source.

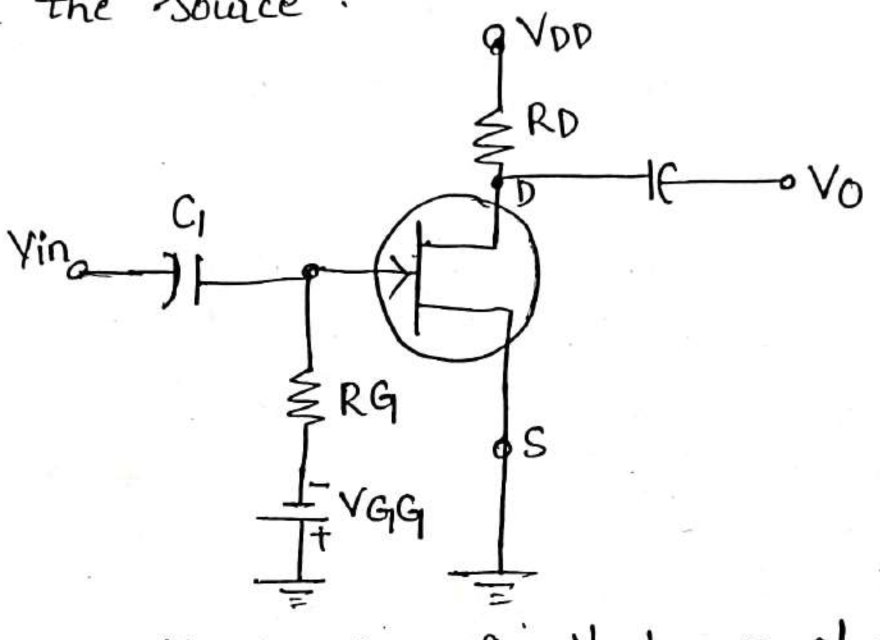


Fig: fixed bias circuit for n-channel circuit.

D.C Analysis :-

For the d.c analysis coupling Capacitors are open Circuit. The current through R_G is I_G which is zero. This permits R_G to replace by short circuit, simplifying the fixed bias circuit.

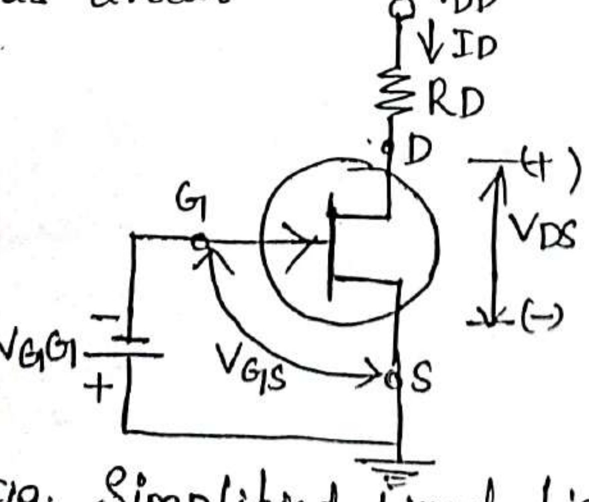


Fig: Simplified fixed bias Circuit.

We know for d.c analysis

$$I_G = 0A$$

Applying KVL to the input circuit we get

$$V_{GS} + V_{GG} = 0$$

$$V_{GS} = -V_{GG}$$

For fixed bias circuit the drain current I_D can be calculated using

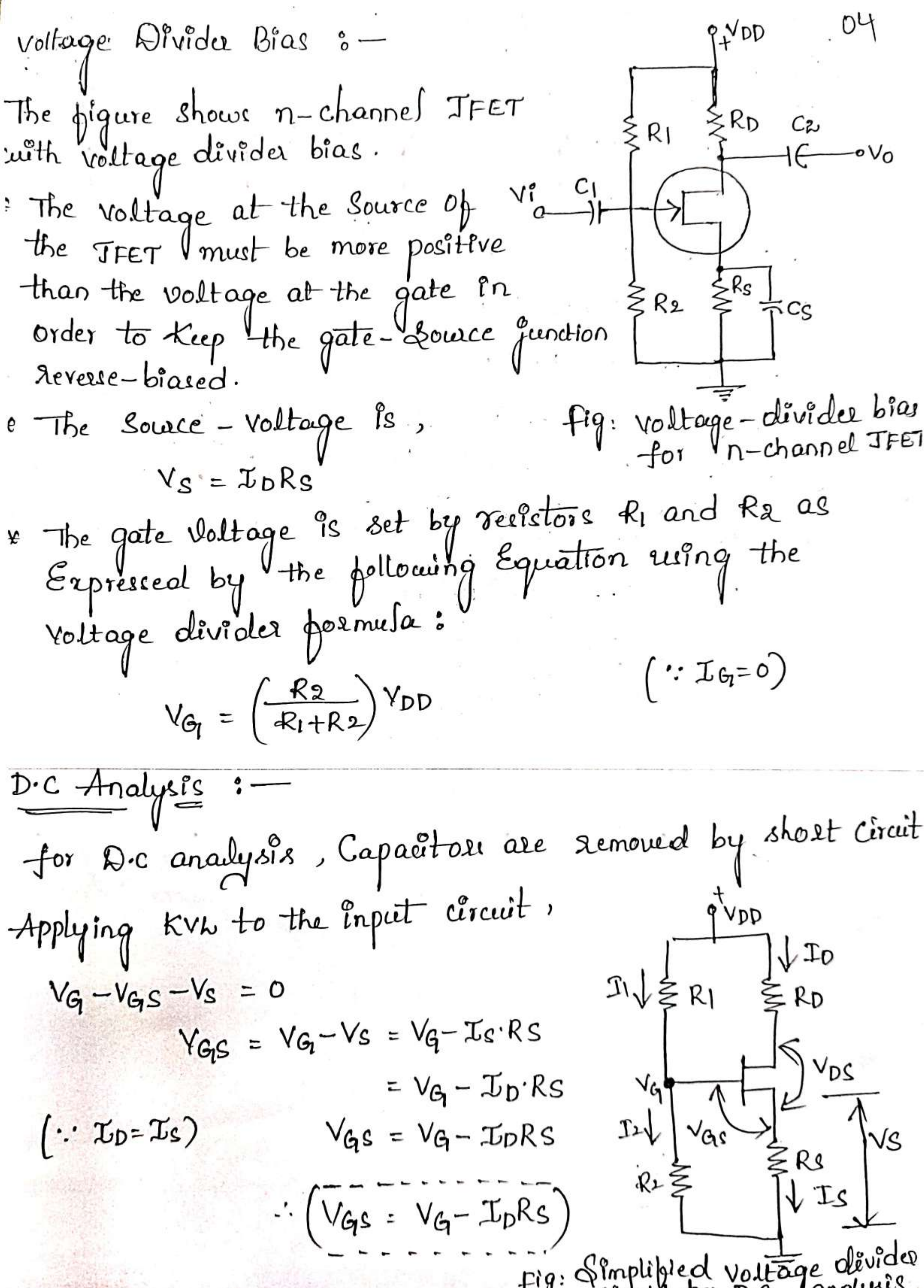
$$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

The Drain-to-Source voltage of output circuit can be determined by applying KVL to output

$$V_{DD} = V_{DS} + I_D R_D$$

$$V_{DS} = V_{DD} - I_{DQ} \cdot R_D$$

//.



Voltage Divider Bias :—

The figure shows n-channel JFET with voltage divider bias.

- The voltage at the Source of the JFET must be more positive than the voltage at the gate in order to Keep the gate-Source junction reverse-biased.

fig: voltage-divider bias for n-channel JFET

- The Source-voltage is,

$$V_S = I_D R_S$$

- The gate voltage is set by resistors R_1 and R_2 as Expressed by the following Equation using the voltage divider formula:

$$V_G = \left(\frac{R_2}{R_1+R_2}\right) V_{DD} \qquad (\because I_G = 0)$$

D.C Analysis :—

for D.C analysis, Capacitors are removed by short circuit

Applying KVL to the input circuit,

$$V_G - V_{GS} - V_S = 0$$

$$V_{GS} = V_G - V_S = V_G - I_S \cdot R_S$$

$$= V_G - I_D \cdot R_S$$

$$(\because I_D = I_S) \qquad V_{GS} = V_G - I_D R_S$$

$$\therefore \boxed{V_{GS} = V_G - I_D R_S}$$

fig: Simplified voltage divider circuit for D.C analysis

Applying KVL to the operating output, we get

$$V_{DS} + I_D R_D + V_S - V_{DD} = 0$$

$$V_{DD} = V_{DS} + I_D R_D + V_S$$

$$V_{DS} = V_{DD} - I_D R_D - V_S$$

$$V_{DS} = V_{DD} - I_D R_D - I_S R_S \quad (\because I_S = I_D)$$

$$V_{DS} = V_{DD} - I_D R_D - I_D R_S$$

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

$\therefore$ The Q-point of a JFET amplifier using the voltage-divider bias is given by,

$$I_{DQ} = I_{DSS}\left[1 - \frac{V_{GS}}{V_P}\right]^2$$

$$V_{DSQ} = V_{DD} - I_D (R_D + R_S)$$

Self-Bias Circuit :-

* Self-bias is the most common-type of JFET bias.
* JFET must be operated as gate-source junction is always reverse-biased.
  This condition requires a negative V_{GS} for an n-channel and a positive V_{GS} for p-channel.
* This can be achieved by using self-bias circuit.
* If $V_G = 0V$ then also the JFET able to flow current so it is called as "self-bias".
* The circuit for self bias is shown below :-

(a) Self-bias circuit for N-channel JFET

(b) Self-bias circuit for p-channel JFET.

* For the n-channel FET, I_S produces a voltage drop across R_S and make the source positive with respect to ground.

  Since $I_S = I_D$ and $V_G = 0$, then

$$V_{GS} = V_G - V_S = 0 - I_D R_S = -I_D \cdot R_S$$

$$\boxed{V_{GS} = -I_D R_S}$$

DC Analysis :—

For D.C analysis we can replace coupling capacitors by open circuit and we can also replace the resistor R_G by a short circuit equivalent.

Since $I_G = 0$. This is illustrated in fig below

fig:— Simplified self-bias circuit for d.c analysis.

We know,
$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Sub V_{GS} in the equation we get

$$I_D = I_{DSS}\left(1 - \frac{-I_D R_S}{V_P}\right)^2 = I_{DSS}\left(1 + \frac{I_D R_S}{V_P}\right)^2 \rightarrow (1).$$

$$\boxed{I_{DQ} = I_{SS}\left(1 + \frac{I_D R_S}{V_P}\right)^2} \rightarrow (2)$$

Apply KVL to output circuit,

$$V_{DD} = I_D R_D + V_{DS} + V_S$$

$$V_{DS} = V_{DD} - V_S - I_D R_D = V_{DD} - I_D R_S - I_D R_D$$

$$= V_{DD} - I_D(R_S + R_D)$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

$$\therefore \boxed{V_{DSQ} = V_{DD} - I_D(R_S + R_D)}$$

MOS FIELD EFFECT TRANSISTORS [MOSFETS]

* Metal oxide field effect transistor is the common term for the Insulated Gate field effect transistor (IGFET).

* There are two basic forms of MOSFET
  1. Depletion MOSFET
  2. Enhancement MOSFET

N-CHANNEL DEPLETION MODE MOSFET:

CONSTRUCTION :-

* The basic construction of the n-channel depletion type MOSFET consists of, a slab of p-type material is formed from a silicon base and is referred to as the substrate.
* The source and drain terminals are connected through the metallic contacts to heavily doped two n+ regions linked by a n-channel.
* The gate is also connected to a metal contact surface but remains insulated from the channel by a very thin Silicon dioxide (SiO_2) layer.
* In some cases the substrate(ss) is internally connected to the source terminal resulting in forming a four terminals.
* There is no direct electrical connection between the gate terminal and the channel of a MOSFET.

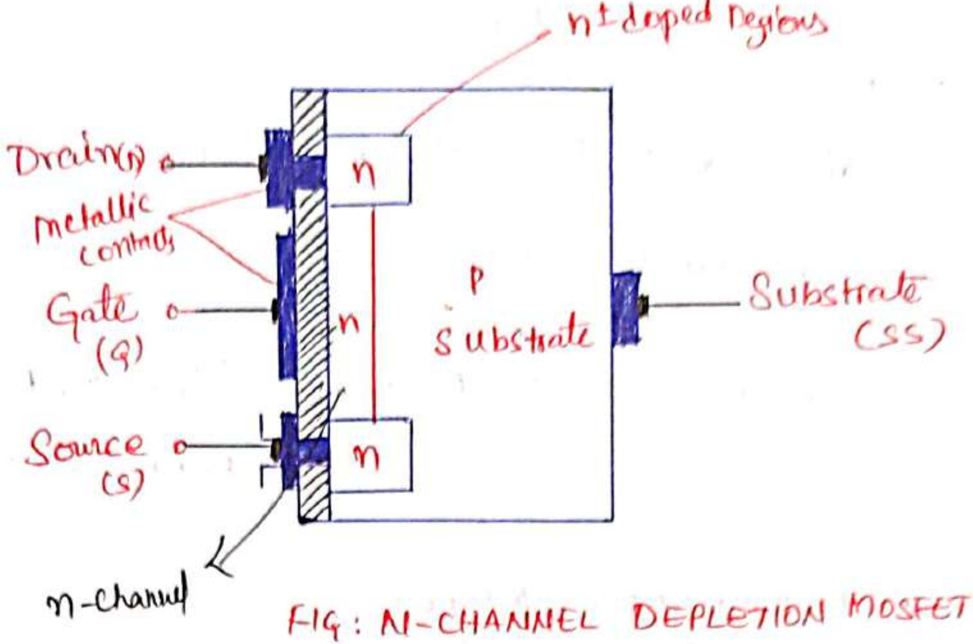
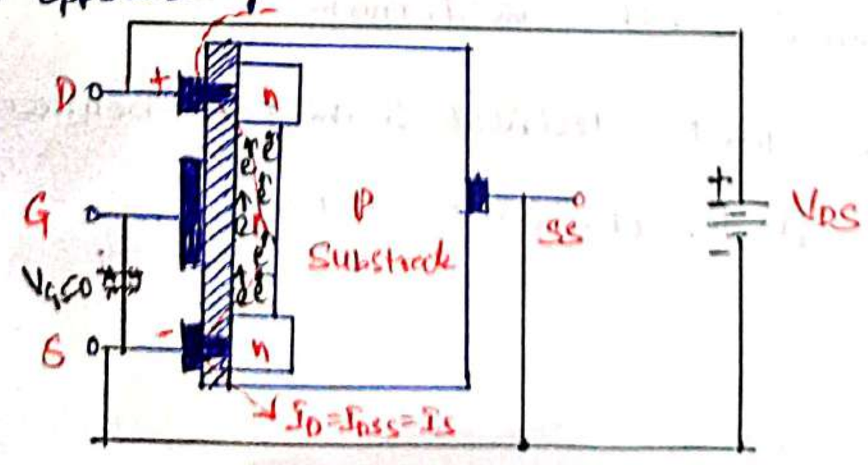


FIG: N-CHANNEL DEPLETION MOSFET

OPERATION :-

1. $V_{GS} = 0V$ & $V_{DS} > 0V$

* When the applied voltage b/n gate and source i.e., V_{GS} is 0 V and a voltage V_{DS} is applied across the drain to source terminals
* The positive terminal is connected to drain because of this the free electrons present in the n-channel gets attracted towards the drain terminal.
* Due to this there will be a current between source to drain which is I_{DSS} when $V_{GS} = 0V$.
* The electrons moves from source to drain the conventional current is opposite of it.



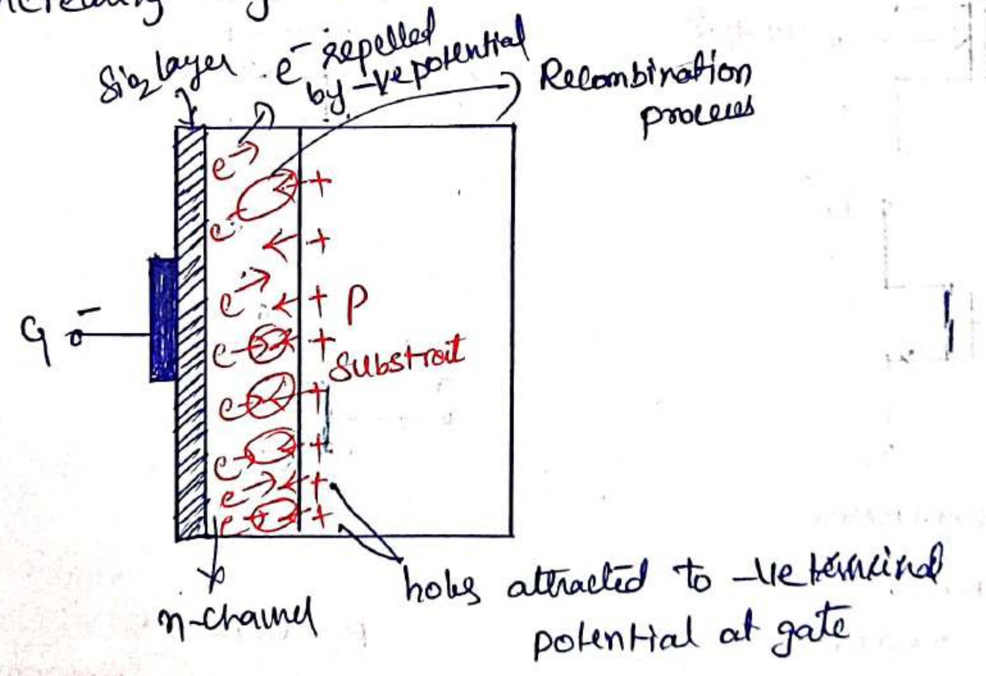
2. V_{GS} is negative:

* When the applied voltage between gate and source (V_{GS}) is negative, the negative potential at the gate will tend to pressure the electrons toward the p-type substrate and attract holes from the p-type substrate.

* Depending upon the magnitude of V_{GS}, a level of recombination of electrons and holes will occur that will reduce the number of free electrons in the channel for conduction.

* The more negative the bias, the higher rate of recombination thus the resulting level of drain current is therefore reduced with increasing negative bias for V_{GS} and channel gets pinched off.

*



* The drain and transfer characteristics of n-channel depletion MOSFET is shown below.

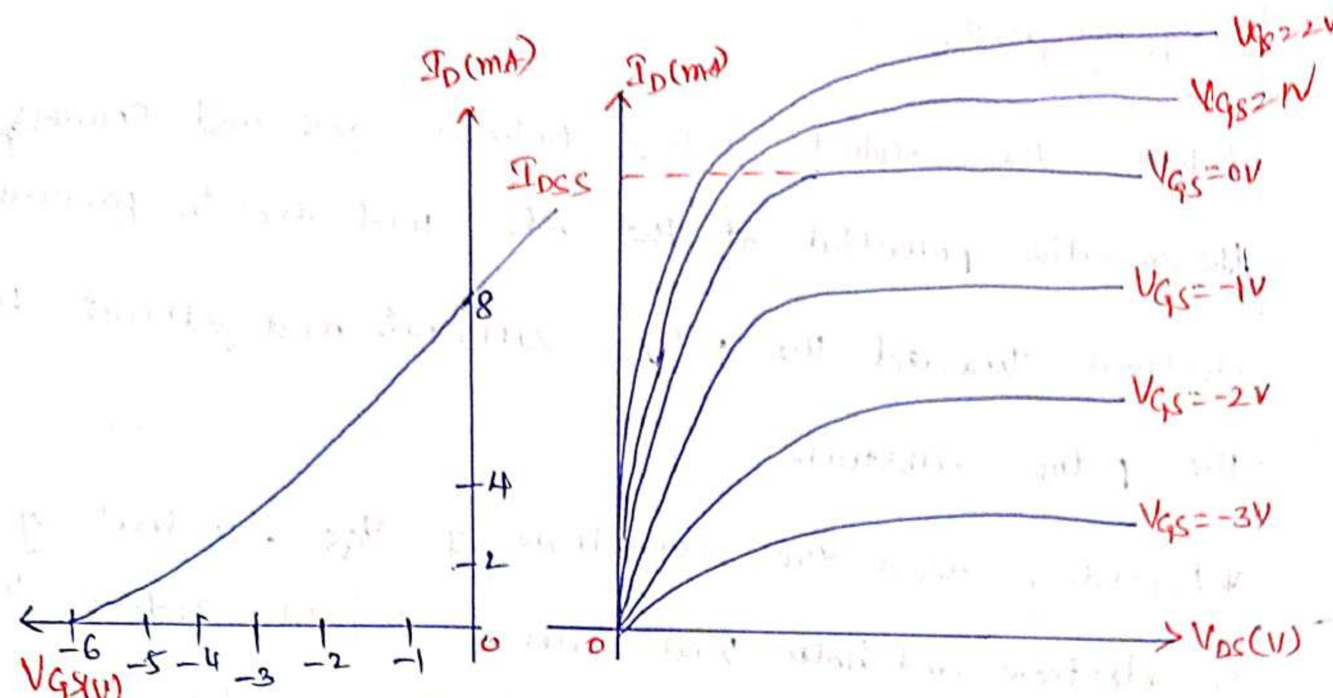
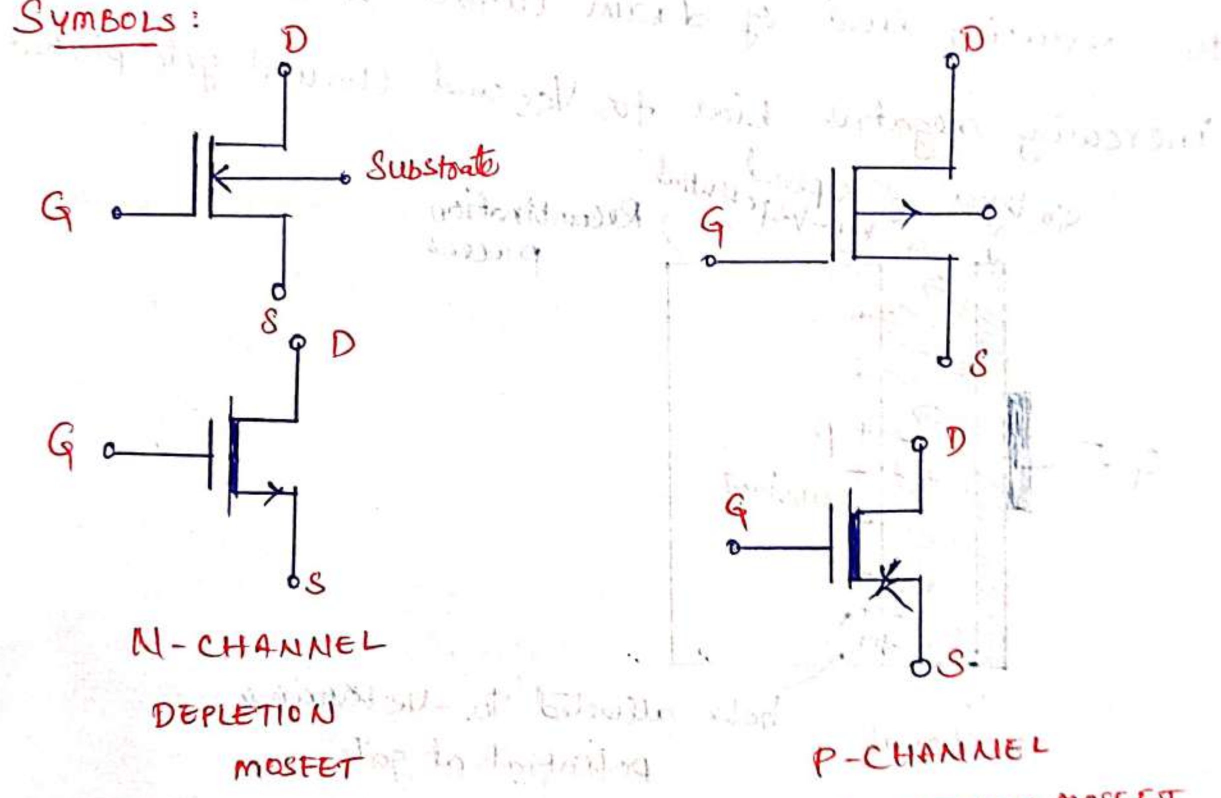


FIG: DRAIN AND TRANSFER CHARACTERISTICS

SYMBOLS:



N-CHANNEL DEPLETION MOSFET

P-CHANNEL DEPLETION MOSFET

N-CHANNEL ENHANCEMENT MODE MOSFET:

* Although there are some similarities in construction and mode of operation between depletion type and enhancement MOSFETS but the characteristics are quite different.

CONSTRUCTION:

* The basic construction of the n-channel enhancement mode MOSFET consists of, a p-type slab is formed from a silicon base and is reffered as substrate.
* The source and drain terminals are connected through a metallic contacts to heavily doped two n+ regions.
* Unlike depletion mode, there is no presence of physical channel between the two n regions.
* This is the primary difference between the construction of depletion type and enhancement type MOSFETS- the absence of the channel as a constructed component of the device.
* The gate is also connected to a metal contact surface but remains isolated from a very thin silicon dioxide layer.

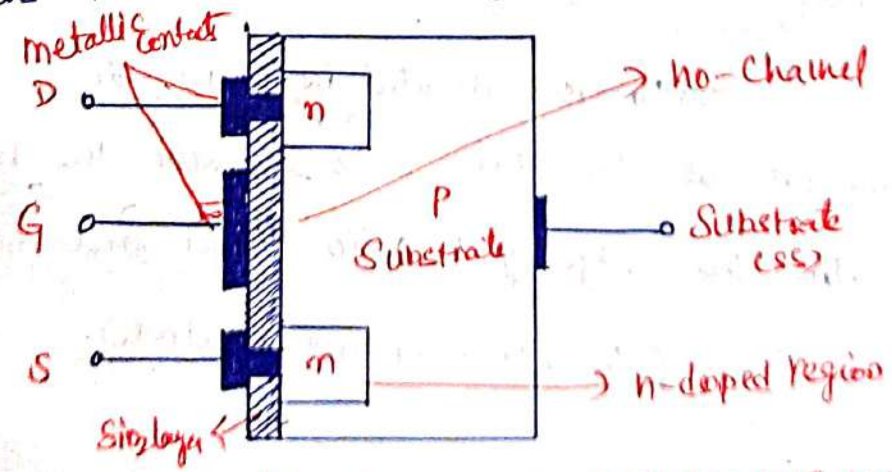


FIG: N-CHANNEL ENHANCEMENT MODE MOSFET

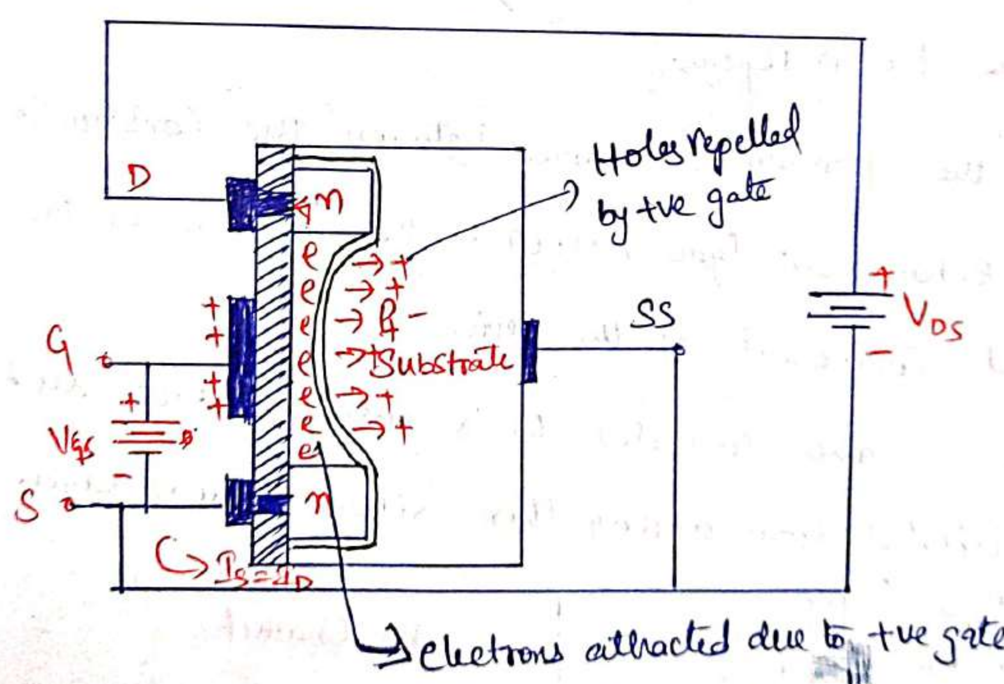
OPERATION :-

$V_{GS} = 0V$ & $V_{DS} > 0V$

* When the applied voltage between gate and source $V_{GS} = 0V$ and a voltage is applied between source and drain V_{DS}, since there is no presence of channel the drain current will be zero.
* Because there is no conduction path for the electrons to move from source to drain.

$V_{GS} > 0V$ & $V_{DS} > 0V$

* If both V_{GS} and V_{DS} have been set at some positive voltage greater than 0V, establishing the drain and gate at a positive potential with respect to the source.



* The positive potential at the gate will pressure the holes in the p-substrate along the edge of the SiO_2 layer and enter deeper regions of the p-substrate (to bottom of the substrate).

* The minority charge carriers i.e., electrons in the p-substrate will be attracted to the positive gate and accumulate in the region near the surface of the SiO_2 layer

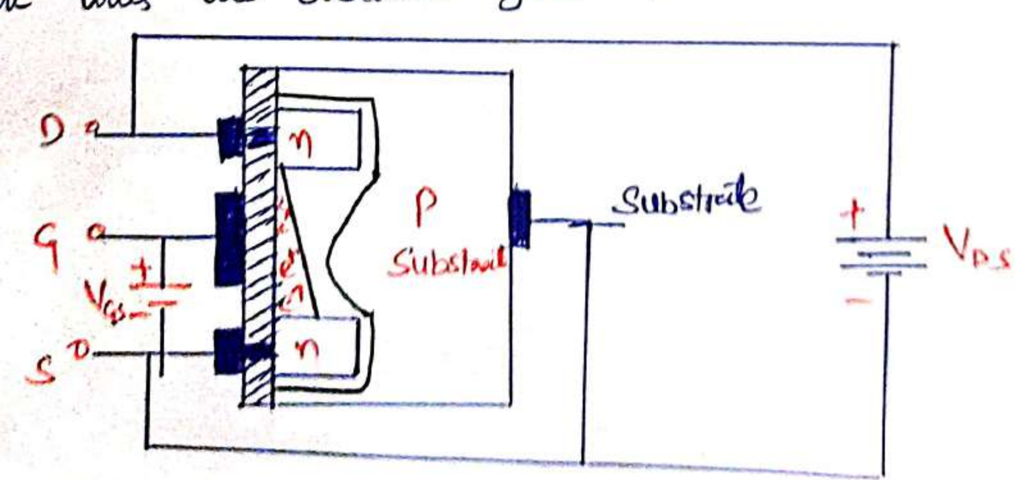
* As the magnitude of V_{GS} increases, the concentration of electrons near the SiO_2 surface increases eventually the n-type channel gets induced between drain and source. The corresponding voltage of V_{GS} is called threshold voltage V_t.

* Since the channel is nonexistent with $V_{GS} = 0V$ and enhanced by the application of a positive gate to source voltage this type of MOSFET is called Enhancement mode MOSFET.

* As V_{GS} is increased beyond the threshold level, the density of free carriers induced in the channel will increase resulting in increasing of drain current.

* If we hold V_{GS} constant and increase the level of V_{DS} the drain current will eventually reach a saturation level.

* When V_{DS} is increased beyond the $V_{GS} - V_t$, the depletion region occupies the area of the channel and becomes narrower near the drain thus the channel gets pinched off near the drain.



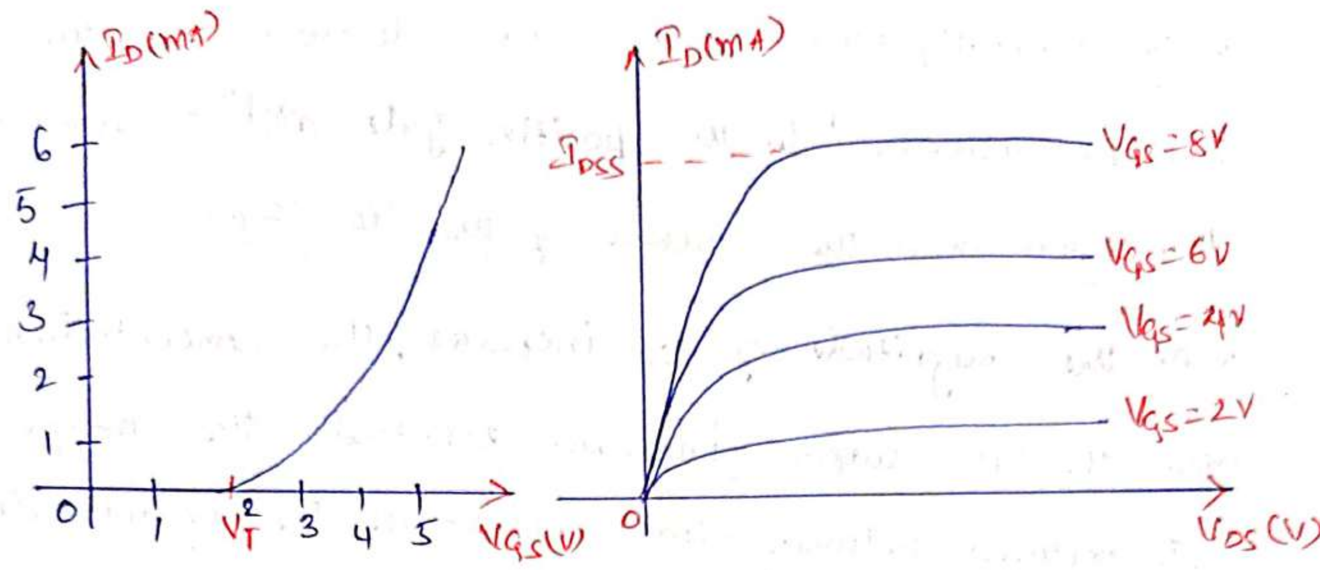
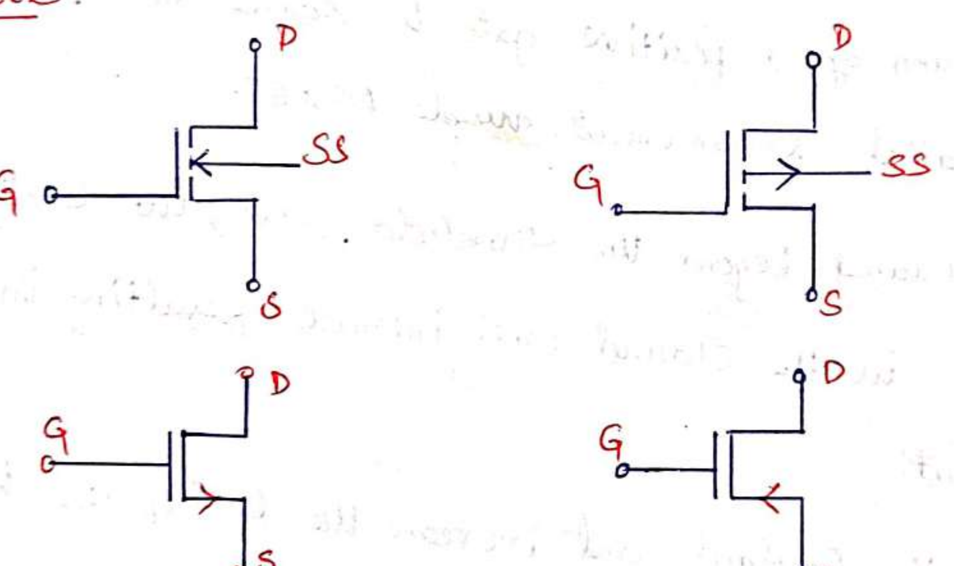


FIG: TRANSFER AND DRAIN CHARACTERISTICS OF N-CHANNEL ENHANCEMENT MOSFET

SYMBOLS:



N-CHANNEL E-MOSFET

P-CHANNEL E-MOSFET

BIASING IN MOS AMPLIFIER CIRCUITS :-

* An essential step in the design of a MOSFET amplifier circuit is the establishment of an appropriate dc operating point for the transistor.

* This step is known as biasing or bias design. An appropriate dc operating point or bias point is characterized by a stable and predictable dc current gain I_D and by a dc drain-to-source voltage V_{DS} that ensures the operation in the saturation region for all expected input signal levels.

* The Biasing techniques are,
    1. By fixing V_{GS}
    2. By fixing V_G and connecting a feedback resistance to the Source
    3. Using a Constant Current Source.

1. BIASING BY FIXING V_{GS} :

* The simplest approach to biasing a MOSFET to get desired is to fix its gate-to-source voltage V_{GS} to get the desired value I_D.

* This voltage (V_{GS}) value can be derived from the power supply voltage V_{DD} through the use of an appropriate voltage divider.

* Alternatively it can be derived from another suitable reference voltage that might be available in the system.

* Independent of how this voltage V_{GS} may be generated, this is not a good approach to biasing a MOSFET.

we know that $I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t)^2$

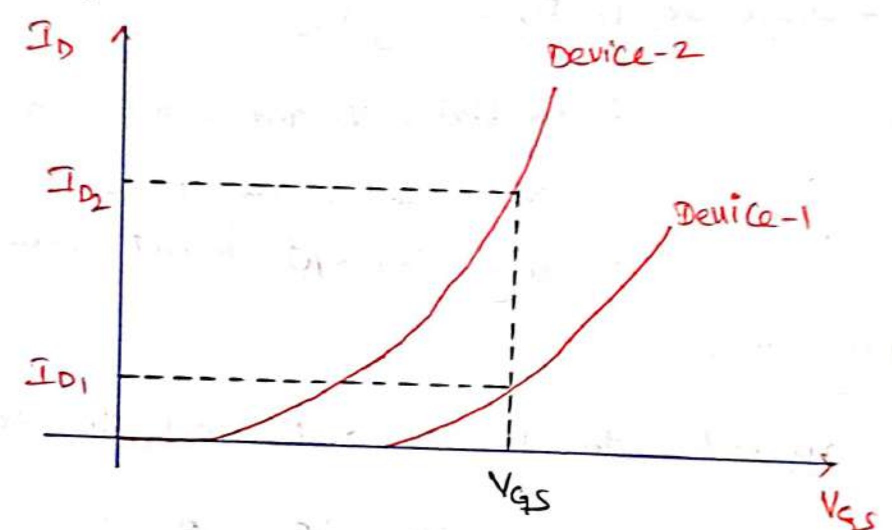
where V_t – Threshold value

C_{ox} – Oxide capacitance

$\frac{W}{L}$ – transistor aspect ratio

* The values of $\frac{W}{L}$, C_{ox} is not same for any same transistors because they are manufacture dependent.

* Furthermore, V_t, and μ_n depend on temperature, with result if we fix the value of V_{GS}, the current I_D becomes very much temperature dependent.



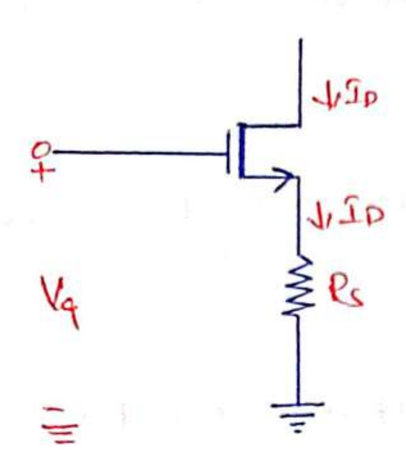
* The I_d Vs V_{GS} Characteristic curves representing extreme values in a batch of MOSFET's of the same type.

* Observe that for the fixed value of V_{GS}, the resultant spread in the values of the drain current can be substantial.

2. BIASING BY FIXING V_G AND CONNECTING A RESISTANCE IN THE SOURCE:

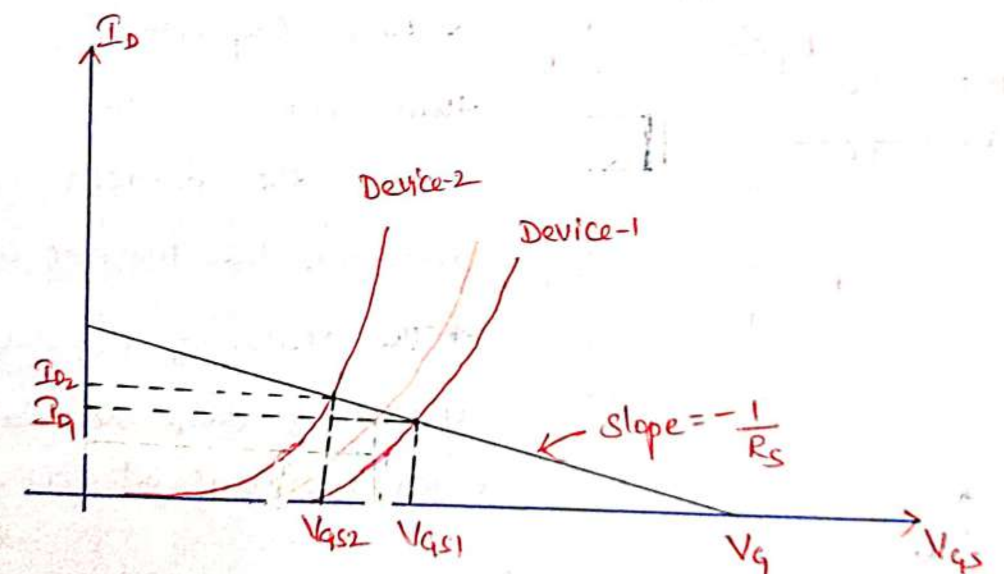
* An excellent biasing technique for discrete MOSFET circuits consist of fixing the dc voltage(V_G) at the gate and connecting a resistance in the source lead.

$$V_G = V_{GS} + R_S I_D \rightarrow (1)$$



* Now, if V_G is much greater than V_{GS}, I_D, will be determined by the values of V_G and R_S.
* However if V_G is not much larger than V_{GS}, resistor R_S provides negative feedback, which acts to stabilize the value of bias current I_D.

* Let us consider a case when I_D increases for whatever reason. From the equation ①, it indicates that since V_G is constant, V_{GS} will have to decrease, this in turn results in a decrease in I_D. A change that is opposite to that initially assumed.
* Thus the action of R_S works to keep I_D as constant as possible. This negative feedback action of R_S gives it the name degeneration resistance.



* The graphical illustration of the effectiveness of this biasing scheme. The i_D-V_{GS} characteristics is a straight line that represents the constraint imposed by the bias circuit.
* The intersection of this straight line with the i_D-V_{GS} characteristics curve provides the coordinates (I_D and V_{GS}) of the bias point.

* Observe that compared to the case of fixed V_{GS}, here the variability obtained in I_D is much smaller.

* Two possible practical discrete implementations of this bias scheme are as follows,

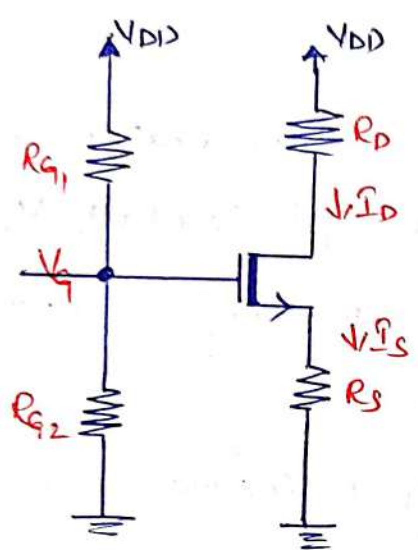
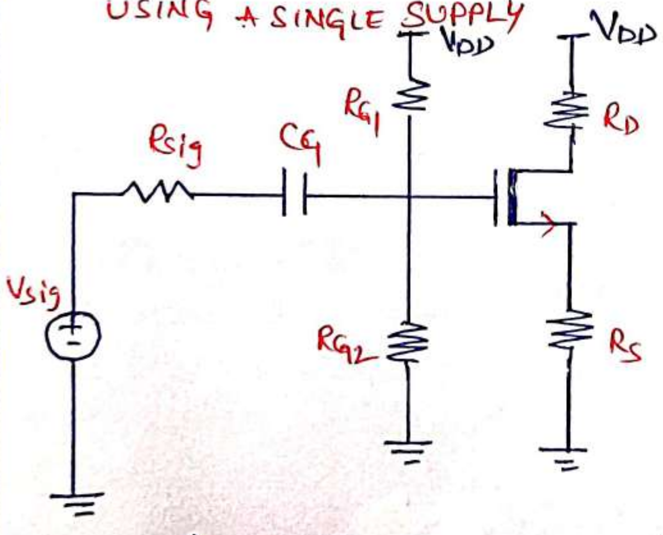
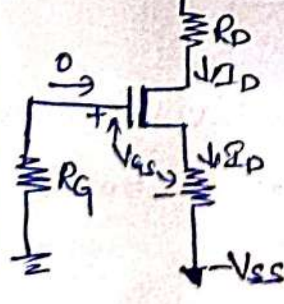


FIG: PRACTICAL IMPLEMENTATION USING A SINGLE SUPPLY

* This circuit utilizes one power supply V_{DD} and derives V_G through a voltage divider (R_{G1}, R_{G2}). Since $I_G = 0$, R_{G1} and R_{G2} can be selected to be very large (in MΩ ranges) allowing MOSFET to present a ~~long~~ large input resistance to a signal source that may be connected to the gate through a coupling capacitor.



* Here capacitor C_{C1} blocks dc and thus allows us to couple the signal V_{sig} to the amplifier input without disturbing the MOSFET dc bias point.
* The value of C_{C1} should be selected sufficiently large so that it approximates a short circuit at all signal frequencies.



* This circuit is an implementation of eq ① with V_G replaced by V_{SS}. Resistor R_G establishes a dc ground at the gate and presents a high input resistance to a signal that may be connected to the gate through a coupling capacitor.

4.5.3 Biasing Using a Drain-to-Gate Feedback Resistor

A simple and effective discrete-circuit biasing arrangement utilizing a feedback resistor connected between the drain and the gate is shown in Fig. 4.32. Here the large feedback resistance R_G (usually in the MΩ range) forces the dc voltage at the gate to be equal to that at the drain (because $I_G = 0$). Thus we can write

$$V_{GS} = V_{DS} = V_{DD} - R_D I_D$$

which can be rewritten in the form

$$V_{DD} = V_{GS} + R_D I_D \tag{4.49}$$

which is identical in form to Eq. (4.46), which describes the operation of the bias scheme discussed above [that in Fig. 4.30(a)]. Thus, here too, if I_D for some reason changes, say increases, then Eq. (4.49) indicates that V_{GS} must decrease. The decrease in V_{GS} in turn causes a decrease in I_D, a change that is opposite in direction to the one originally assumed. Thus the negative feedback or degeneration provided by R_G works to keep the value of I_D as constant as possible.

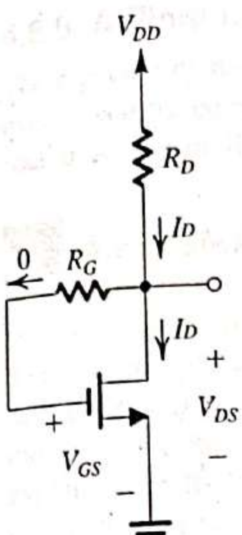


FIGURE 4.32 Biasing the MOSFET using a large drain-to-gate feedback resistance, R_G.

The circuit of Fig. 4.32 can be utilized as a CS amplifier by applying the input voltage signal to the gate via a coupling capacitor so as not to disturb the dc bias conditions already established. The amplified output signal at the drain can be coupled to another part of the circuit, again via a capacitor. We shall consider such a CS amplifier circuit in Section 4.6. There we will learn that this circuit has the drawback of a rather limited output voltage signal swing.

EXERCISE

D4.21 It is required to design the circuit in Fig. 4.32 to operate at a dc drain current of 0.5 mA. Assume V_{DD} = +5 V, $k_n'W/L = 1\ \text{mA/V}^2$, $V_t = 1$ V, and $\lambda = 0$. Use a standard 5% resistance value for R_D, and give the actual values obtained for I_D and V_D.

Ans. $R_D = 6.2\ \text{k}\Omega$; $I_D \cong 0.49$ mA; $V_D \cong 1.96$ V

4.5.4 Biasing Using a Constant-Current Source

The most effective scheme for biasing a MOSFET amplifier is that using a constant-current source. Figure 4.33(a) shows such an arrangement applied to a discrete MOSFET. Here R_G (usually in the MΩ range) establishes a dc ground at the gate and presents a large resistance to an input signal source that can be capacitively coupled to the gate. Resistor R_D establishes an appropriate dc voltage at the drain to allow for the required output signal swing while ensuring that the transistor always remains in the saturation region.

A circuit for implementing the constant-current source I is shown in Fig. 4.33(b). The heart of the circuit is transistor Q_1, whose drain is shorted to its gate and thus is operating in the saturation region, such that

$$I_{D1} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_1(V_{GS} - V_t)^2 \tag{4.50}$$

where we have neglected channel-length modulation (i.e., assumed $\lambda = 0$). The drain current of Q_1 is supplied by V_{DD} through resistor R. Since the gate currents are zero,

$$I_{D1} = I_{\text{REF}} = \frac{V_{DD} + V_{SS} - V_{GS}}{R} \tag{4.51}$$

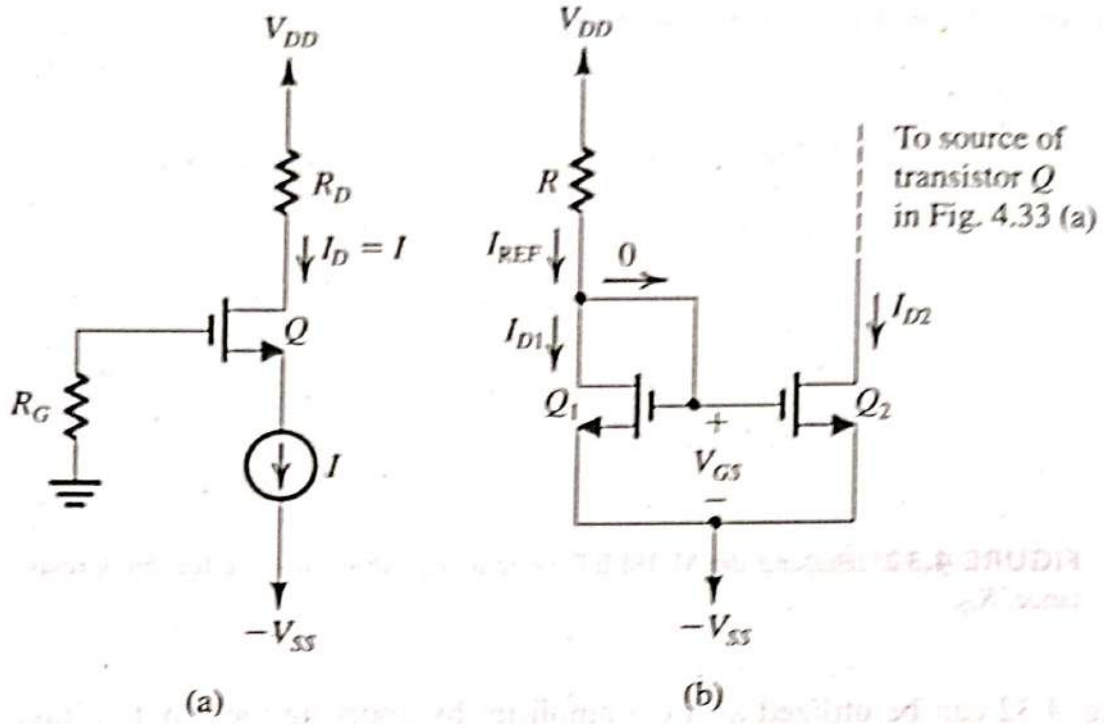


FIGURE 4.33 (a) Biasing the MOSFET using a constant-current source I. (b) Implementation of the constant-current source I using a current mirror.

where the current through R is considered to be the *reference current* of the current source and is denoted I_{REF}. Given the parameter values of Q_1 and a desired value for I_{REF}, Eqs. (4.50) and (4.51) can be used to determine the value of R. Now consider transistor Q_2: It has the same V_{GS} as Q_1; thus if we assume that it is operating in saturation, its drain current, which is the desired current I of the current source, will be

$$I = I_{D2} = \frac{1}{2}k_n'\left(\frac{W}{L}\right)_2 (V_{GS} - V_t)^2 \tag{4.52}$$

where we have neglected channel-length modulation. Equations (4.51) and (4.52) enable us to relate the current I to the reference current I_{REF},

$$I = I_{REF}\frac{(W/L)_2}{(W/L)_1} \tag{4.53}$$

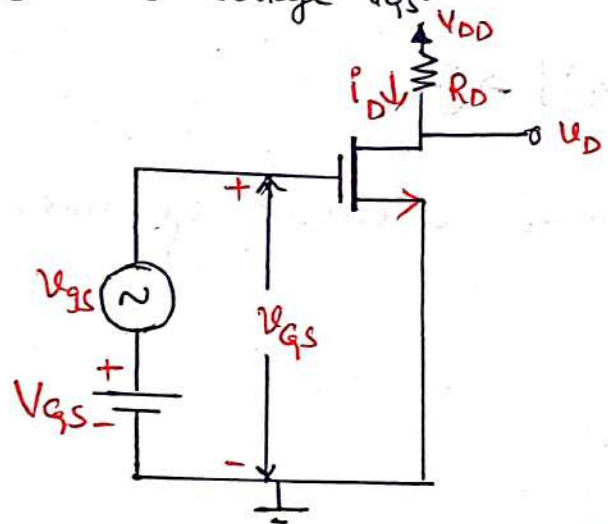
Thus I is related to I_{REF} by the ratio of the aspect ratios of Q_1 and Q_2. This circuit, known as a **current mirror,** is very popular in the design of IC MOS amplifiers and will be studied in great detail in Chapter 6.

MOSFET SMALL SIGNAL OPERATION MODELS

* In small signal analysis one assumes that the device is biased at a DC operating point and then a small signal is superimposed on the DC biasing point.

The DC Bias point:

* Here the MOS transistor is biased by applying a dc voltage V_{GS}. The input signal to be amplified v_{gs} is shown superimposed on the dc bias voltage V_{GS}.



* From the circuit v_{gs} → ac voltage, i_d → ac current
  V_{GS} → dc voltage, I_D → dc current
  v_{GS} → Total voltage, i_D → total current

total voltages $v_{GS} = v_{gs} + V_{GS}$ → (1)

total current $i_D = i_d + I_D$ → (2)

* The dc bias current is given by

$$I_D = \frac{1}{2} K_n \frac{W}{L} (V_{GS} - V_t)^2 \rightarrow (3)$$

* The total Current is

$$i_D = \frac{1}{2} k_n \frac{W}{L} ((V_{GS} + v_{gs}) - V_t)^2$$

$(\because (a+b-c)^2 = a^2+b^2+c^2+2ab - 2bc - 2ca)$

$$i_D = \frac{1}{2} k_n \frac{W}{L} (V_{GS}^2 + v_{gs}^2 - V_t^2 + 2 V_{GS} v_{gs} - 2 v_{gs} V_t - 2 V_t V_{GS})$$

* In the above expressions ac components are

$$i_d = \frac{1}{2} k_n \frac{W}{L} (2 V_{GS} v_{gs} - 2 v_{gs} V_t)$$

$$i_d = \frac{1}{2} k_n \frac{W}{L} [2 v_{gs} (V_{GS} - V_t)]$$

$$i_d = k_n \frac{W}{L} [v_{gs} (V_{GS} - V_t)] \rightarrow (4)$$

* The eq (4) is the expression for ac current in small signal model of MOSFET.

TRANSCONDUCTANCE:

* The transconductance g_m is given by

$$g_m = \frac{i_d}{v_{gs}}$$

$(\because i_d = k_n \frac{W}{L} (v_{gs}(V_{GS} - V_t)]$ for small signal model)

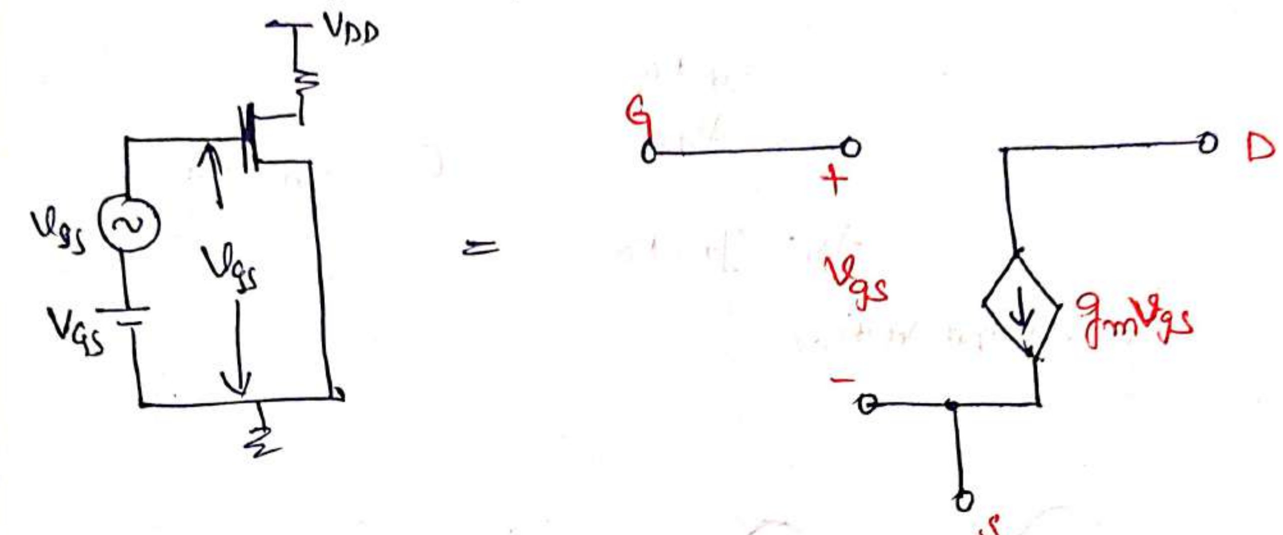
$$= \frac{k_n \frac{W}{L} [v_{gs} (V_{GS} - V_t)]}{v_{gs}}$$

$$g_m = k_n \frac{W}{L} (V_{GS} - V_t)$$

$$\boxed{g_m = k_n \frac{W}{L} (V_{G} - V_t)}$$

SMALL-SIGNAL EQUIVALENT CIRCUIT MODELS:

* In the analysis of a MOSFET amplifier circuit, the transistor can be replaced by the equivalent circuit model.



* The rest of the circuit remains unchanged except that ideal constant dc voltage sources are replaced by short circuits.

* This is a result of the fact that the voltage across an ideal constant dc voltage source does not change and thus there will always be a zero voltage signal across a constant dc voltage source.

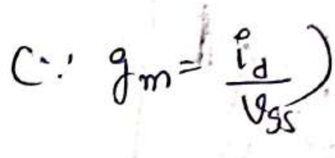
* An ideal constant dc current source can be replaced by an open circuit in the small-signal equivalent circuit of the amplifier.

* The most serious shortcoming of the small signal model is that it assumes the drain current in saturation is independent of the drain voltage.

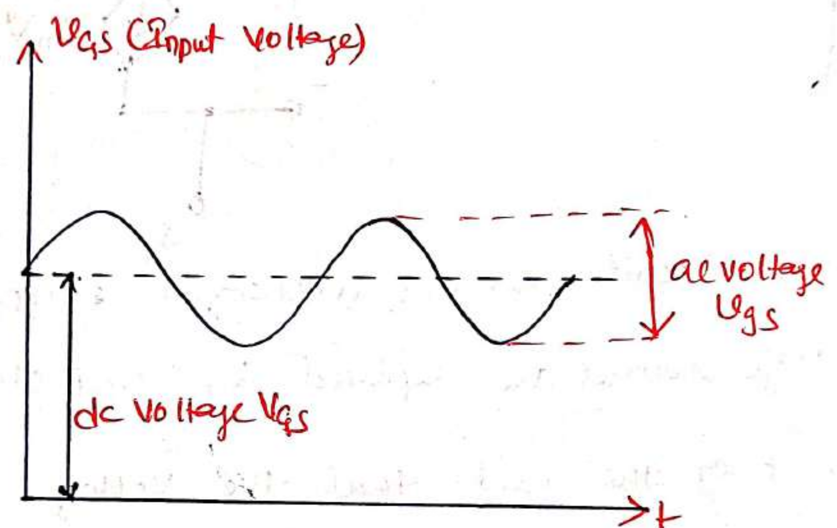
VOLTAGE GAIN:

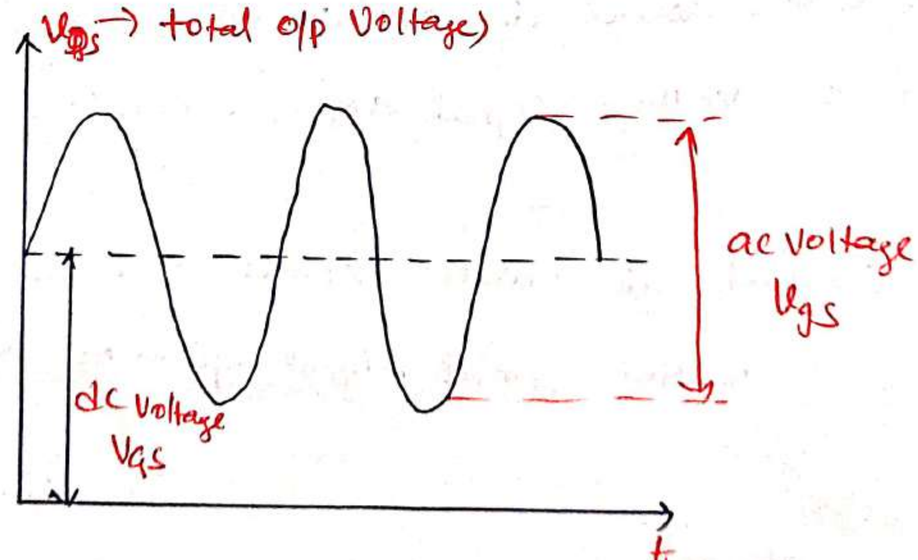
* The Voltage gain $A_V = \frac{v_{ds}}{v_{gs}}$

$$= \frac{i_d \cdot R_D}{v_{gs}}$$

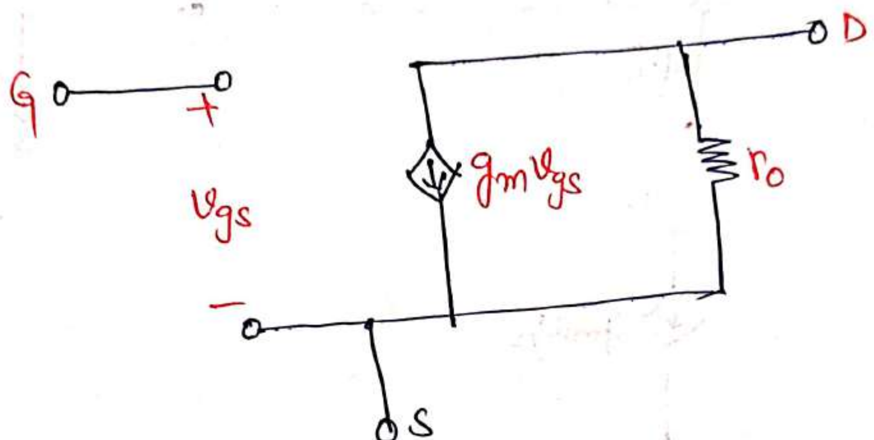


$$A_V = g_m \cdot R_D$$





* we know that the drain current does in fact depend on v_{DS} in a linear manner.
* Such dependence was modeled by a finite resistance r_o between drain and source.



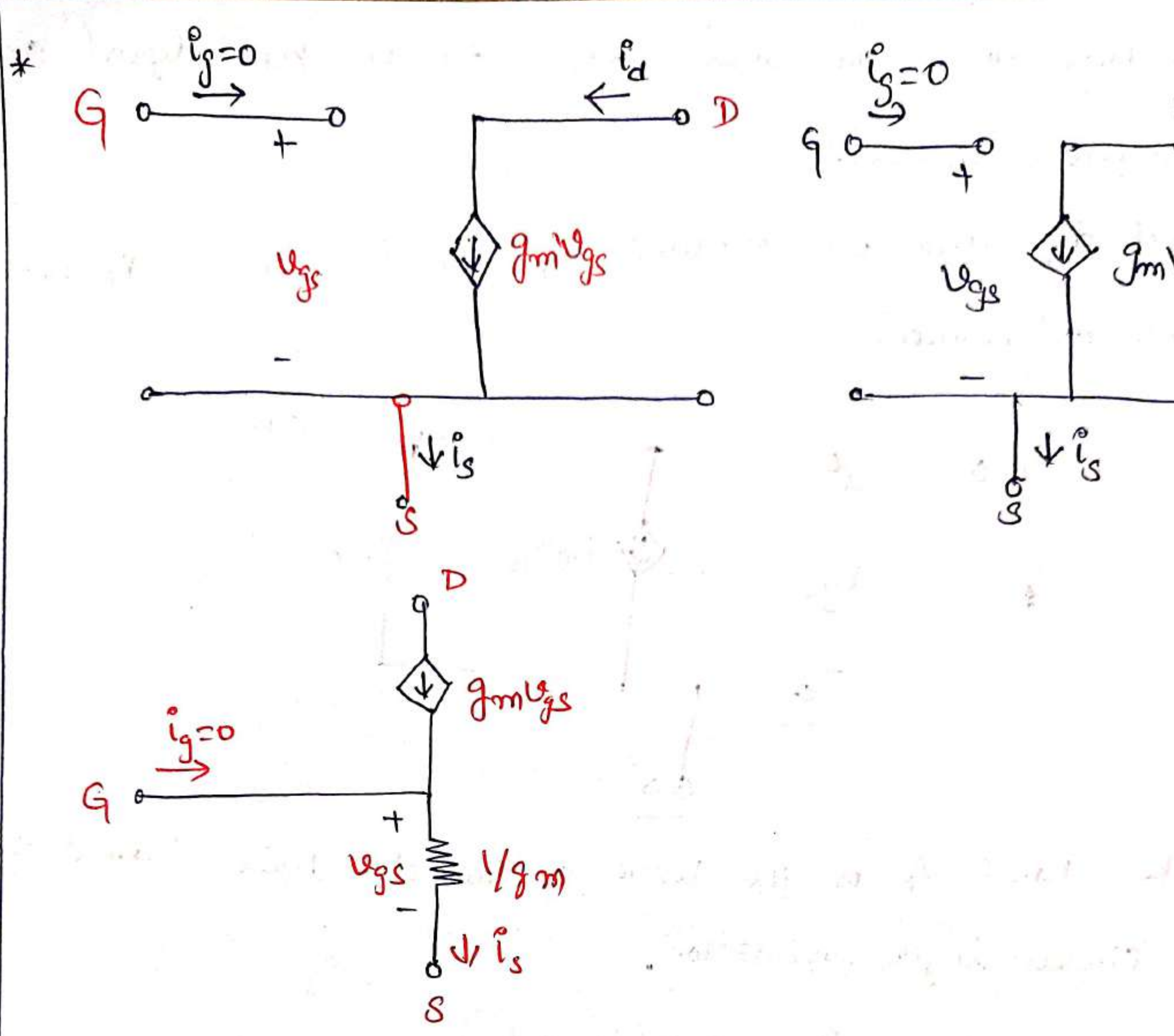
* The current I_D is the value of the dc drain current without the channel-length modulation,

$$I_D = \frac{1}{2} k_n \frac{W}{L} V_{GS}^2 .$$

The T Equivalent - Circuit Model:

* A simple circuit transformation it is possible to develop an alternative equivalent circuit model for the MOSFET.
* The development of such a model, known as the T model. the equivalent circuit studied above without r_o we have added a second $g_m v_{gs}$ current source in series with the original controlled source.

*

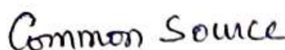


SINGLE-STAGE MOS AMPLIFIERS:

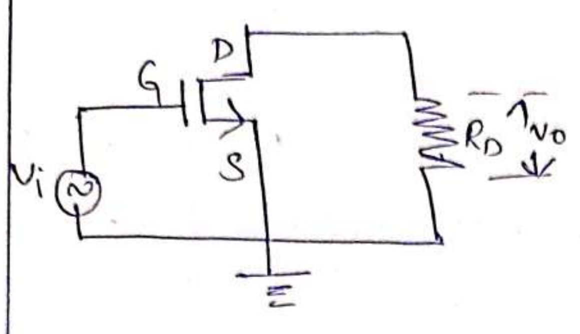
* There are three configurations for mos amplifier circuits

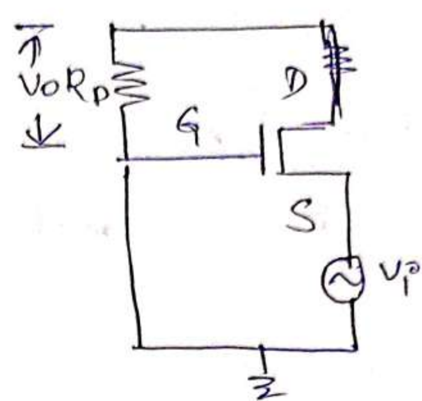
1. Common Source Configuration
2. Common Drain Configuration
3. Common Gate Configuration

Configuration	Gate	Source	Drain
CS	I/p	Common	O/p
CG	GND	I/p	O/p
CD	I/p	O/p	GND

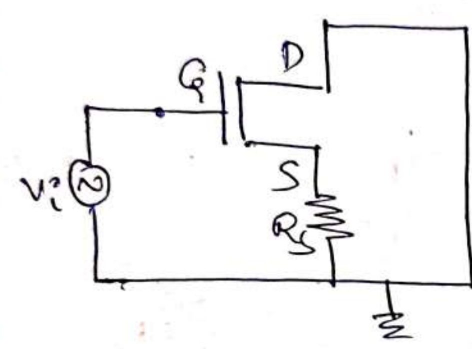


Common gate





Common Drain



* Amplifier circuit is converted to small signal model
* Find Input resistance, output resistance
* Voltage gain

COMMON SOURCE (CS) AMPLIFIER:

* The Common source (CS) or grounded source configuration is the most widely used for all MOSFET amplifier circuits
* A large capacitor C_S is connected between the source and ground. In this way, the signal current passes through C_S to ground and thus bypasses the output resistance of current source 'I' hence C_S is called a bypass capacitor.
* An voltage source V_{sig} with an internal resistance R_{sig} is connected to the gate through a large capacitor C_{C1} known as

Coupling capacitor is required to act as a perfect short circuit at all signal frequencies.

* The voltage signal resulting at the drain is coupled to the load resistance R_L via another coupling capacitor C_{C2}.

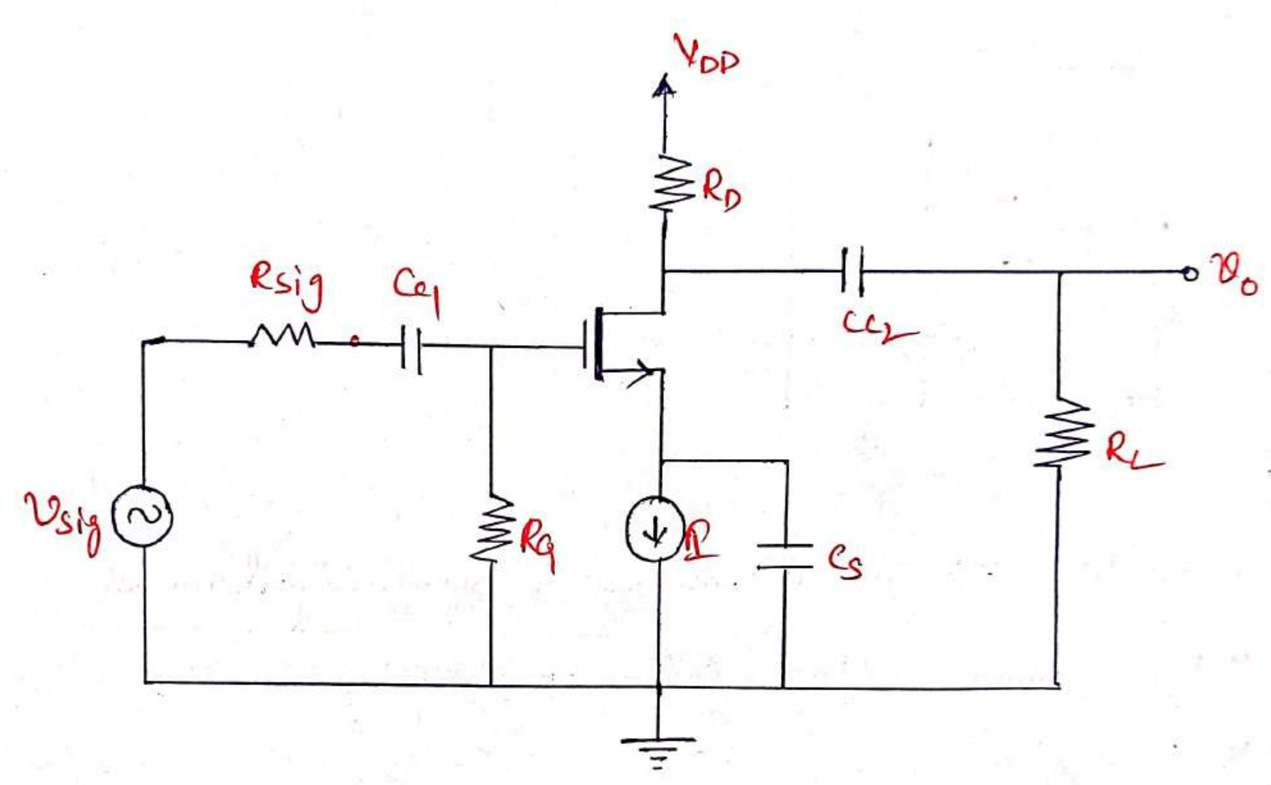
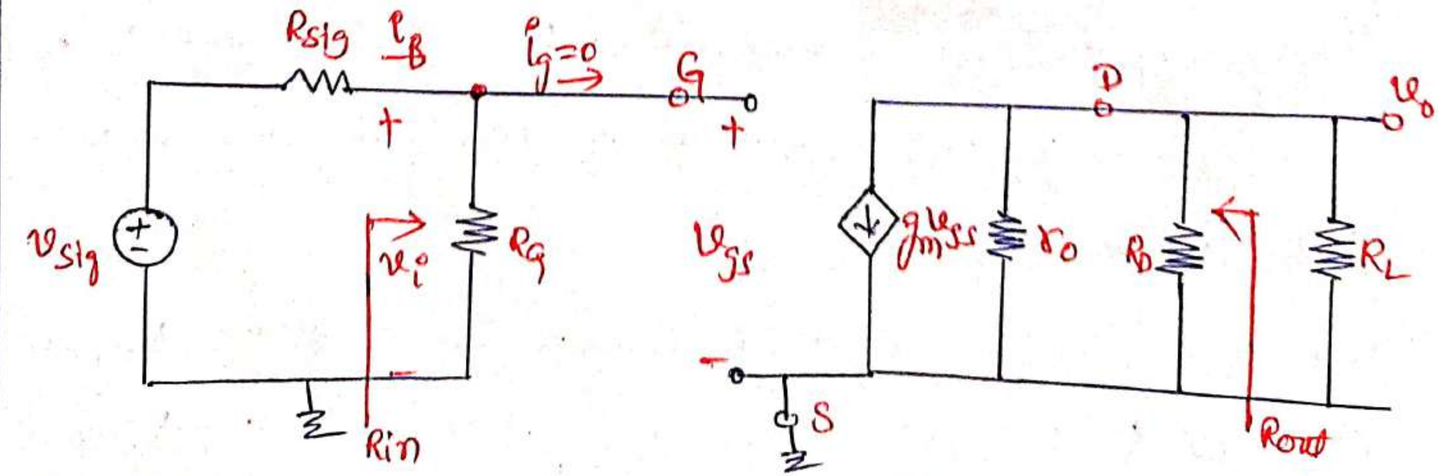


FIG: COMMON SOURCE AMPLIFIER

* To determine the terminal characteristics of the CS amplifier, i.e., its input resistance, voltage gain and output resistance. by replacing MOSFET with its small signal model.

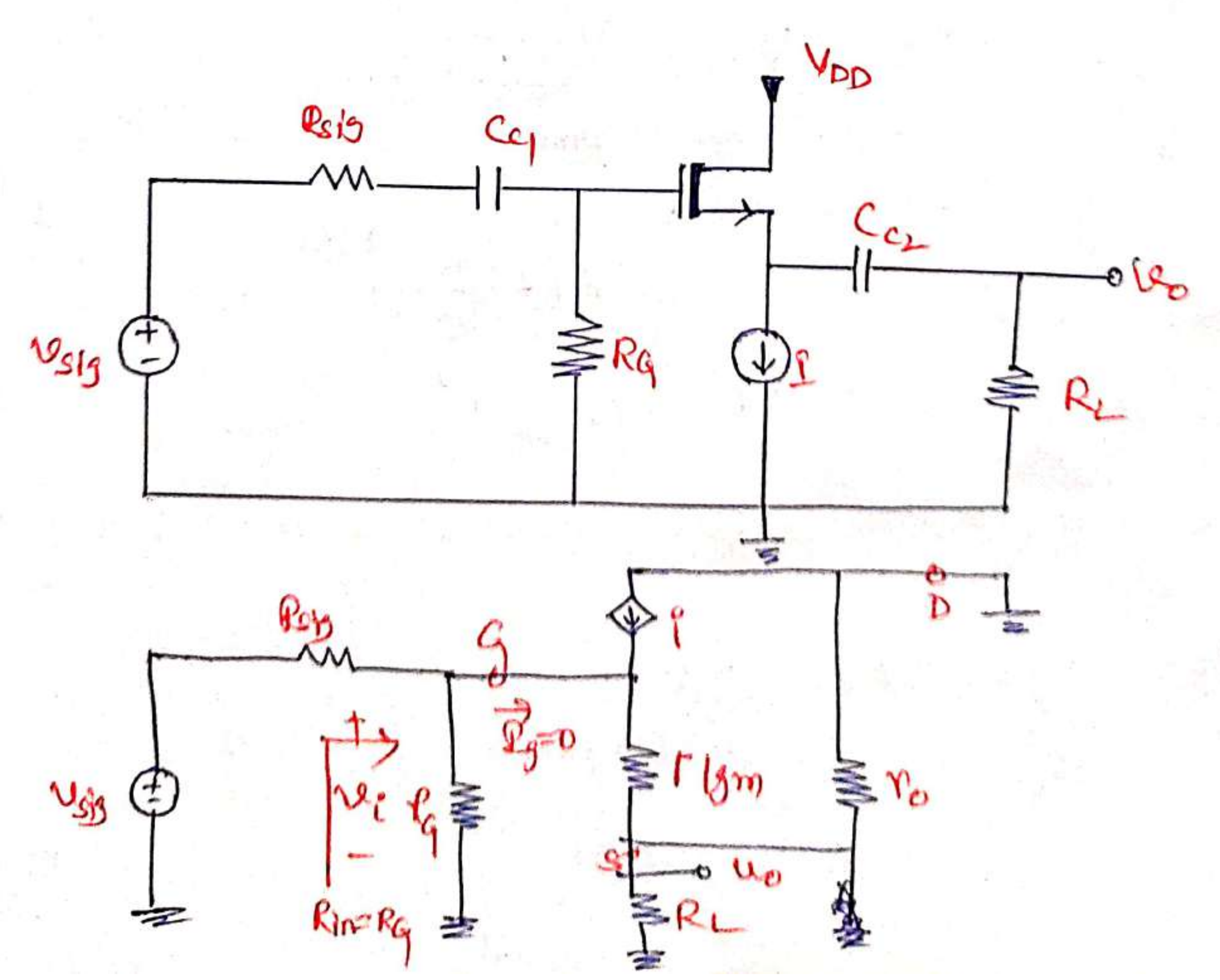


COMMON DRAIN or SOURCE-FOLLOWER AMPLIFIER:

* The given circuit shows a common drain amplifier since the drain is to function as a signal ground there is no need for resistor R_D and it has therefore been eliminated.

* The input signal is coupled via capacitor C_{C1} to the MOSFET gate and the output signal at the MOSFET source is coupled via capacitor C_{C2} to a load resistor R_L.

* Since R_L is in effect connected in series with the source terminal of the transistor source I acts as an open circuit as far as signals it is more convenient to use the MOSFET's T model. The resulting small-signal equivalent circuit of the common drain amplifier is as shown.



* The transistor has been replaced by its T-equivalent circuit model. In general whenever a resistance is connected in the source lead, instead the hybrid π model T model is preferred.

Input Resistance :

* $R_{in} = R_i = R_G = \infty$ as $i_g = 0$

Output resistance

$$R_O = R_D$$

Voltage Gain

$$A_V = \frac{V_o}{V_i}$$

from the circuit

$$v_{gs} = \frac{1/g_m}{1/g_m + R_s} * v_i$$

$$= \frac{1}{g_m\left(\frac{1+g_mR_s}{g_m}\right)} * v_i$$

$$v_{gs} = \frac{1}{1+g_mR_s} * v_i$$

$$v_i = v_{gs}(1+g_mR_s)$$

from the circuit

$$V_o = -i_D R_D$$

Voltage gain $A_V = \frac{-i_D R_D}{v_{gs}(1+g_mR_s)}$ $\left(\because g_m = \frac{i_D}{v_{gs}}\right)$

$$A_V = \frac{-g_m R_D}{1+g_mR_S}$$

At the input $i_g = 0$

$$R_{in} = R_G$$

$$v_i = \frac{R_{in}}{R_{in} + R_{sig}} v_{sig}$$

$$v_i = \frac{R_G}{R_G + R_{sig}} v_{sig}$$

Input resistance:

$$R_{in} = R_G = \infty \quad (\because i_g = 0 \text{ as gate is input terminal})$$

Output resistance:

$$R_{out} = r_o \| R_D = \frac{r_o R_D}{r_o + R_D}$$

Here, $r_o >> R_D$

$$\boxed{R_{out} = R_D}$$

Voltage Gain Av

$$A_V = \frac{V_o}{V_i}$$

from the circuit $V_o = -i_d (R_D \| r_o)$

$$A_V = \frac{-i_d (R_D \| r_o)}{v_{gs}} \quad (\because g_m = i_d / v_{gs})$$

$$A_V = -g_m (R_D \| r_o)$$

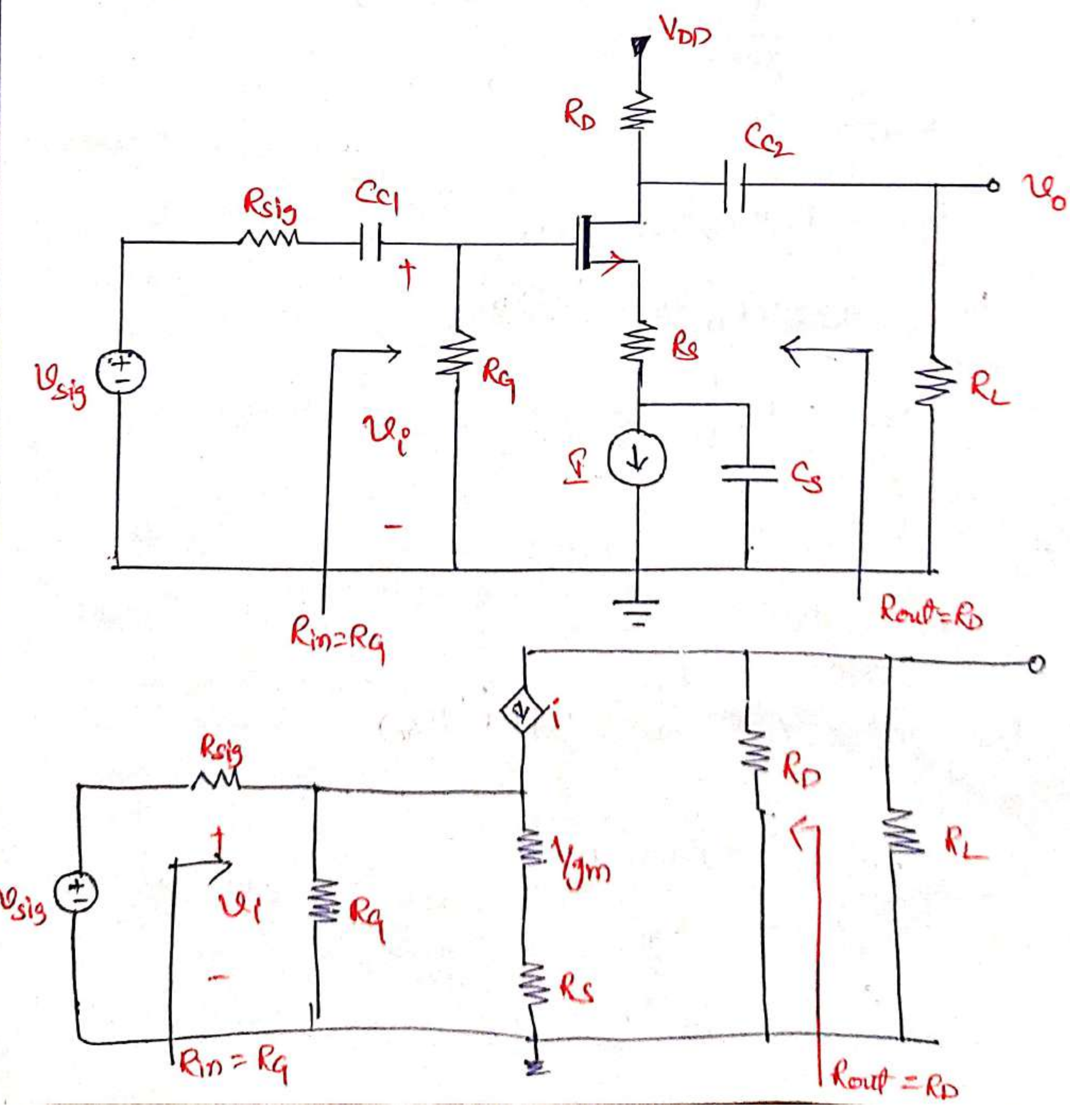
Overall Voltage gain:

$$G_v = \frac{v_o}{v_{sig}} = \frac{v_o}{v_{in}} \quad (\because v_{sig} = v_{in})$$

$$\boxed{G_v = -g_m (R_d \parallel R_o)}$$

COMMON SOURCE AMPLIFIER WITH SOURCE RESISTOR:

* It is often beneficial to insert a resistance R_s in the source lead of the common source amplifier. The corresponding small-signal equivalent circuit.



Input Resistance:

* The input resistance R_{in} is given by,

$$R_{in} = R_G$$

$$\because i_g = 0 \quad R_i = \infty$$

output resistance :-

1/gm
ro

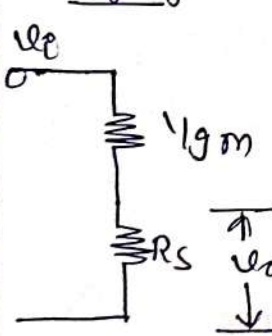
* The output resistance is given by,

$$R_{out} = 1/g_m \,||\, R_L r_o$$

$$\because R_o << 1/g_m$$

$$\boxed{R_{out} = 1/g_m}$$

Voltage gain :



The voltage gain A_v is given by

$$A_v = \frac{V_o}{V_i}$$

from the circuit

$$v_o = \frac{R_S}{R_S + 1/g_m} * v_i$$

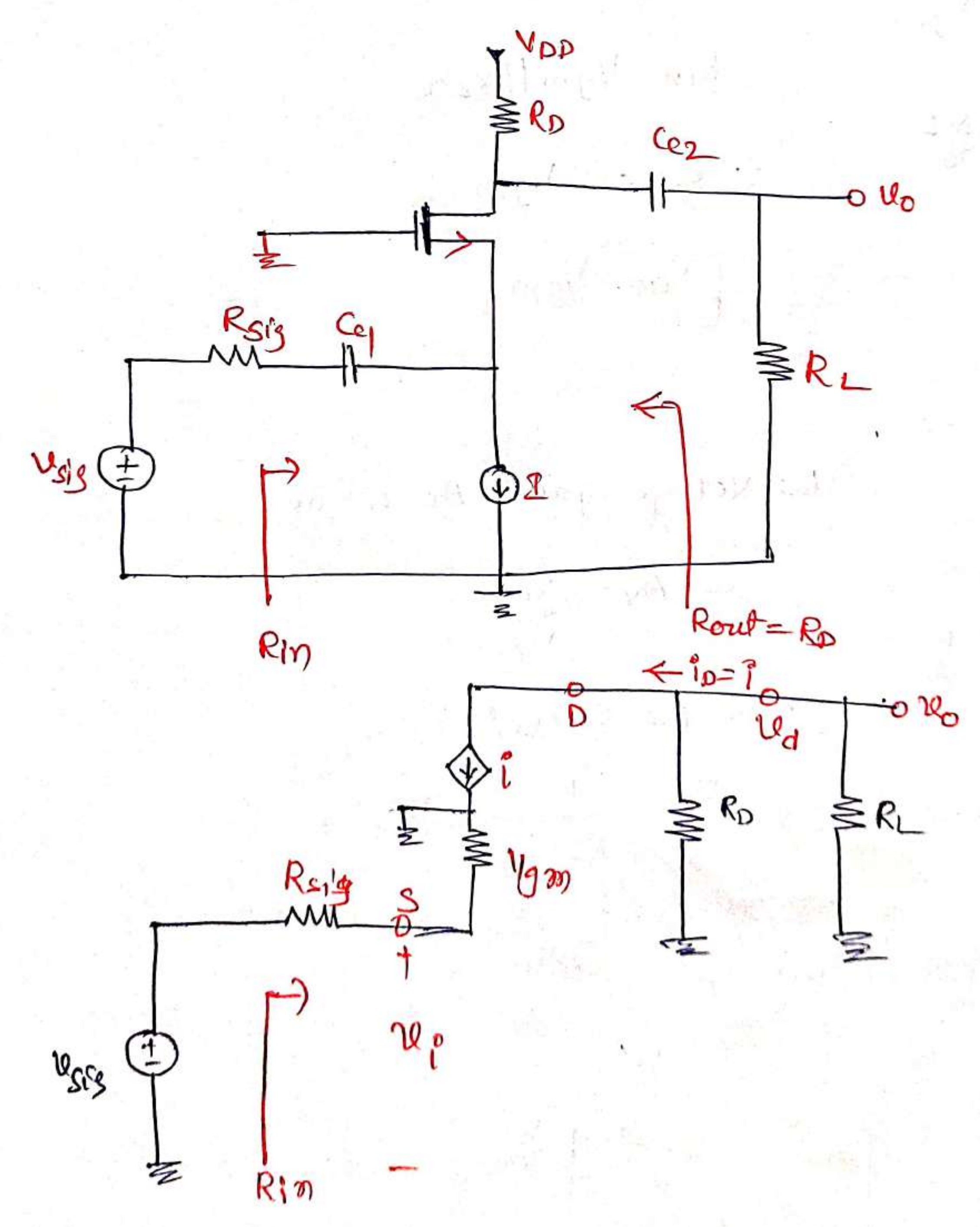
$$A_V = \frac{\frac{R_S}{R_S + 1/g_m} * v_i}{v_i}$$

$$\boxed{A_V = \frac{R_S}{R_S + 1/g_m}}$$

COMMON-GATE AMPLIFIER :-

* The input signal is applied to the source and the output is taken at the drain with the gate forming a common terminal between the input and output ports.

* Observe that since both dc and ac voltages at the gate are to be zero, we have connected the gate directly to ground thus eliminating resistor R_G altogether.



Input resistance

* From the circuit, the input resistance is given by,

$$R_{in} = 1/g_m$$

Output resistance

the output resistance is given by,

$$R_O = R_D$$

Voltage Gain :

from the circuit $v_o = -i_d R_D$

v_{sig} R_{sig} R_{in} v_i

$$v_i = \frac{R_{in}}{R_{in} + R_{sig}} * v_{sig}$$

$$A_V = \frac{v_o}{v_i}$$

$$= \frac{-i_d R_D}{\frac{R_{in}}{R_{in} + R_{sig}}} * v_{sig}$$

$$\boxed{A_V = \frac{-i_d R_D (R_{in} + R_{sig})}{R_{in}} * v_{sig}}$$

BODY EFFECT:

* The body effect occurs in a MOSFET when the source is not tied to substrate. Thus the substrate (body) will be at signal ground but since the source is not, a signal voltage v_{bs} develops between the body (B) and the source (S).

* That the substrate acts as a "second gate" or a backgate for the MOSFET. Thus the signal v_{bs} gives rise to a drain-current component, which we shall write as $g_m v_{bs}$, where g_{mb} is the body transconductance

$$g_{mb} = \left. \frac{\partial i_D}{\partial v_{BS}} \right|_{\substack{v_{GS} = \text{Constant} \\ v_{DS} = \text{Constant}}}$$